

Standard Sequential Modules

CS 140 Lecture 15 Sequential Modules

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1. Serial Adders
2. Serial Multipliers
3. Register
4. Counter

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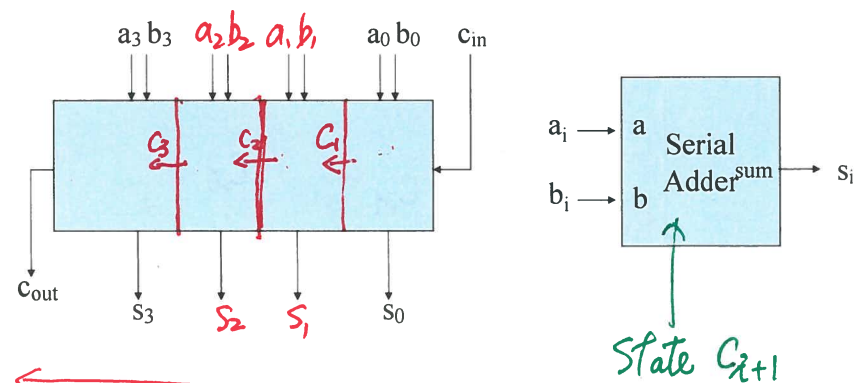
Motivation for Serial Adders and Multipliers

- Tradeoff of silicon area and system performance
 - Perform process in a series of time
- Utilization of FPGA architecture
 - Slice operation bitwise
- Metrics of Cost, Speed, and Power
- Ad: Cheaper hardware, Fit for FPGA architecture, Pipelining for excellent throughput
- Dis: Longer latency

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Serial Adder: Perform serial bit-addition

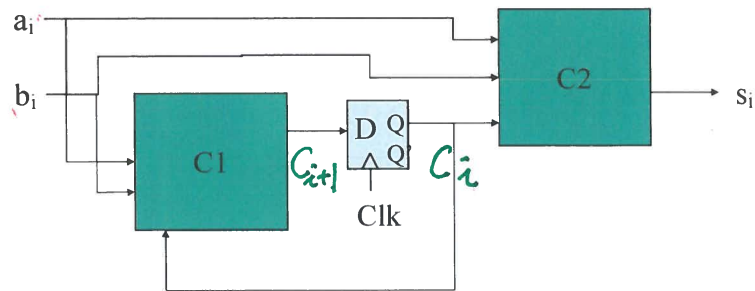
At time i , read a_i and b_i . Produce s_i and c_{i+1}
Internal state stores c_i . Carry bit c_0 is set as c_{in}



Space ←
Time ←

4

Serial Adder using D F-F



Feed a_i and b_i and generate s_i at time i .
Where is c_i and c_{i+1} ?

$$\begin{array}{r} 5 \\ + 7 \\ \hline 12 \end{array}$$

$$\begin{array}{r} 1100 \\ + 1111 \\ \hline 11000 \end{array}$$

$c_{in}=0$

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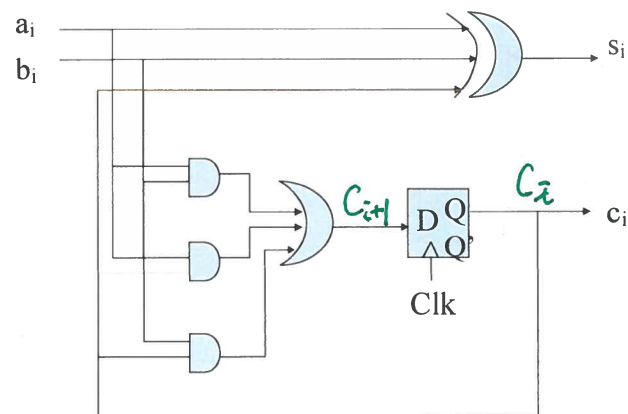
Serial Adder using a D Flip-Flop

id	a_i	b_i	c_i	c_{i+1}	s_i
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	0	1
3	0	1	1	1	0
4	1	0	0	0	1
5	1	0	1	1	0
6	1	1	0	1	0
7	1	1	1	1	1

$D=c_{i+1}$
 $Q=c_i$

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Serial Adder using a D Flip-Flop Logic Diagram



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Multiplication using Serial Addition

$$3 \times 5 = 15$$

$$\begin{array}{r} 011 \\ \times 101 \\ \hline 011 \\ 000 \\ + 011 \\ \hline 01111 \end{array}$$

$$\begin{array}{r} a_2 a_1 a_0 \\ \times b_2 b_1 b_0 \\ \hline a_2 b_0 a_1 b_0 a_0 b_0 \\ a_2 b_1 a_1 b_1 a_0 b_1 \\ + a_2 b_2 a_1 b_2 a_0 b_2 \\ \hline m_5 m_4 m_3 m_2 m_1 m_0 \end{array}$$

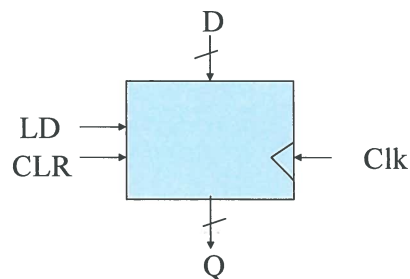
For $m=A \times B$, set $m^{(0)}=0$

At time i , perform $m^{(i+1)}=m^{(i)}+A b_i 2^i$

$\uparrow$
 i th bit of B

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Register



CLR: initialize the content

Priority: CLR
2. LD

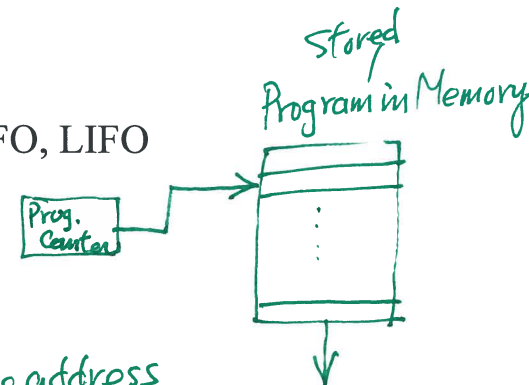
$$Q(t+1) = (0, 0, \dots, 0) \\ = D \\ = Q(t)$$

if CLR = 1
if LD = 1 and CLR = 0
if LD = 0 and CLR = 0

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Counter

- Program Counter
- Address Keeper: FIFO, LIFO
- Clock Divider
- Sequential Machine



Program Counter:
Increment the address
by one word (instruction)
as a default.

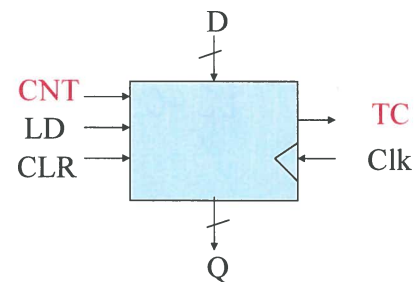
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Counter

- Modulo-n Counter
- Modulo Counter ($m < n$)
- Counter (a-to-b)
- Counter of an Arbitrary Sequence
- Cascade Counter

Modulo-n Counter



Priority
1. CLR
2. LD
3. CNT

$$Q(t+1) = (0, 0, \dots, 0) \\ = D \\ = (Q(t) + 1) \bmod n \\ = Q(t)$$

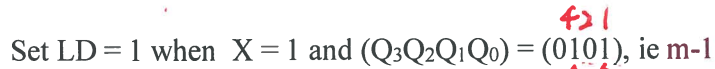
TC = 1 if $Q(t) = n-1$ and CNT = 1
TC = 0 otherwise

if CLR = 1
if LD = 1 and CLR = 0
if LD = 0, CNT = 1 and CLR = 0
if LD = 0, CNT = 0 and CLR = 0

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Given a mod 16 counter, construct
a mod-m counter ($0 < m < 16$) with AND, OR, NOT gates



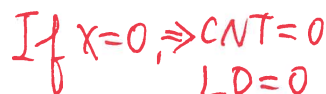
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Given a mod 16 counter, construct an a-to-b counter ($0 \leq a \leq b \leq 15$)



Given a mod 8 counter, construct a counter with sequence 0 → 1 → 5 → 6 → 2 → 3 → 7 → 0

When $Q = 3$, load $D = 7$



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Given a mod 8 counter, construct a counter with sequence 0 → 1 → 5 → 6 → 2 → 3 → 7

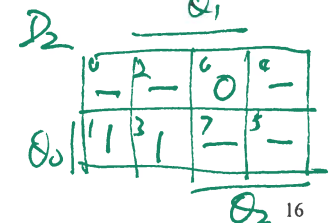
K Mapping LD and D,
we get

$$LD = Q_2'Q_0 + Q_2Q_0'$$

$$D_2 = Q_0$$

$$D_1 = Q_1$$

$$D_0 = Q_0$$



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Counter of an Arbitrary Sequence

Example: Count in sequence 0 2 3 4 5 7 6

LD = 1 D = 2 When Q(t) = 0
 LD = 1 D = 7 When Q(t) = 5
 LD = 1 D = 6 When Q(t) = 7
 LD = 1 D = 0 When Q(t) = 6

Through K-map, we derive

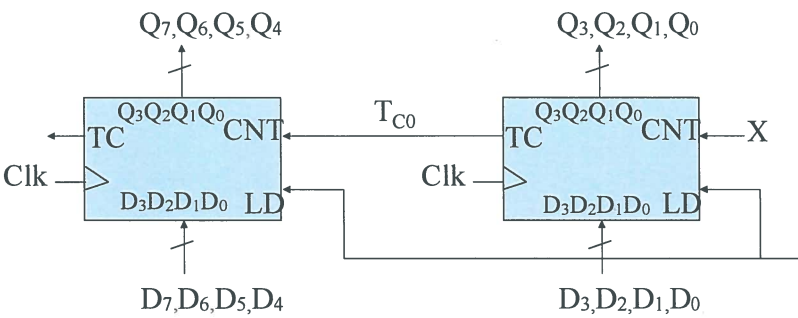
$LD = Q_2' Q_1' + Q_2 Q_0 + Q_2 Q_1$
 $D_2 = Q_0$
 $D_1 = Q_1' + Q_0$
 $D_0 = Q_1' Q_0$

Id	$Q_2Q_1Q_0$	LD	D_2	D_1	D_0
0	000	1	0	1	0
1	001	-	-	-	-
2	010	0	-	-	-
3	011	0	-	-	-
4	100	0	-	-	-
5	101	1	1	1	1
6	110	1	0	0	0
7	111	1	1	1	0

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Cascade Counter

A Cascade Modulo 256 Counter



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Cascade Counter

$TC = 1$ when $(Q_3, Q_2, Q_1, Q_0) = (1, 1, 1, 1)$ and $X = 1$
 $(Q_7(t+1) Q_6(t+1) Q_5(t+1) Q_4(t+1)) = (Q_7(t) Q_6(t) Q_5(t) Q_4(t)) + 1 \bmod 16$
 when $T_{C0} = 1$

The circuit functions as a modulo 256 counter.

Time	0	1	2	3	...	13	14	15	16	17	18	19
Q_{7-4}	0	0	0	0	...	0	0	0	1	1	1	1
T_{C0}	0	0	0	0	...	0	0	1	0	0	0	0
Q_{3-0}	0	1	2	3	...	13	14	15	0	1	2	3

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System Designs

CSE 140 Lecture 16 System Designs

Methodology

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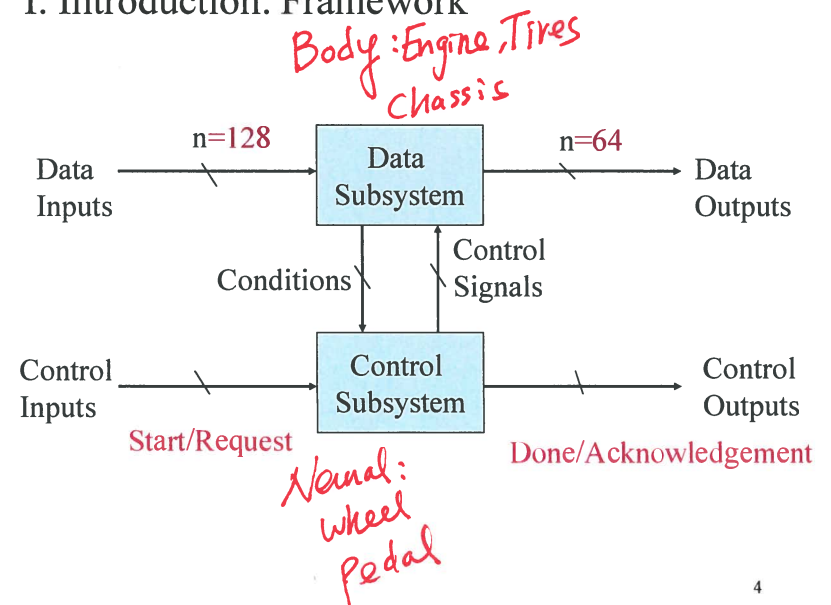
- Introduction
 - Methodology and Framework
- Components
- Specification
- Implementation

Introduction

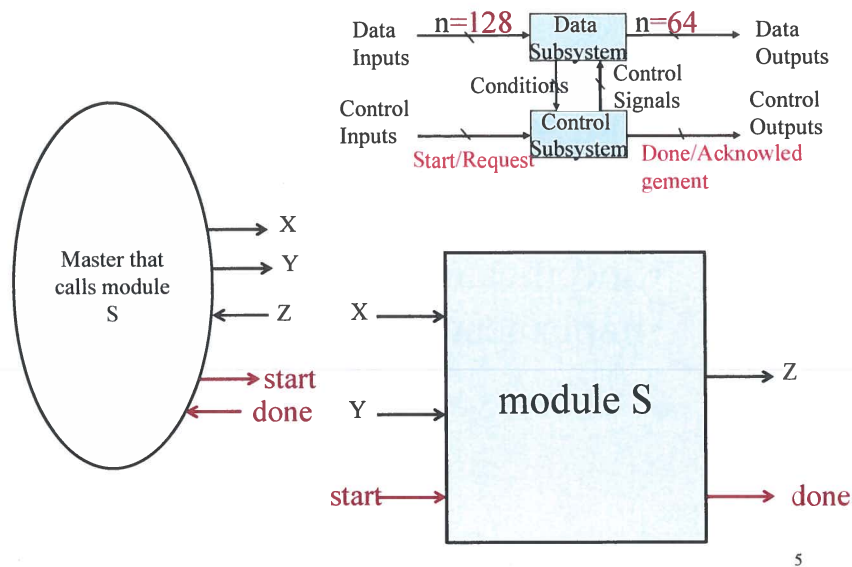
- Methodology
 - Approach with success stories.
 - Hierarchical designs with interface between the modules (BSV).
10 billions trans.
- Data Subsystem and Control Subsystem
 - For n-bit data, each operation takes n times or more in hardware complexity.
 - Data subsystem carries out the data operations and transports.
 - Control system sequences the data subsystem and itself.

Design Flow
System Level
RTL Logic Synthesis (Kmap)
Physical Layout
Verification
Verilog VHDL

I. Introduction: Framework

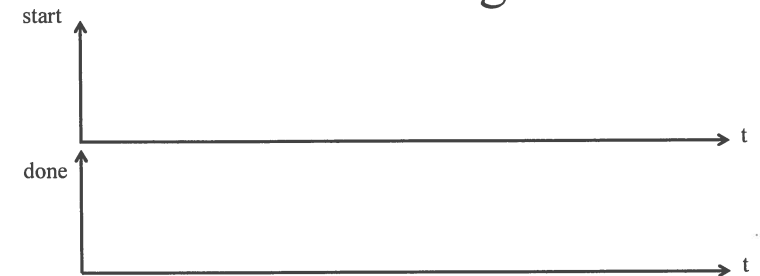


I. Introduction: Handshaking



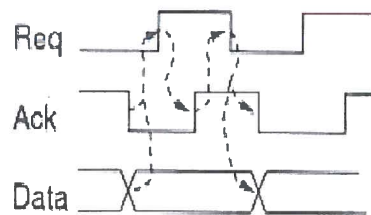
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Handshaking



6

Handshaking



7

Handshaking: Example

The master module that calls module S controls the following signals

- A. Signal **start**
- B. Signal **done**
- C. Signals **start** and **done**
- D. None of the above

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4-Phase Handshaking

A Hello, Could I
Speak to B

↗

Thx^{is} B

↖ B speaking

Thank you for
your time

↗

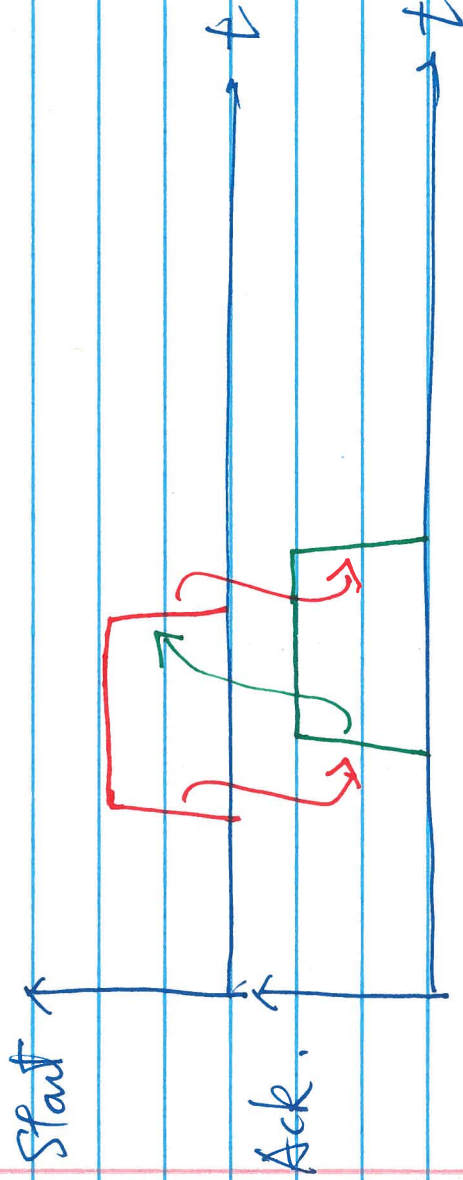
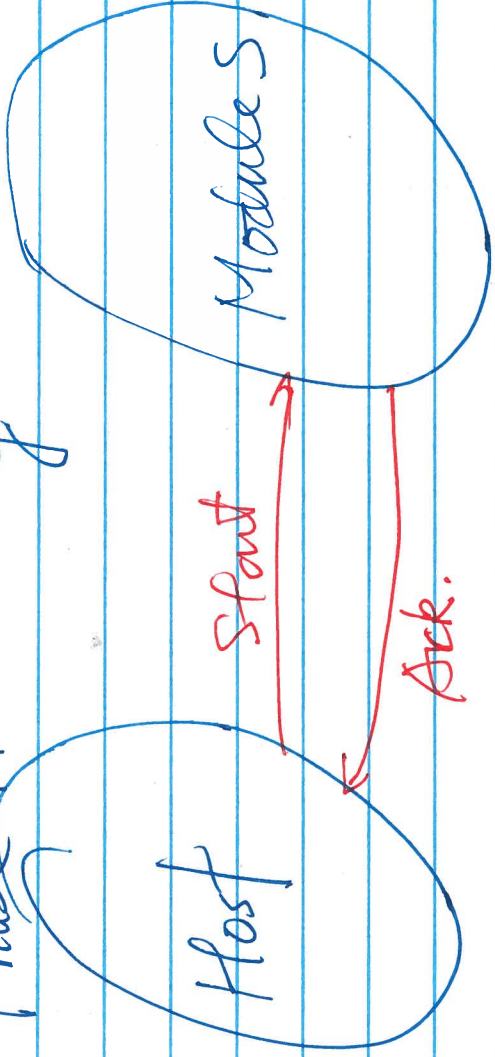
You are
welcome!

↖

1. What is the main purpose of the document?
 2. What are the key findings of the study?
 3. What are the implications of the findings?
 4. What are the limitations of the study?
 5. What are the conclusions of the study?

[illegible]

4-Phase Handshaking



Sender wants to start the operation

raises $Start = 1$

Receiver detects $start = 1$,

raises $Ack = 1$

Sender detects $Ack = 1$

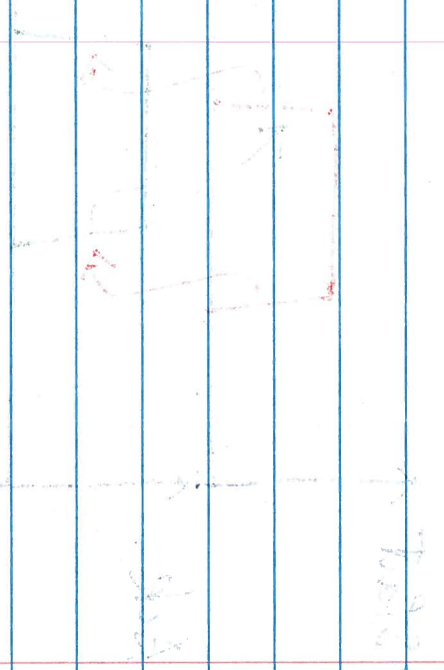
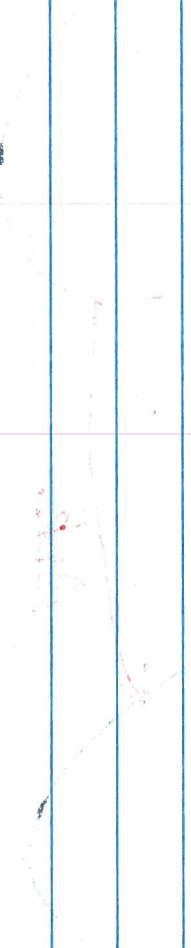
lowers $Start = 0$

Receiver detects $Start = 0$

lowers $Ack = 0$

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