

CSE 140: Components and Design Techniques for Digital Systems

Lecture 10:

Sequential Networks: Timing and Retiming

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Timing

- Motivation
- Basic Timing Characteristic
 - Gate Delay, Interconnect Delay
 - Flip-Flop Timing Window
- Two Timing Constraints: shortest and longest timing paths
 - Examples
- Clock Skews and Retiming
 - Examples

Timing: Motivation

- Clock specifies a precise time for the next state
 - In general, we allocate one clock period for signal propagation between registers. **Goldilocks** timing.
- Too late: Fail to reach for the **setup** of the next state.
- Too early: Race to disturb the **holding** of the next state.
- Analysis: Verify the timing of the system.
- Goal: A robust design.

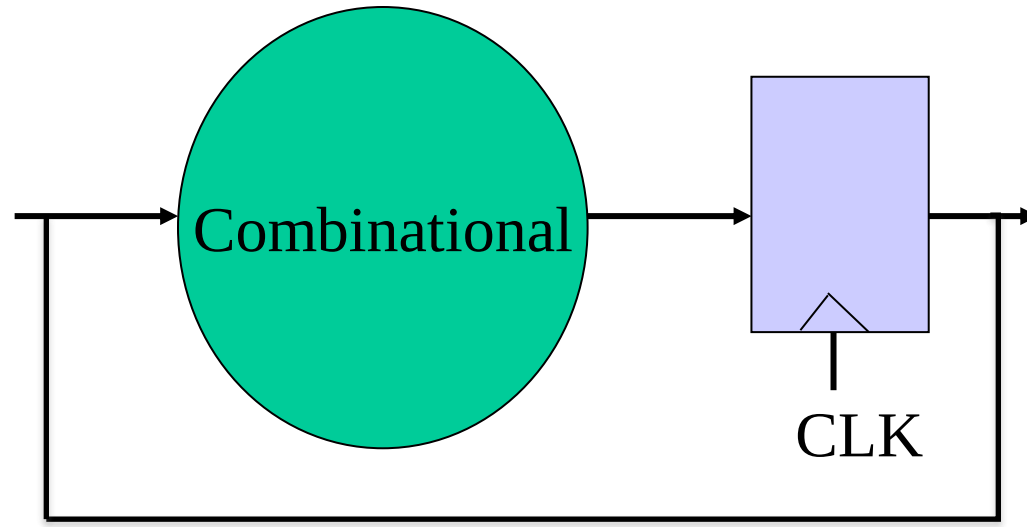
The Story of Goldilocks and the Three Bears

Once upon a time, there was a little girl named **Goldilocks**. She went for a walk in the forest. Pretty soon, she came upon a house. She knocked and, when no one answered, she walked right in. At the table in the kitchen, there were three bowls of porridge. Goldilocks was hungry. She tasted the porridge from the first bowl. "This porridge is **too hot**!" she exclaimed. So, she tasted the porridge from the second bowl. "This porridge is **too cold**," she said. So, she tasted the last bowl of porridge. "Ahhh, this porridge is **just right**," she said happily and she ate it all up.

DLTK's Crafts for Kids

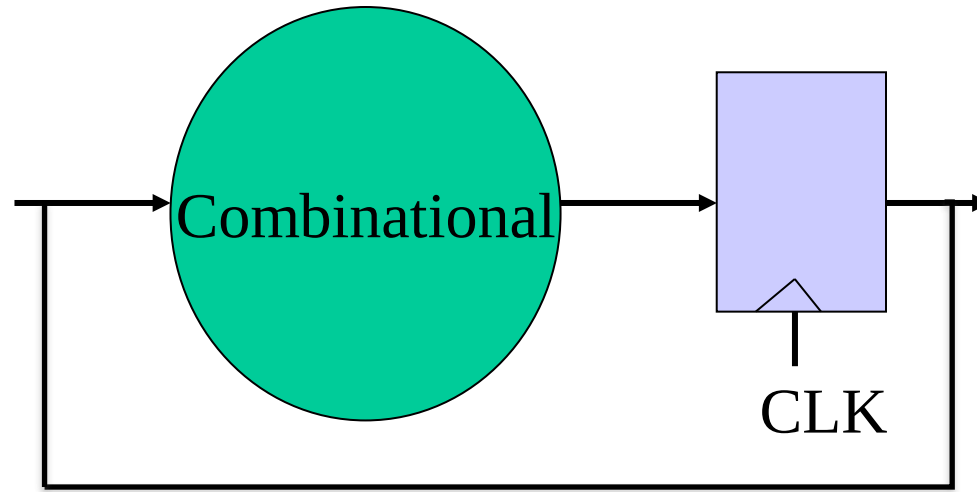


Motivation: So far



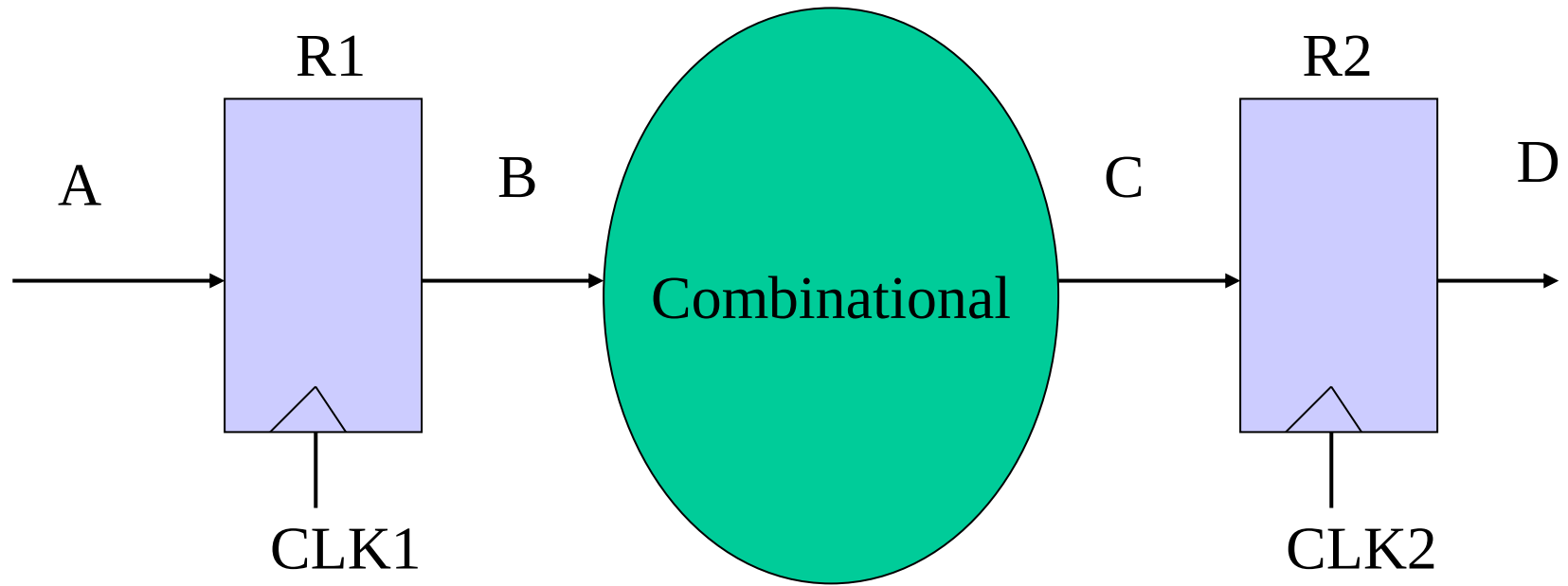
Logic-level analysis

Motivation: This lecture ...



- When does our (seemingly logically correct) design go wrong?
- How can we design a circuit that works under real constraints?
- Popular interview questions.

Motivation: Sequential Networks



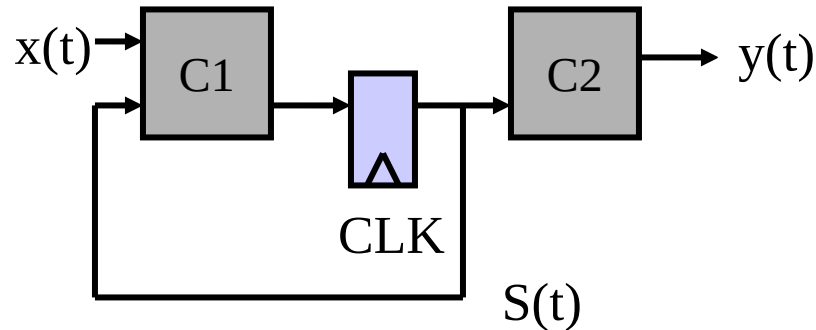
A typical sequential network has combinational circuit between registers (R1 to R2).

The registers are synchronized by clocks (CLK1 and CLK2).

Timing is set between clocks (CLK1 and CLK2).

The beauty of the synchronized design is that we need only to take care of the timing of the regions separated by the registers.

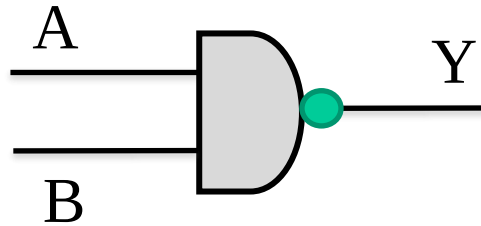
Timing of the System



For a synchronized digital Moore machine, we take care of the timing of the following three groups of paths between:

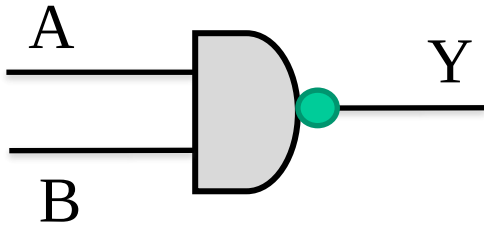
- Every pair of registers,
- Each input and register, and
- Each register and output.

Basic Timing Characteristics: Gate Delay



- I. Min delay of a gate, also called **Contamination delay: t_{cd}**
Minimum time from when an input changes until the output *starts* to change
- II. Max delay of a gate, also called **Propagation delay: t_{pd}**
Maximum time from when an input changes until the output *is* guaranteed to reach its final value (i.e., stop changing)

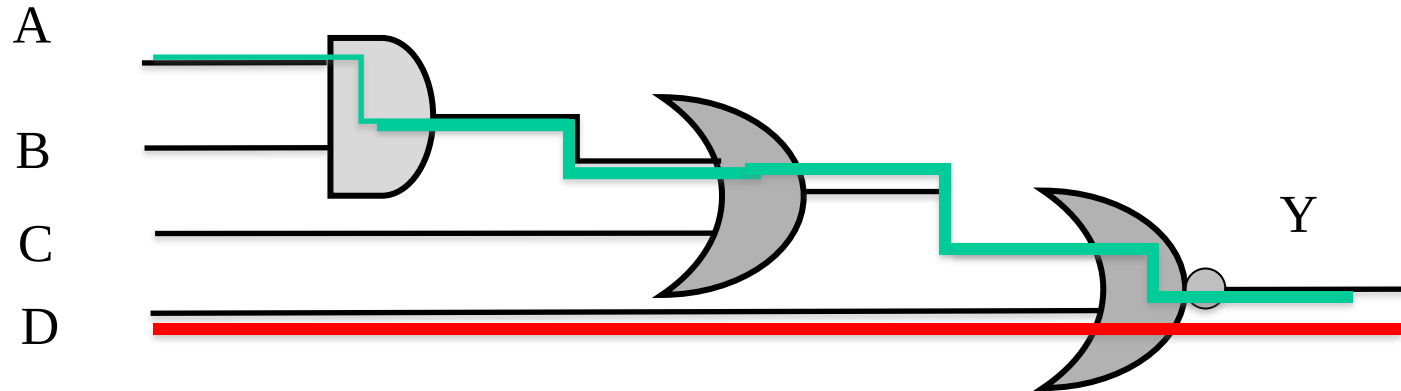
Gate Delay: Combinational Logic Timing



$A_t B_t$	$A_{t+1} B_{t+1}$	$Y = (AB)'$
00	11	$1 \Rightarrow 0$
01	11	$1 \Rightarrow 0$
10	11	$1 \Rightarrow 0$
11	11	$0 \Rightarrow 0$

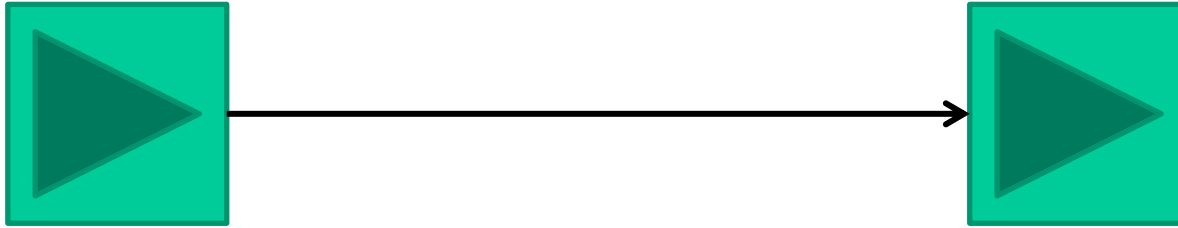
Different situation causes different delay at output, e.g.
input patterns, process variations, noises, temperature, aging

Combinational Logic Delay



Different path causes different output transition delay.

Interconnect Delay



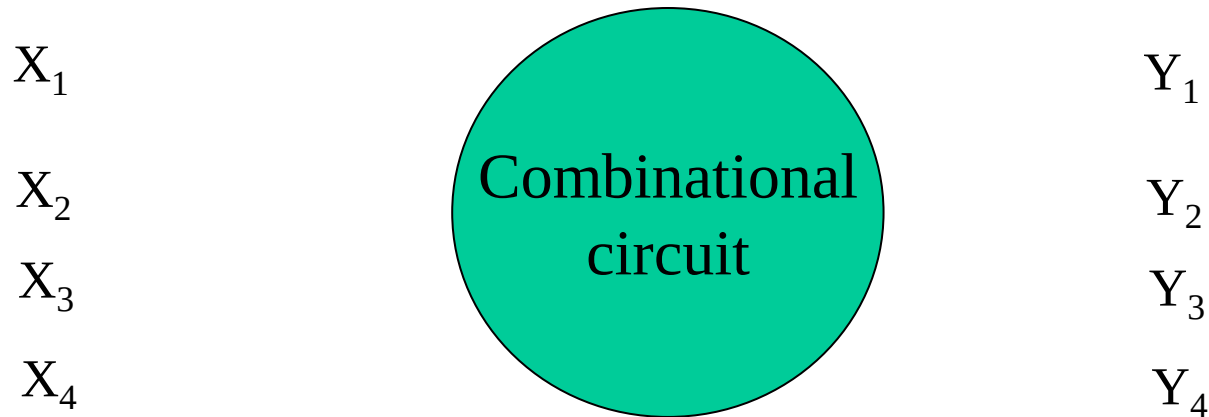
Speed of light: $C/\sqrt{\epsilon} \approx 1.5 \times 10^{10}$ cm/s

For 1cm, it takes $0.7 \times 10^{-10} s = 70ps$ (*picosecond*)
for the light to reach from one end to the other end.

Chain of buffers: 5-40 times of speed of light.

For 5GHz, the clock period is $200ps/cycle$.

Combinational Logic: Output timing constraints



I. Contamination delay (shortest): t_{cd}

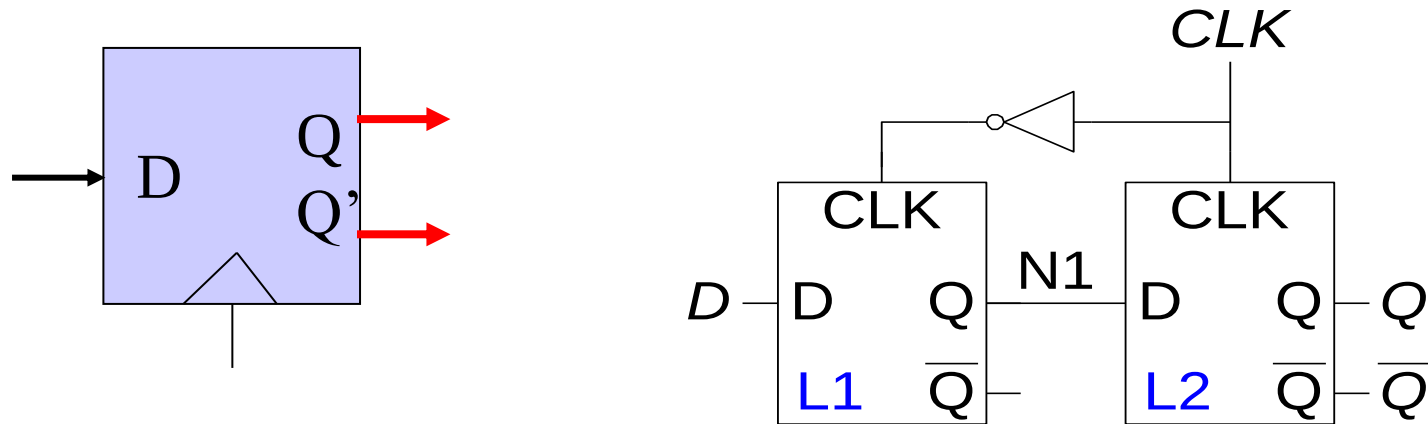
Minimum time from when an input changes until any output *starts* to change

II. Propagation delay (longest): t_{pd}

Maximum time from when an input changes until the output *or* outputs of a combinational circuit are guaranteed to reach their final value (i.e., stop changing)

Flip-Flop Timing Window

Timing: Setup Time and Hold Time Constraints



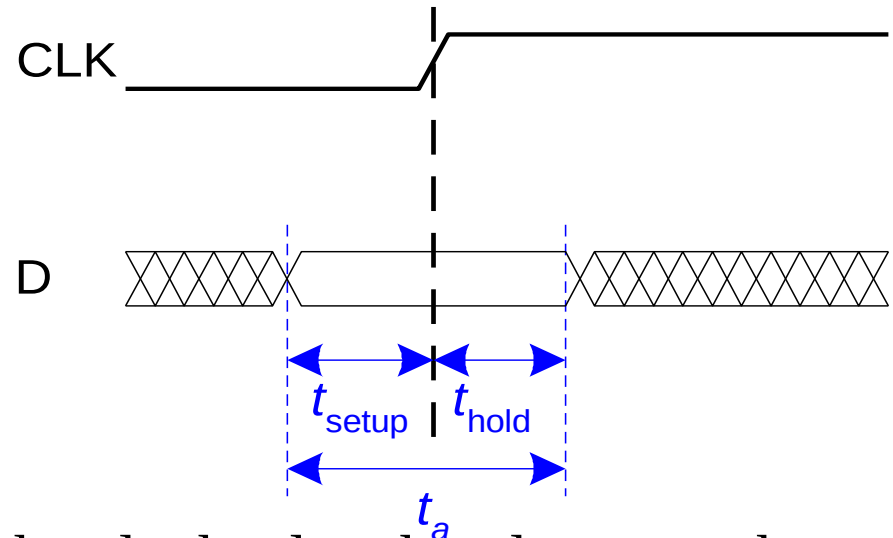
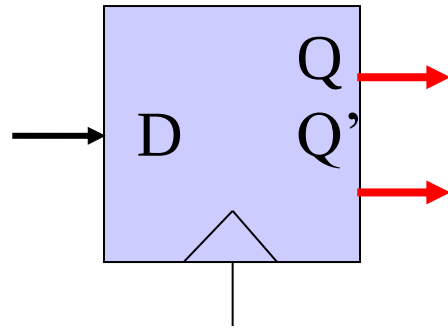
Once a flip flop has been ‘built’ we are stuck with its timing characteristics:

t_{setup} , t_{hold} timing relation between D and CLK

t_{ccq} , t_{pcq} timing relation between CLK and Q

No direct timing relation between input D and output Q

FF Input Constraints: Set up and hold time



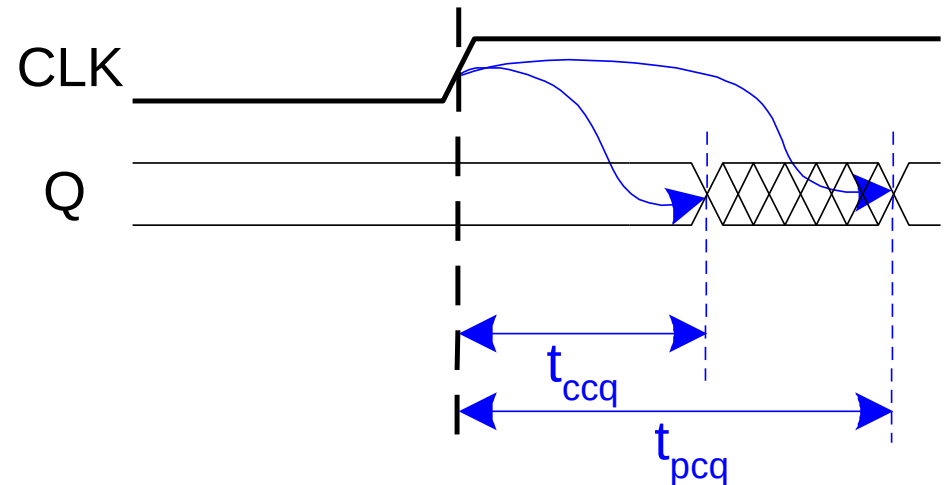
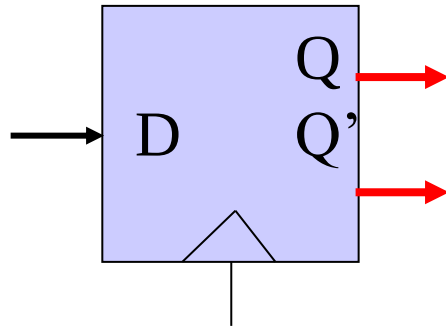
Setup time t_{setup} Time *before* the clock edge that data must be stable (i.e. no change)

Setup time violation This occurs if the input signal D does not settle (**set up**) to the stable value at least t_{setup} *before* the clock edge.

Hold time t_{hold} Time *after* the clock edge that data must be stable

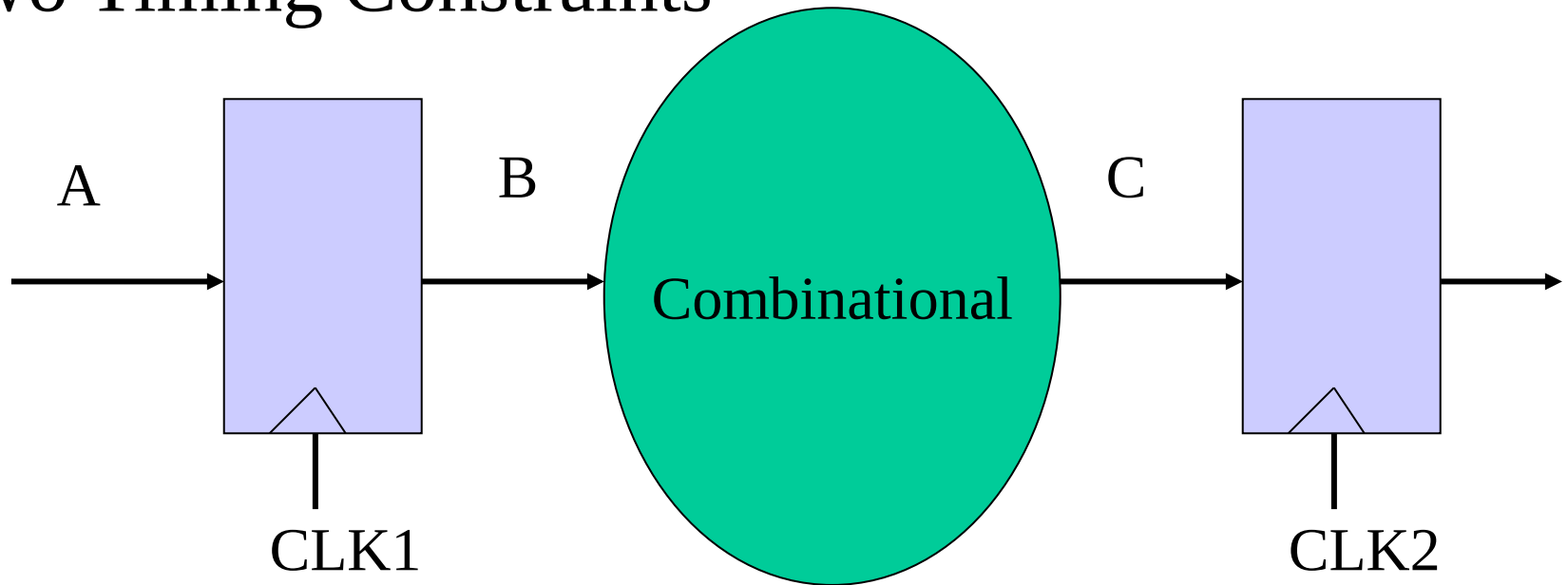
Hold time violation This occurs if the input signal D does not remain unchanged (**hold**) for at least t_{hold} *after* the clock edge.

FF Output Timing Constraints



- Propagation delay: t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- Contamination delay: t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)

Two Timing Constraints



$$t_{cq} + t_{comb} + t_{setup} \leq T$$

$$t_{hold} < t_{cq} + t_{comb}$$

t_{cq} : time from rising edge of clock to Q update (**CLK1**⇒**B**)

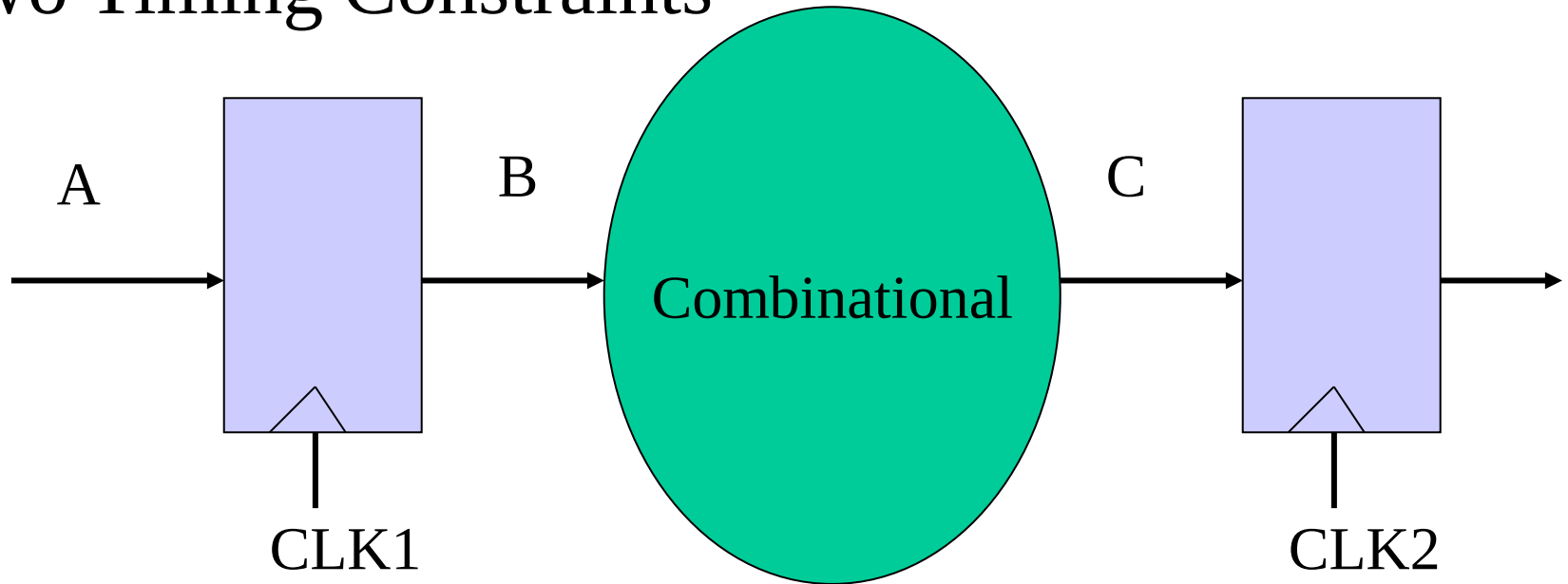
t_{comb} : time of combinational logic delay (**B**⇒**C**)

t_{setup} : setup time before rising edge of clock (**C**⇒**CLK2**)

t_{hold} : hold time after the rising edge of clock

T : clock period (**CLK1**⇒**CLK2**)

Two Timing Constraints



Setup time constraint Longest delay from CLK1 to CLK2

$$t_{cq} + t_{comb} + t_{setup} \leq T \implies \max(t_{cq} + t_{comb} + t_{setup}) \leq T$$

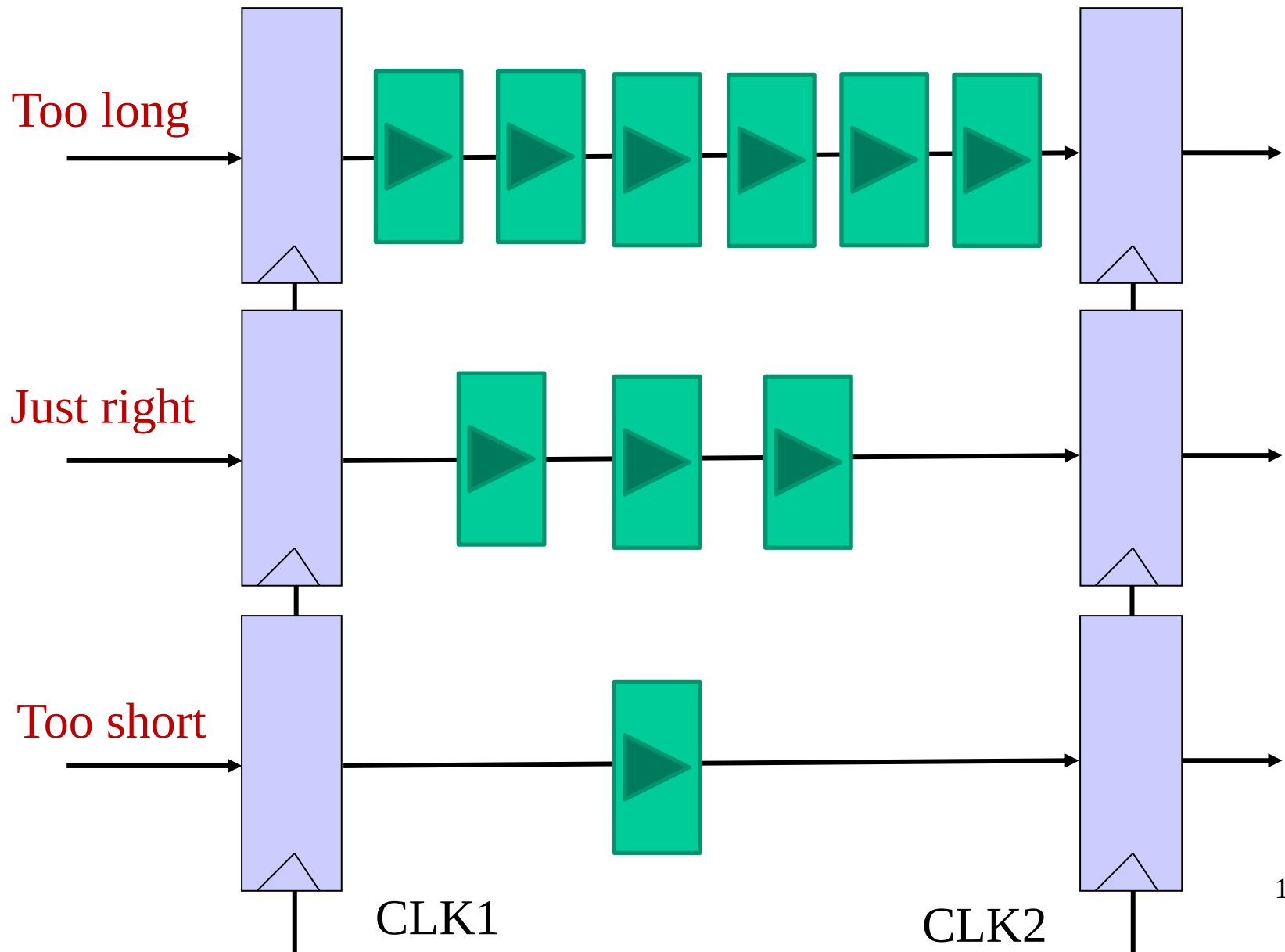
Hold time constraint Shortest delay from CLK1 to CLK2

$$t_{hold} < t_{cq} + t_{comb} \implies t_{hold} < \min(t_{cq} + t_{comb})$$

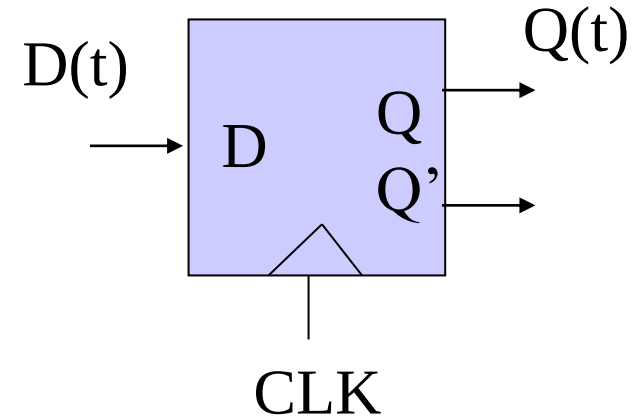
Two Timing Constraints

$$t_{cq} + t_{comb} + t_{setup} \leq T$$

$$t_{hold} < t_{cq} + t_{comb}$$



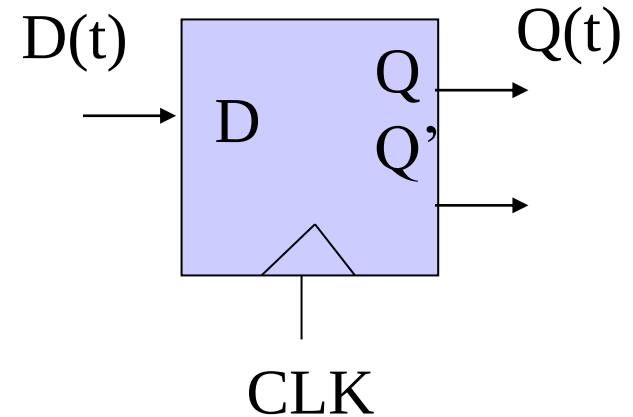
Example: The timing of which of the following signals can cause a setup-time violation?



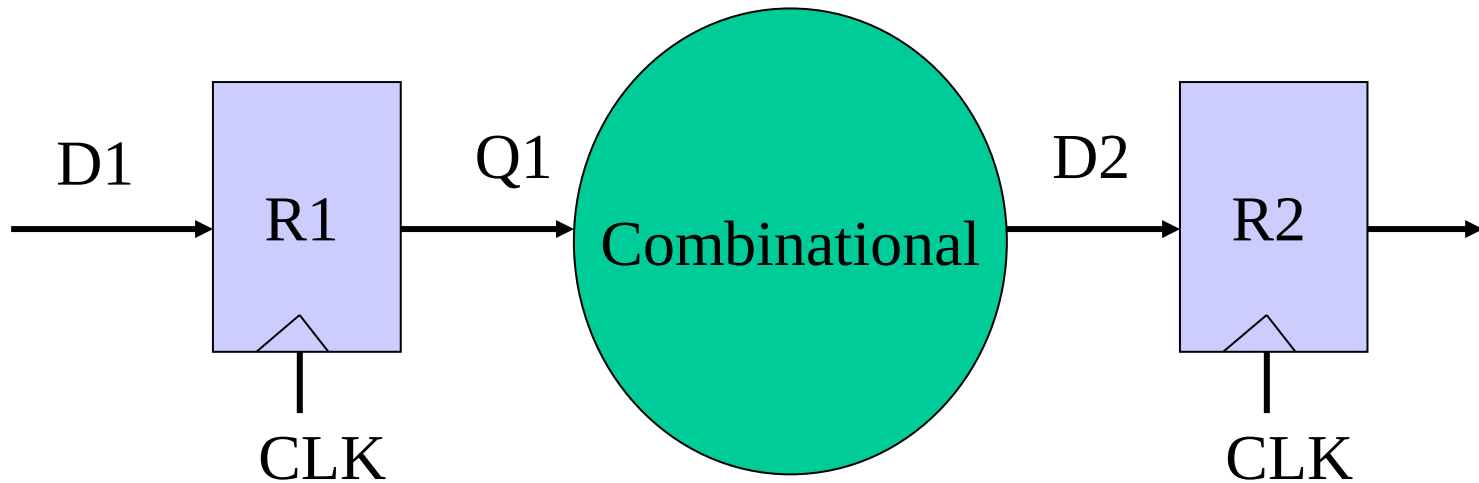
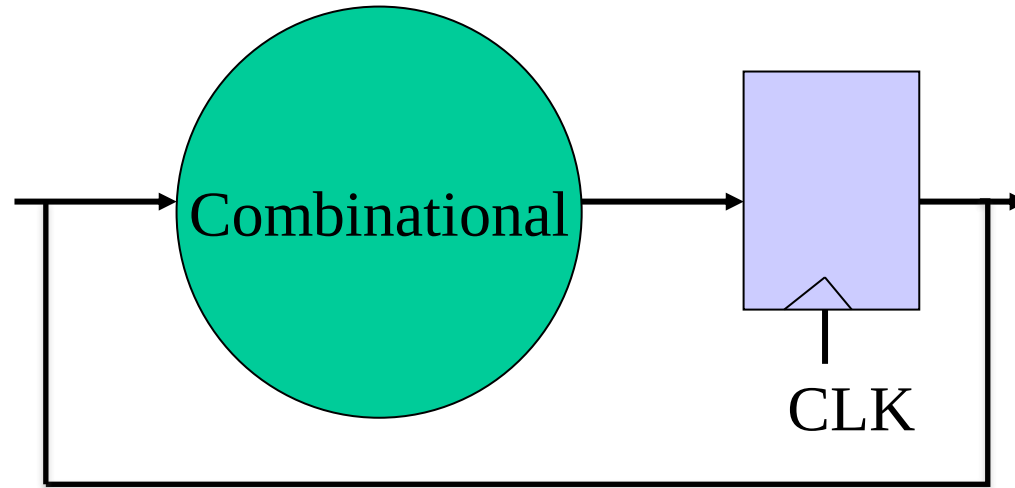
- A. Signal D arrives too early
- B. Signal D arrives too late
- C. Clock CLK arrives too late
- D. Output $Q(t)$ responds too early
- E. None of the above

Example: A hold time violation is likely to occur when

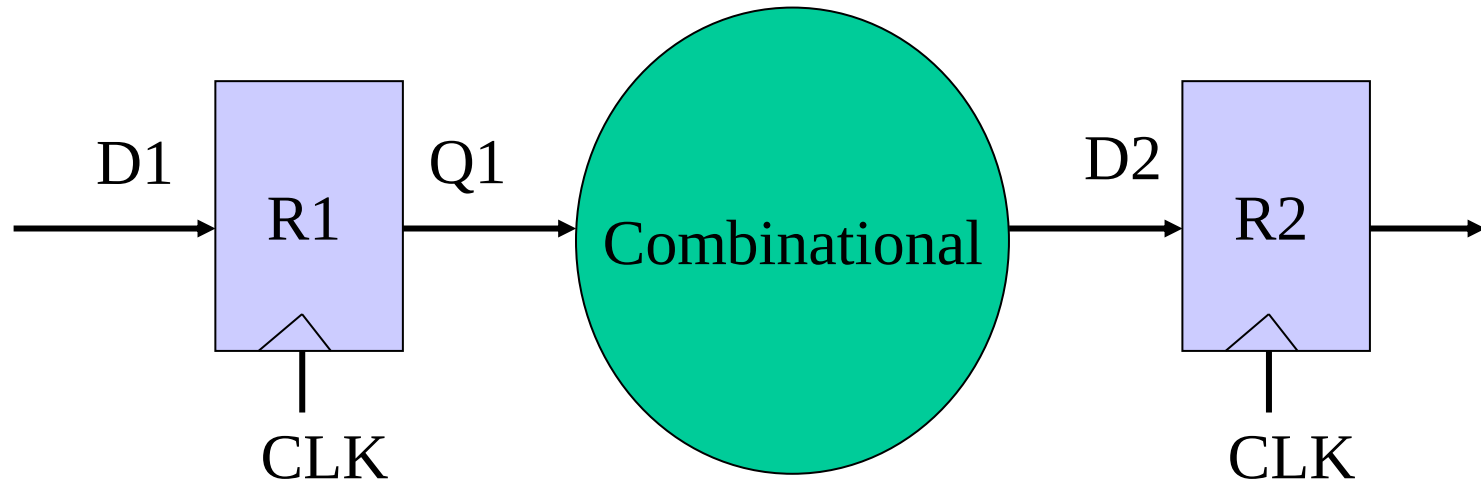
- A. Signal D changes too early
- B. Signal D changes too late
- C. Clock CLK arrives too early
- D. Clock CLK arrives too late



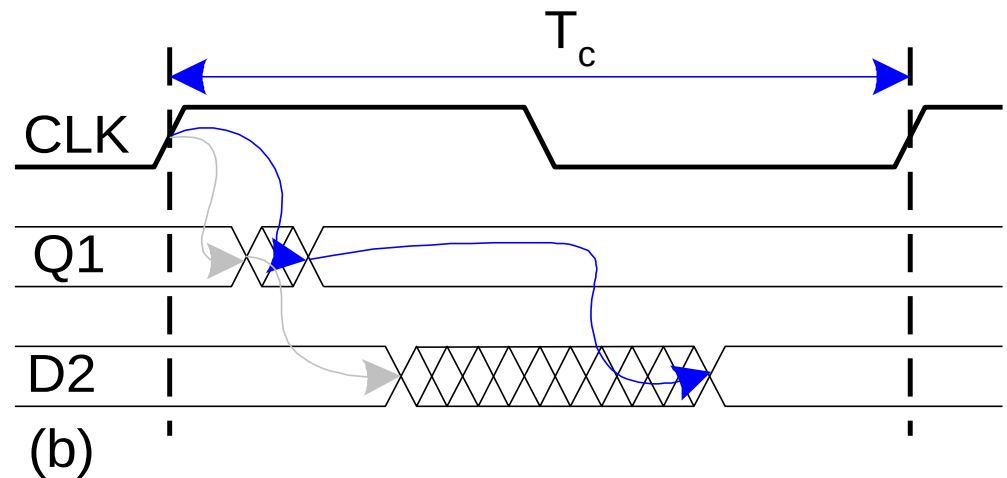
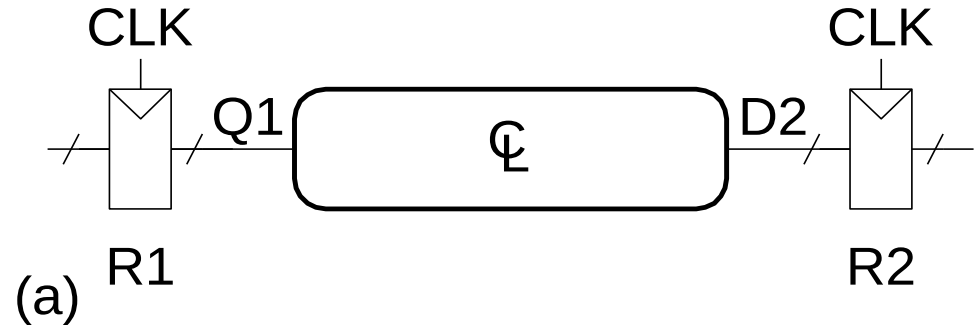
An alternate view of the sequential circuit



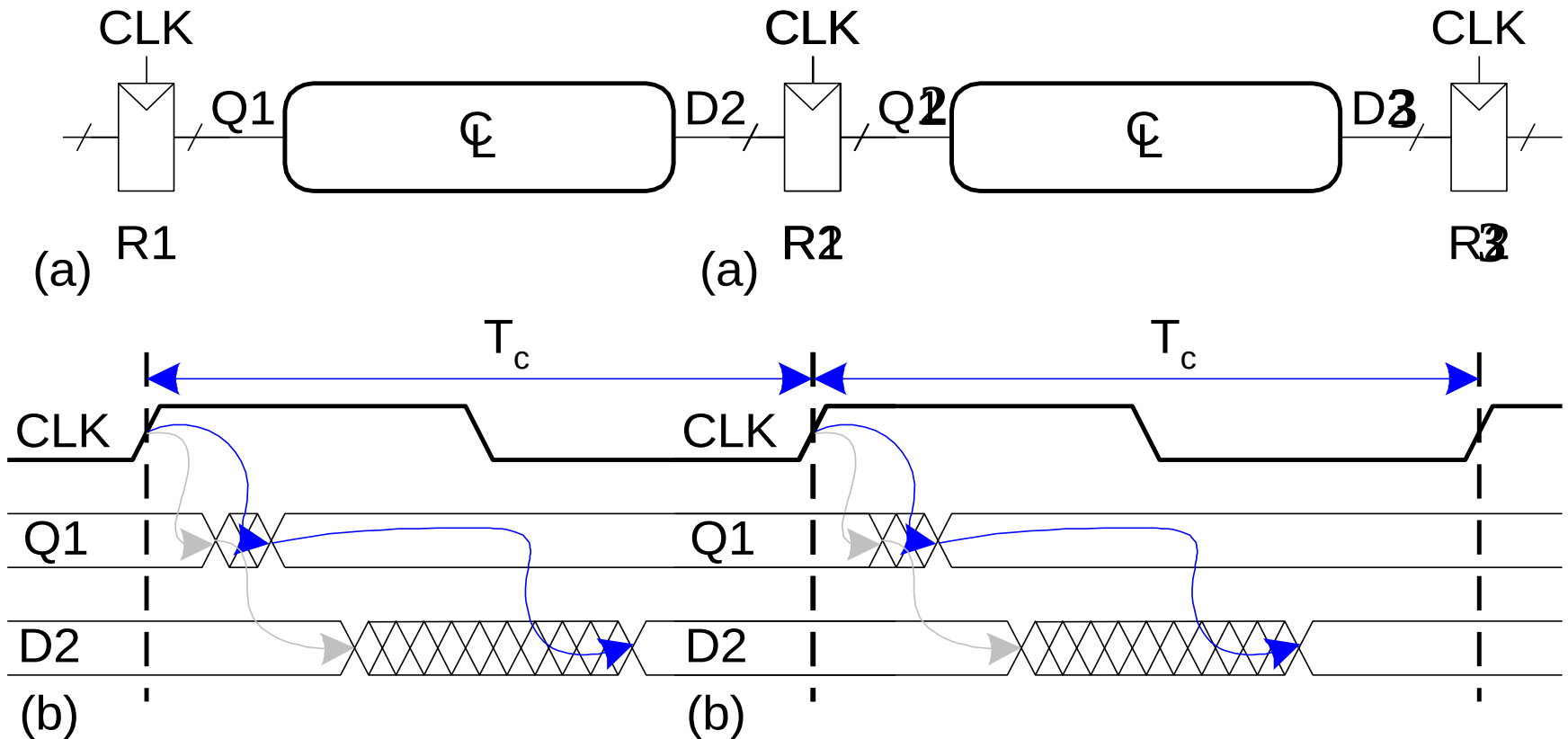
What should happen within a clock cycle for correct functionality?



The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements

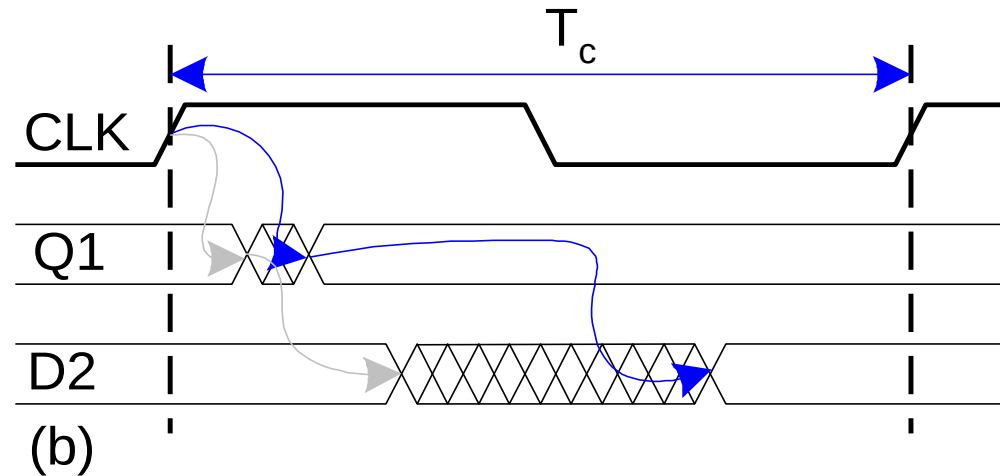
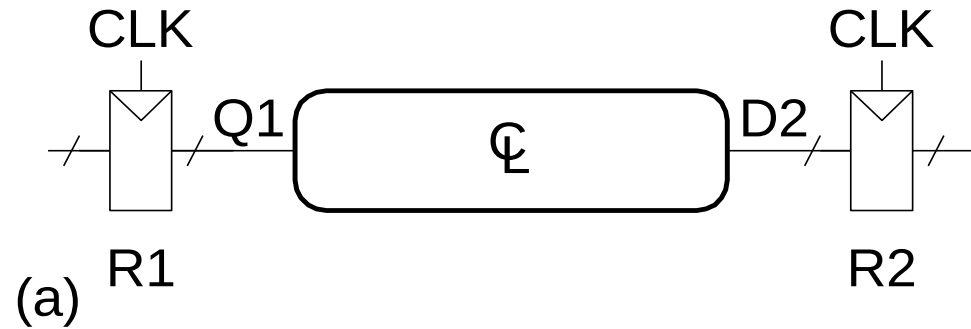


The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements



PI Q: Suppose CLK rises at t_1 , what is the maximum delay (from t_1) after which D2 reaches a stable value?

- A. Setup time of R1+
Propagation delay of CL +
Propagation delay of R2
- B. Hold time of R1+ Propagation
delay of CL + setup time of
R1
- C. Propagation delay of R1+
Propagation delay of CL +
Propagation delay of R2
- D. Propagation delay of R1+
Propagation delay of CL
- E. Propagation delay of CL +
Propagation delay of R2

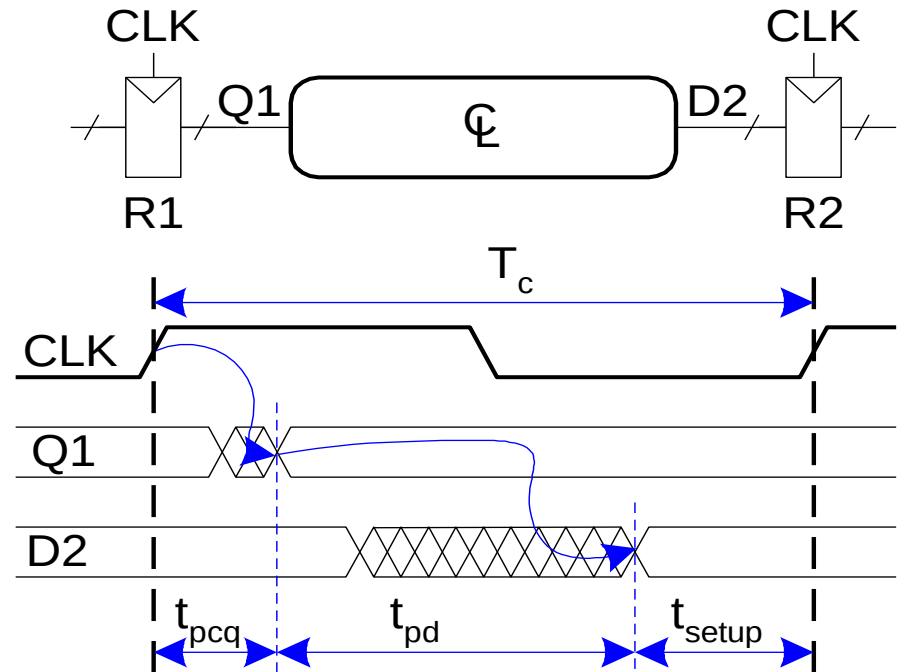


Setup Time Constraint

- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least t_{setup} before the clock edge.

Maximum delay, t_{max}
=

Setup Time Constraint:

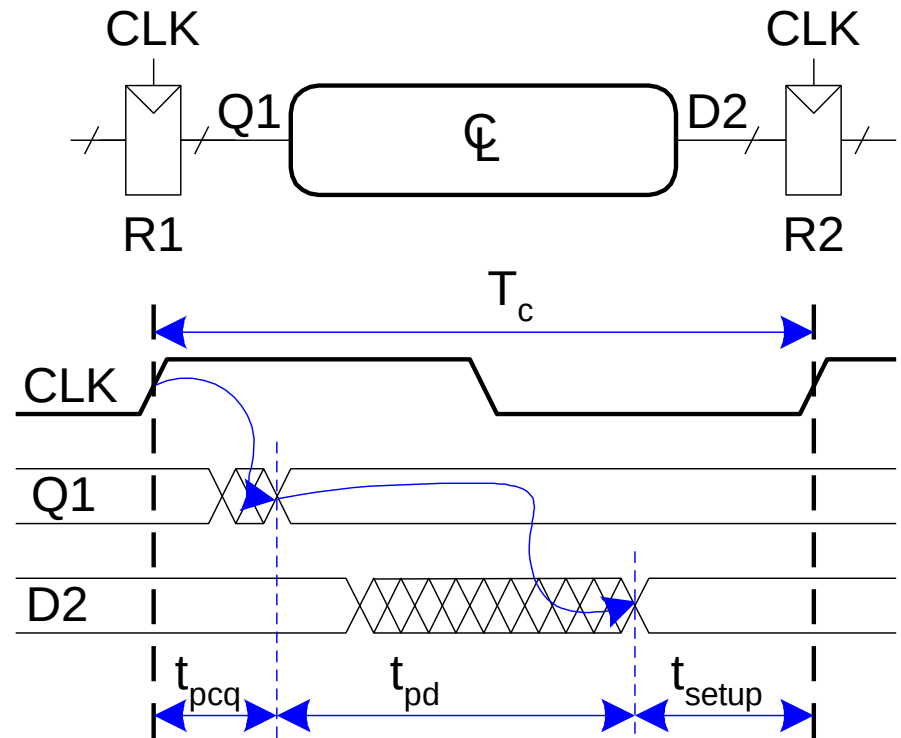


Setup Time Constraint

$$T \geq t_{pcq} + t_{pd} + t_{setup}$$

PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

- A. The clock period, T
- B. The prop. delay of R1, t_{pcq}
- C. The prop. delay of CL, t_{pd}
- D. The setup time of R2, t_{setup}
- E. All of the above



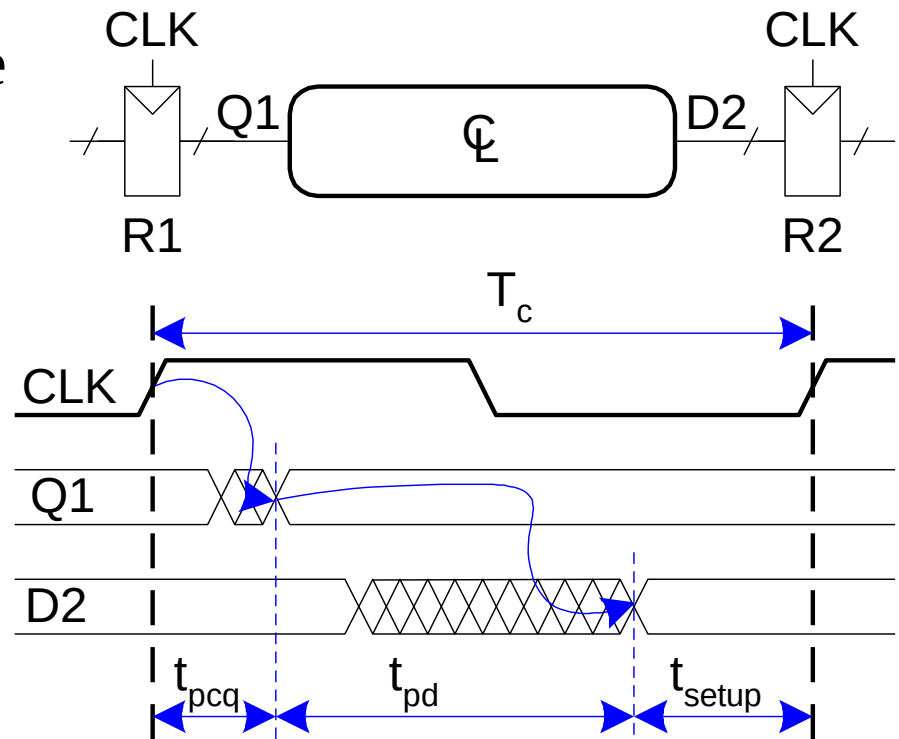
Setup Time Constraint

$$T \geq t_{pcq} + t_{pd} + t_{setup}$$

$$t_{pd} \leq T - (t_{pcq} + t_{setup})$$

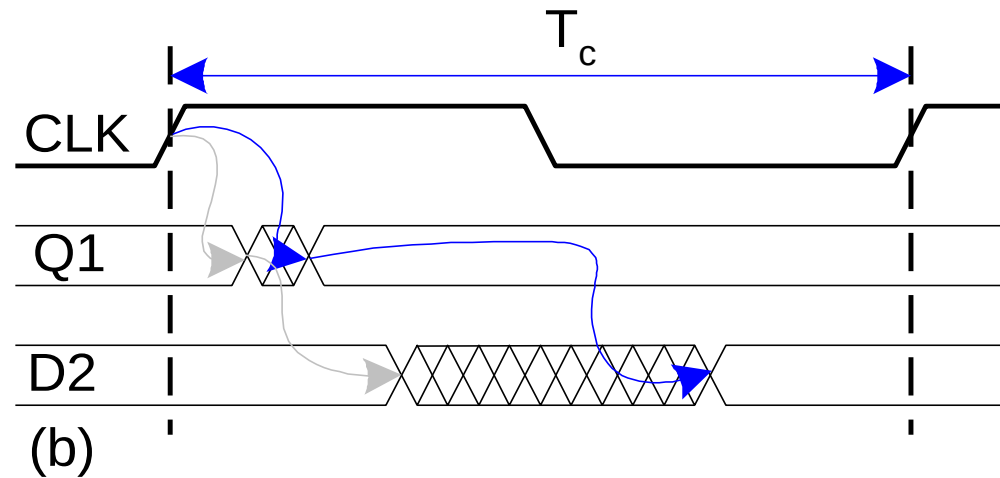
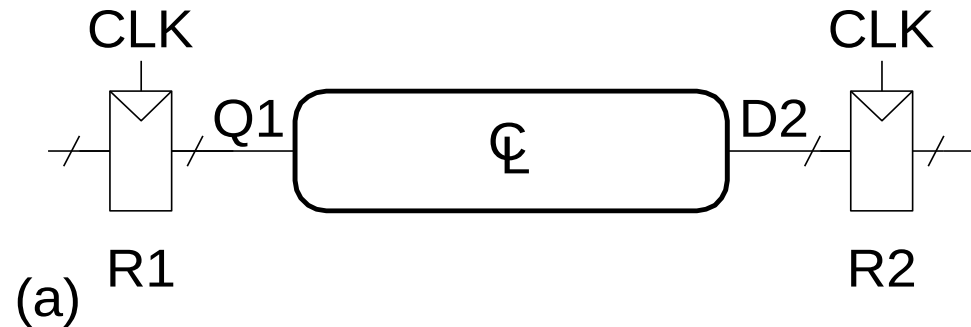
PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

- A. The clock period, T
- B. The prop. delay of R1, t_{pcq}
- C. The prop. delay of CL, t_{pd}
- D. The setup time of R2, t_{setup}
- E. All of the above



PI Q: Suppose CLK rises at t_1 , what is the minimum delay (from t_1) after which D2 starts to change?

- A. Setup time of R1+
propagation delay of CL +
propagation of R2
- B. Hold time of R1+
propagation time of CL
+setup time of R1
- C. Hold time of R1+
Contamination delay of CL
+ Propagation time of R2
- D. Contamination delay of R1+
Contamination delay of CL
- E. Contamination delay of CL
+ Contamination delay of R2



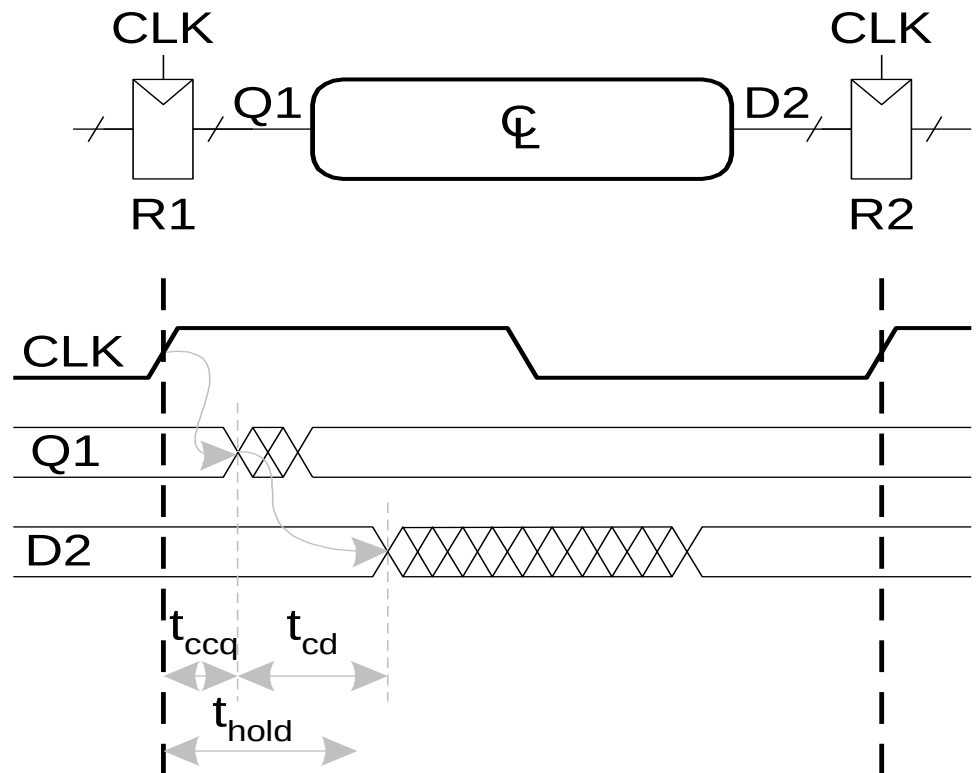
Hold Time Constraint

- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least t_{hold} after the clock edge.

Minimum delay, t_{min}

=

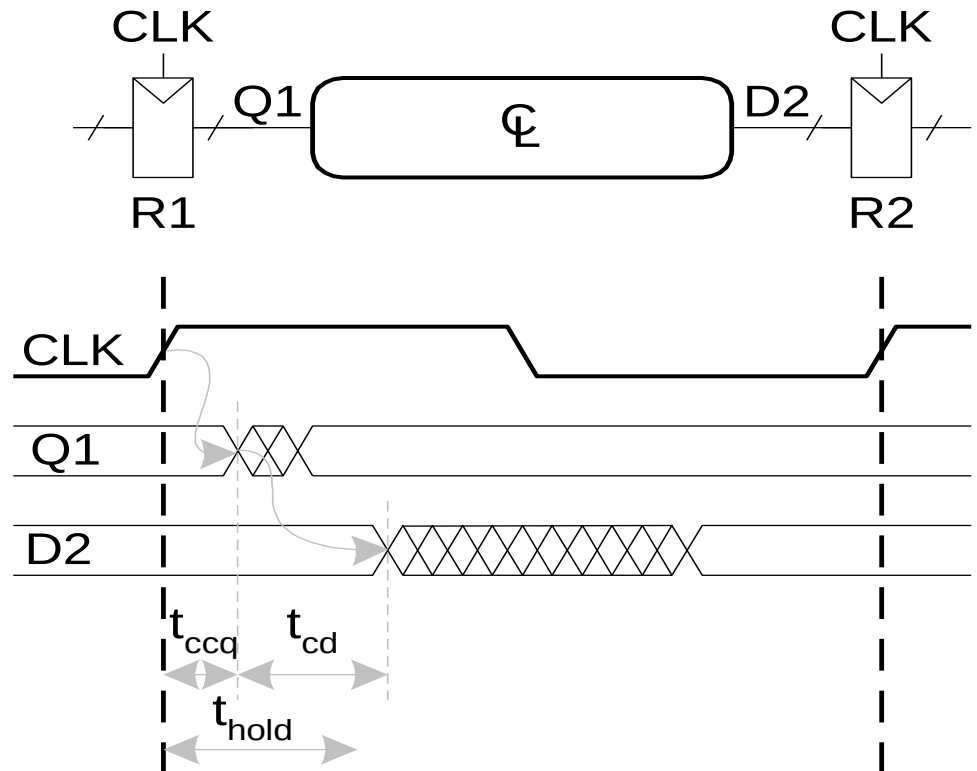
Hold Time Constraint:



Hold Time Constraint

$$t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}$$

$$t_{\text{cd}} > t_{\text{hold}} - t_{\text{ccq}}$$



Timing Analysis: Example

Timing Characteristics

$$FFs \quad t_{ccq} = 30 \text{ ps}$$

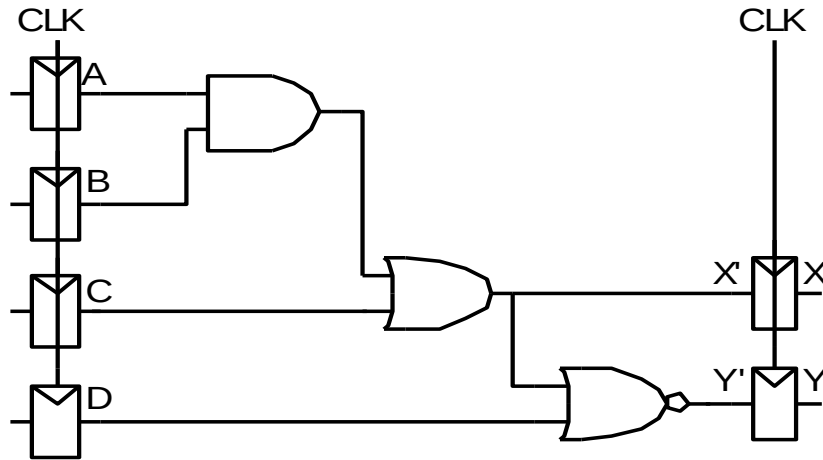
$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$\text{Gates } t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$



$$t_{pd}(\text{com}) =$$

$$t_{cd}(\text{com}) =$$

Setup time constraint:

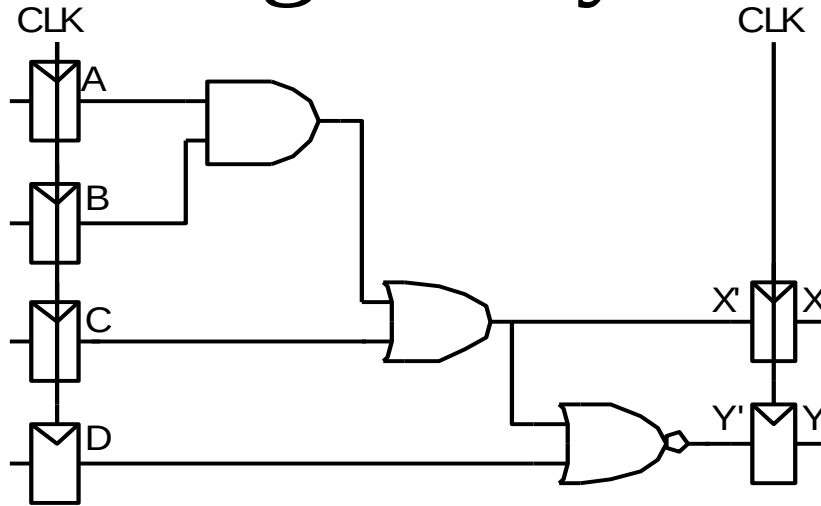
$$T_c \geq$$

$$f_c = 1/T_c =$$

Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

Timing Analysis: Example



$$t_{pd}(\text{com}) = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd}(\text{com}) = 25 \text{ ps}$$

Setup time constraint:

$$T \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}}$$

$$= 50 + 105 + 60 = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$$FFs \quad t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$Gates \quad t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

Hold time constraint:

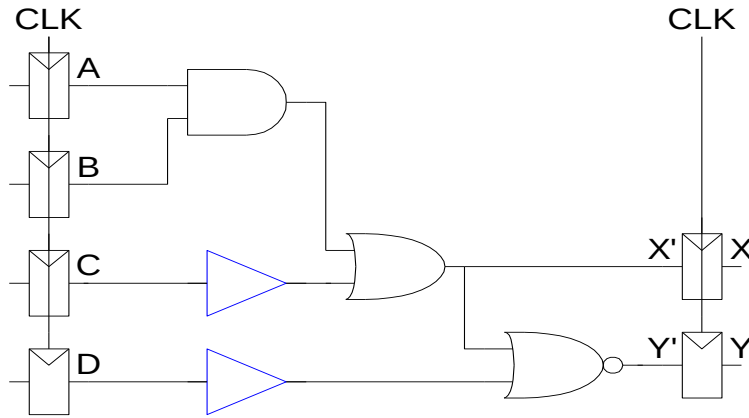
$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ?$$

No!

Example: Fix Hold Time Violation

Add buffers to the short paths:



Timing Characteristics

$$FFs \quad t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$Gates \quad t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

$$t_{pd}(\text{com}) =$$

$$t_{cd}(\text{com}) =$$

Hold time constraint:

Setup time constraint:

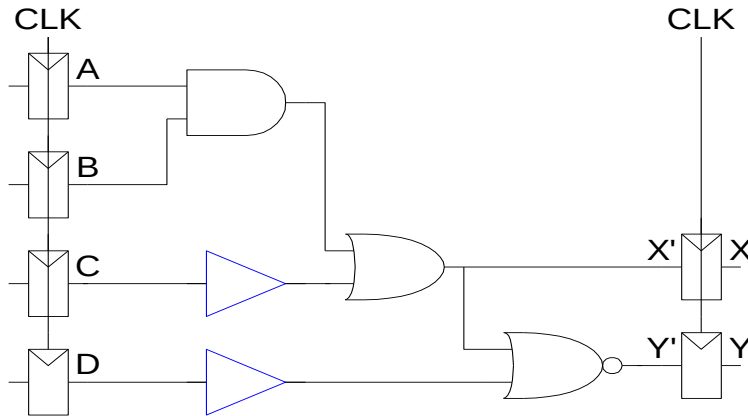
$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

$$T \geq$$

$$f_c =$$

Example: Fix Hold Time Violation

Add buffers to the short paths:



$$t_{pd}(\text{com}) = 3 \times 35 = 105 \text{ ps}$$

$$t_{cd}(\text{com}) = 2 \times 25 = 50 \text{ ps}$$

Setup time constraint:

$$T \geq 50 + 105 + 60 = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$$FFs \quad t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$Gates \quad t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

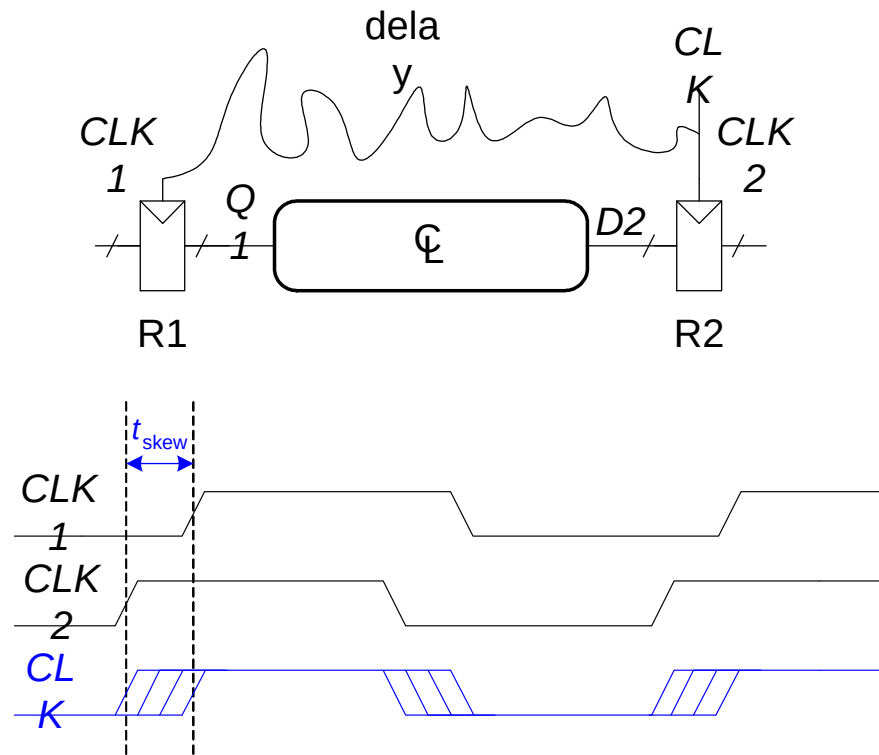
Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} ?$$

Yes!

Clock Skew



The clock doesn't arrive at all registers at the same time. The difference between two clock edges is **skew**.

- **Skew as Noise:** Caused by process variation, voltage fluctuation, crosstalks (PVC). Examine the worst case to guarantee that the timing is right.
- Designated Skew: Make skew by design to improve the performance.

Time Constraint with Clock Skew (Noise)

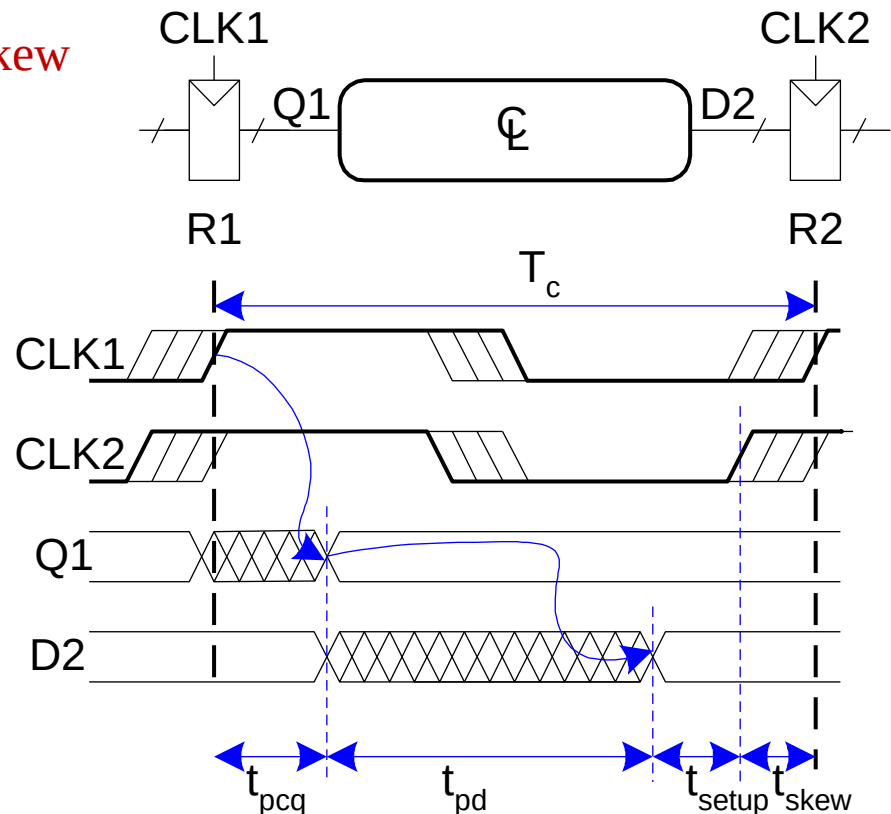
In the worst case, the CLK2 is: $t_{CLK2} = t_{CLK1} \pm t_{skew}$

• Earlier than CLK1 for setup time $t_{CLK2} = t_{CLK1} - t_{skew}$

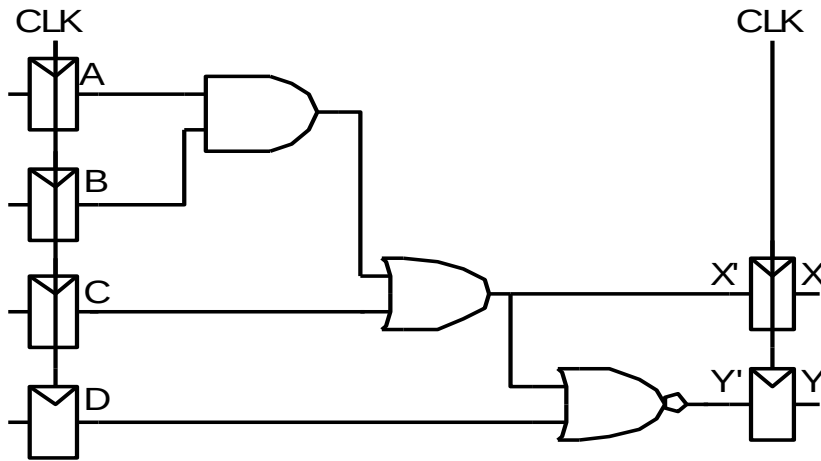
• Later than CLK1 for hold time. $t_{CLK2} = t_{CLK1} + t_{skew}$

$$T_c \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}} + t_{\text{skew}}$$

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}$$



Timing Analysis with Clock Skew: Example



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq 265 \text{ ps}$$

$$f_c = 1/T_c = 3.77 \text{ GHz}$$

Without skew we got $f_c = 4.65 \text{ GHz}$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

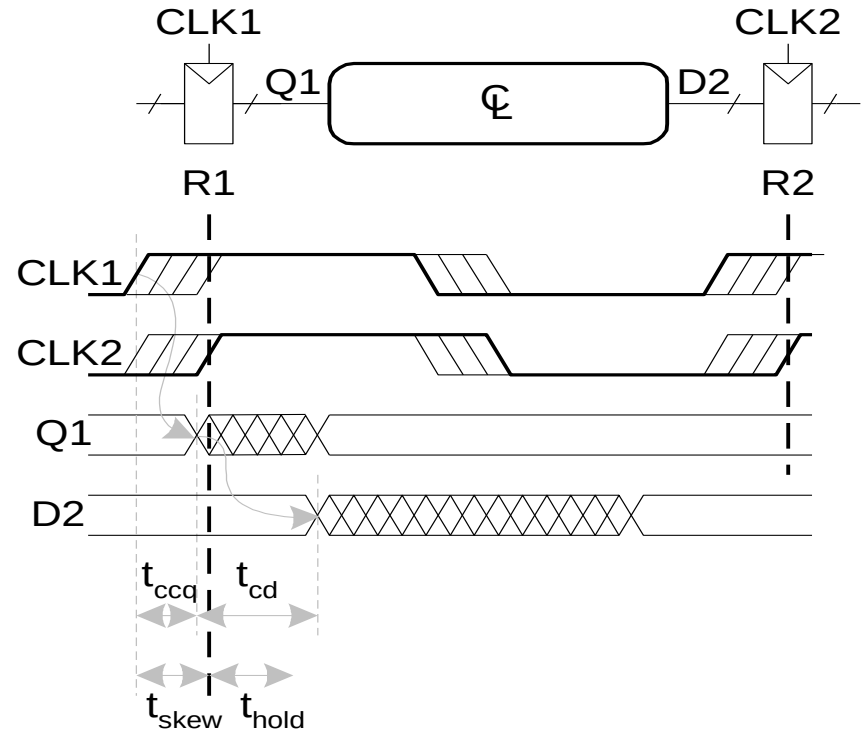
$$t_{cd} = 25 \text{ ps}$$

$$t_{\text{skew}} = 50 \text{ ps}$$

Time Constraint with Clock Skew: Example

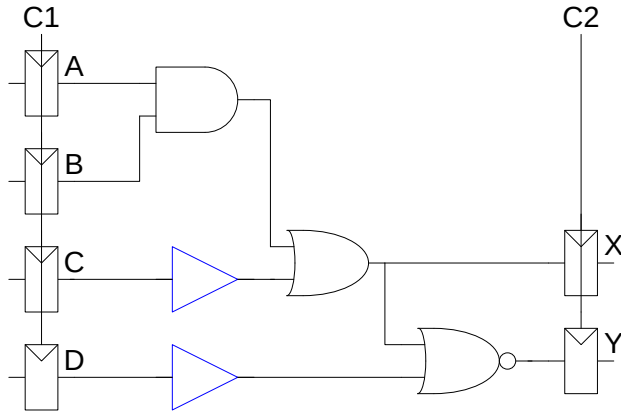
- In the worst case for setup time, CLK2 is later than CLK1

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}$$



Clock Skew: Example

Add buffers to the short paths:



$$t_{pd}(\text{com}) = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd}(\text{com}) = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}?$$

$$(30 + 50) > (70 + 50) \text{ ps} ?$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

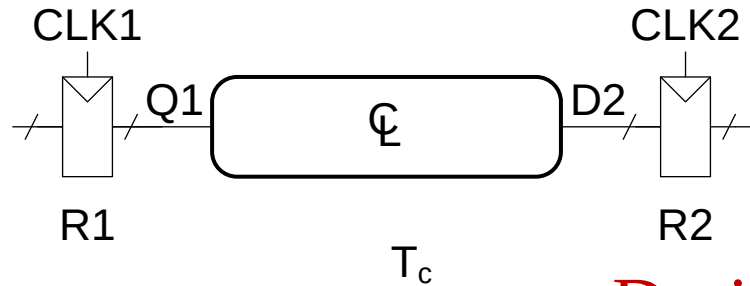
$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd}(\text{g}) = 35 \text{ ps}$$

$$t_{cd}(\text{g}) = 25 \text{ ps}$$

$$t_{\text{skew}} = 50 \text{ ps}$$

Retiming with Designated Skew



Skew as noise (worst case)

Designated skew

$$t_{CLK2} = t_{CLK1} \pm t_{skew}$$

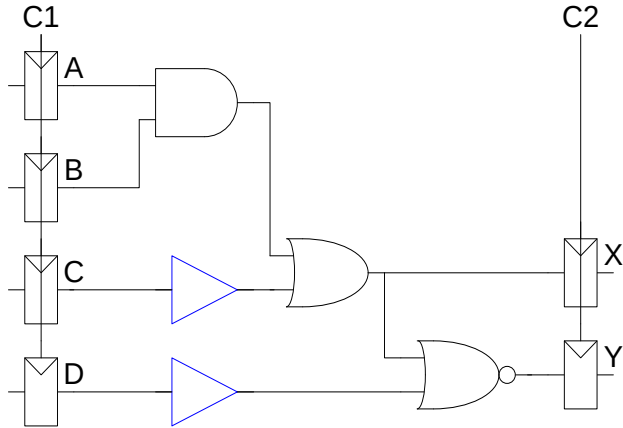
$$t_{CLK2} = t_{CLK1} + t_{skew}$$

$$T \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}} + t_{\text{skew}} \quad T \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}} - t_{\text{skew}}$$

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}$$

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}$$

Retiming: Example



$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

$$T_c \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}} - t_{\text{skew}}$$

$$t_{ccq} + t_{cd}(\text{com}) \geq t_{\text{hold}} + t_{\text{skew}}$$

$$T_c \geq 50 + 105 + 60 - t_{\text{skew}}$$

$$30 + 50 \geq 70 + t_{\text{skew}}$$

Example: The minimum clock period T can be:

A. 195

B. 205

C. 215

D. None of the above

Timing and Retiming

- Retiming: Adjust the clock skew so that the clock period can be reduced.
- Add a few more examples on timing and retiming.

Conclusion

- Clock to Clock: Range of shortest and longest paths
- Design revision and retiming to adjust the constraints
- Research: Variation aware designs

Extra materials:

- C. Leiserson and J. Saxe, "Retiming Synchronous Circuitry," *Algorithmica*, pp. 6:5-35, 1991.
- L.T. Liu, M. Shih, N.C. Chou, C.K. Cheng, and W. Ku, "Performance-Driven Partitioning Using Retiming and Replication," *IEEE Int. Conf. on Computer-Aided Design*, pp. 296-299, Nov. 1993.