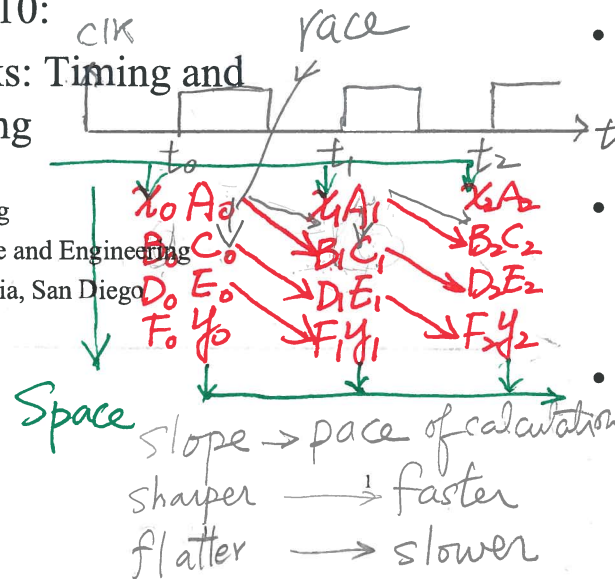
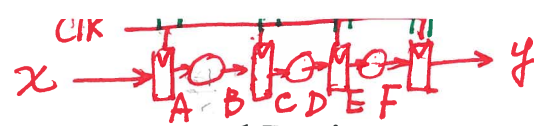


Lecture 10:

Sequential Networks: Timing and Retiming

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Timing

- Motivation
- Basic Timing Characteristic
 - Gate Delay, Interconnect Delay
 - Flip-Flop Timing Window
- Two Timing Constraints: shortest and longest timing paths
 - Examples
- Clock Skews and Retiming
 - Examples

Timing: Motivation

- Clock specifies a precise time for the next state
 - In general, we allocate one clock period for signal propagation between registers. **Goldilocks** timing.
- Too late: Fail to reach for the **setup** of the next state.
- Too early: Race to disturb the **holding** of the next state.
- Analysis: Verify the timing of the system.
- Goal: A robust design.

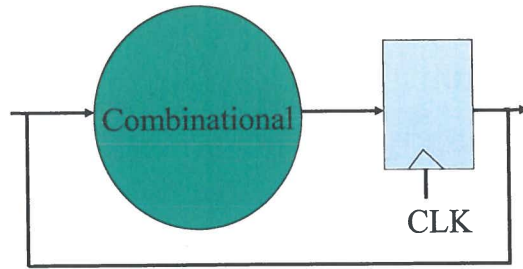
The Story of Goldilocks and the Three Bears

Once upon a time, there was a little girl named **Goldilocks**. She went for a walk in the forest. Pretty soon, she came upon a house. She knocked and, when no one answered, she walked right in. At the table in the kitchen, there were three bowls of porridge. Goldilocks was hungry. She tasted the porridge from the first bowl. "This porridge is **too hot**!" she exclaimed. So, she tasted the porridge from the second bowl. "This porridge is **too cold**," she said. So, she tasted the last bowl of porridge. "Ahhh, this porridge is **just right**," she said happily and she ate it all up.

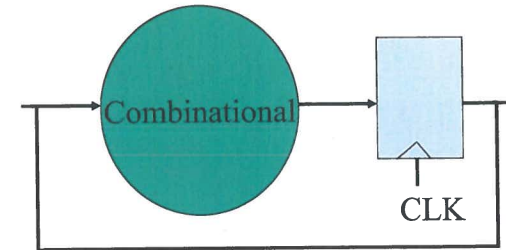
DLTK's Crafts for Kids



Motivation: So far

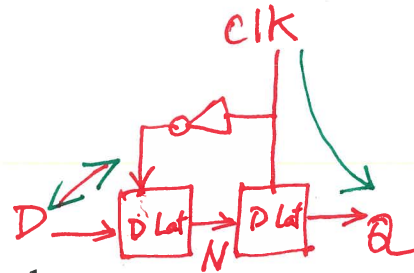


Motivation: This lecture ...

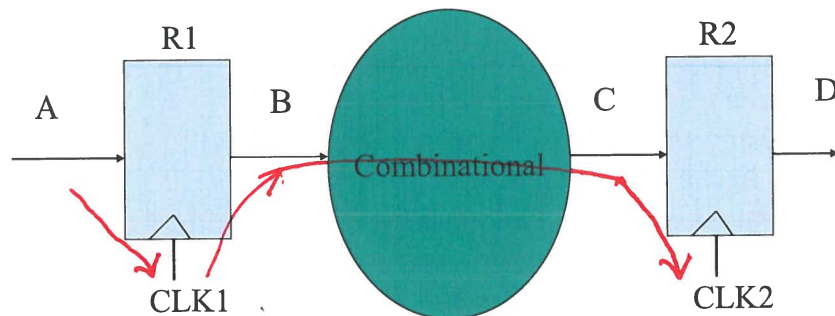


- When does our (seemingly logically correct) design go wrong?
- How can we design a circuit that works under real constraints?
- Popular interview questions.

Logic-level analysis



Motivation: Sequential Networks



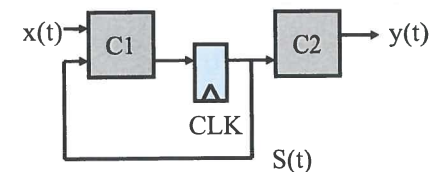
A typical sequential network has combinational circuit between registers (R1 to R2).

The registers are synchronized by clocks (CLK1 and CLK2).

Timing is set between clocks (CLK1 and CLK2).

The beauty of the synchronized design is that we need only to take care of the timing of the regions separated by the registers.

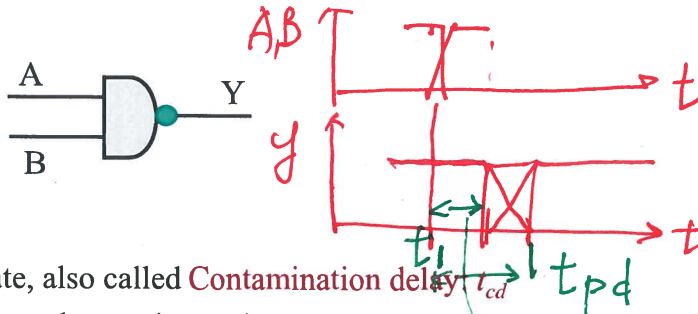
Timing of the System



For a synchronized digital Moore machine, we take care of the timing of the following three groups of paths between:

- Every pair of registers,
- Each input and register, and
- Each register and output.

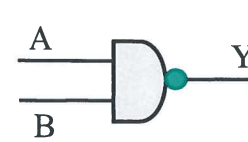
Basic Timing Characteristics: Gate Delay



- I. Min delay of a gate, also called **Contamination delay**: t_{cd}
Minimum time from when an input changes until the output *starts* to change
- II. Max delay of a gate, also called **Propagation delay**: t_{pd}
Maximum time from when an input changes until the output *is* guaranteed to reach its final value (i.e., stop changing)

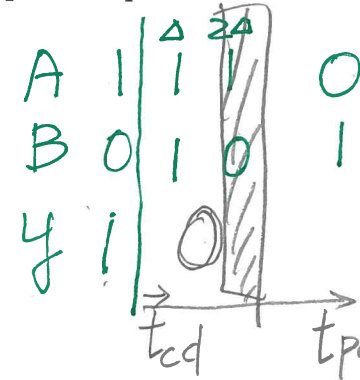
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Gate Delay: Combinational Logic Timing



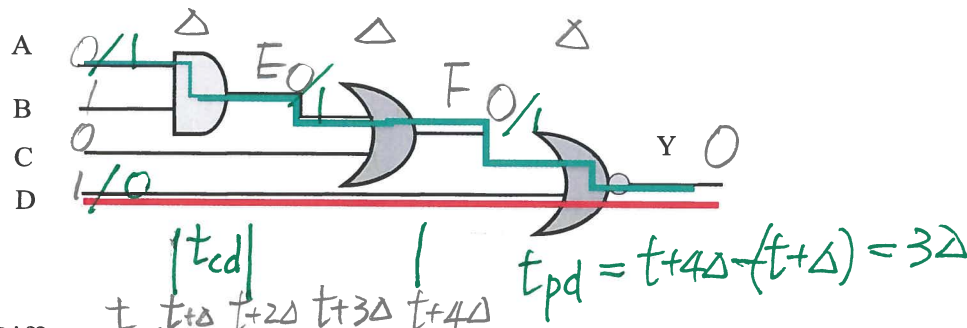
$A_t B_t$	$A_{t+1} B_{t+1}$	$Y = (AB)'$
00	11	1 $\Rightarrow$ 0
01	11	1 $\Rightarrow$ 0
10	11	1 $\Rightarrow$ 0
11	11	0 $\Rightarrow$ 0

Different situation causes different delay at output, e.g. input patterns, process variations, noises, temperature, aging

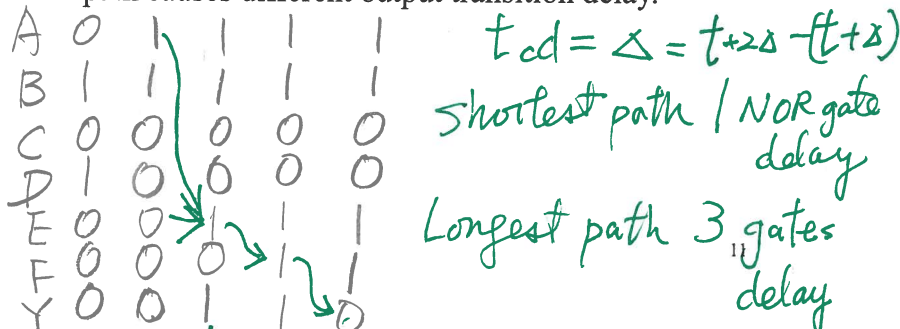


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Combinational Logic Delay



Different path causes different output transition delay.



Interconnect Delay



Speed of light: $C/\sqrt{\epsilon} \approx 1.5 \times 10^{10}$ cm/s

For 1cm, it takes 0.7×10^{-10} s = 70ps (picosecond)

for the light to reach from one end to the other end.

Chain of buffers: 5-40 times of speed of light.

For 5GHz, the clock period is 200ps/cycle.

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Combinational Logic: Output timing constraints



I. Contamination delay (shortest): t_{cd}

Minimum time from when an input changes until any output *starts* to change

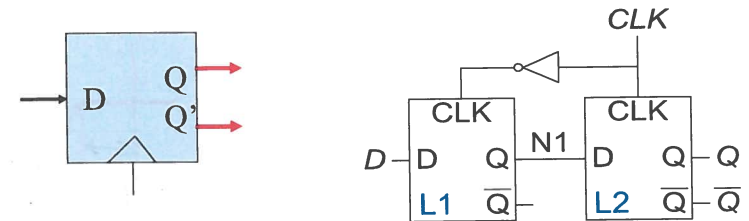
II. Propagation delay (longest): t_{pd}

Maximum time from when an input changes until the output *or* outputs of a combinational circuit are guaranteed to reach their final value (i.e., stop changing)

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Flip-Flop Timing Window

Timing: Setup Time and Hold Time Constraints



Once a flip flop has been 'built' we are stuck with its timing characteristics:

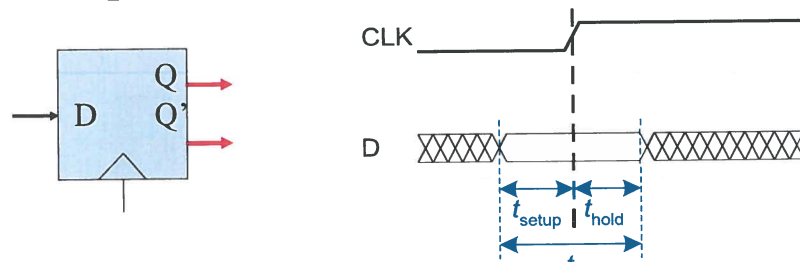
t_{setup} , t_{hold} timing relation between D and CLK

t_{ccq} , t_{pcq} timing relation between CLK and Q

No direct timing relation between input D and output Q

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FF Input Constraints: Set up and hold time



Setup time t_{setup} Time *before* the clock edge that data must be stable (i.e. no change)

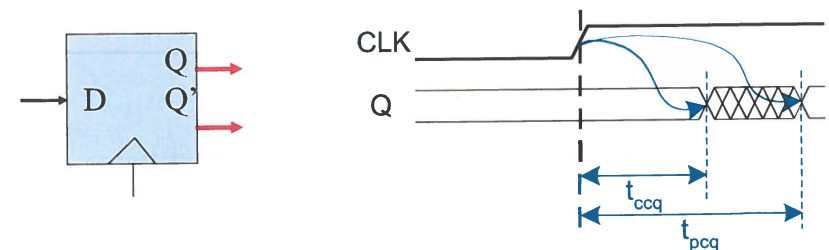
Setup time violation This occurs if the input signal D does not settle (**set up**) to the stable value at least t_{setup} *before* the clock edge.

Hold time t_{hold} Time *after* the clock edge that data must be stable

Hold time violation This occurs if the input signal D does not remain unchanged (**hold**) for at least t_{hold} *after* the clock edge.

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FF Output Timing Constraints



- Propagation delay: t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- Contamination delay: t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)

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