

1 Memory Devices

Use a table to list and compare the number of transistors per memory bit, number of memory bits per data net, and access time of five different memory devices (hint: feel free to search available references).

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Note:

1. This question is fairly open ended and credits will be given to any answer that touches upon the above concepts.

2. Data net simply refers to the data bus

Here is one type of solution that will be given full credit

Flip flop takes about 20 transistors and dedicated interconnect

Register is an array of flip flops that shares the data bus

SRAM takes about 6 transistors per cell and heavily shares the data bus

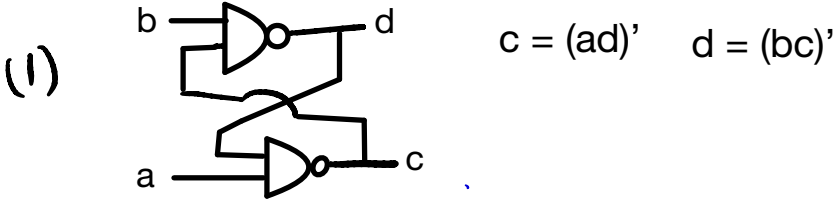
DRAM is one transistor per cell

FLASH also takes one transistor per cell

2 Latch

(1). Given a SR latch of NOR gates, replace the two NOR gates with two NAND gates. Write the state table, state diagram and the characteristic expression of the revised circuit.

(2). Given a SR latch of NOR gates, replace the two NOR gates with two XOR gates. Write the state table and state diagram of the revised circuit. Analyze the behavior of the circuit.



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id	b	a	c	d	c	d	c	d	c	d
0	0	0	0	0	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1
2	0	0	1	0	1	1	1	1	1	1
3	0	0	1	1	1	1	1	1	1	1
4	0	1	0	0	1	1	0	1	0	1
5	0	1	0	1	0	1	0	1	0	1
6	0	1	1	0	1	1	0	1	0	1
7	0	1	1	1	0	1	0	1	0	1
8	1	0	0	0	1	1	1	0	1	0
9	1	0	0	1	1	1	1	0	1	0
10	1	0	1	0	1	0	1	0	1	0
11	1	0	1	1	1	0	1	0	1	0
12	1	1	0	0	1	1	0	0	1	1
13	1	1	0	1	0	1	0	1	0	1
14	1	1	1	0	1	0	1	0	1	0
15	1	1	1	1	0	0	1	1	0	0

From the incremental steps we

obtain :

State table for cd:

ab \ cd	00	01	10	11
00	11	10	01	11
01	11	10	01	01
10	11	10	01	10
11	11	10	01	00

Avoiding $ab=00$, obtain

c \ ab	00	01	11	10
0	x	1	0	0
1	x	1	1	0

$$\Rightarrow c = \bar{a} + bQ(t)$$

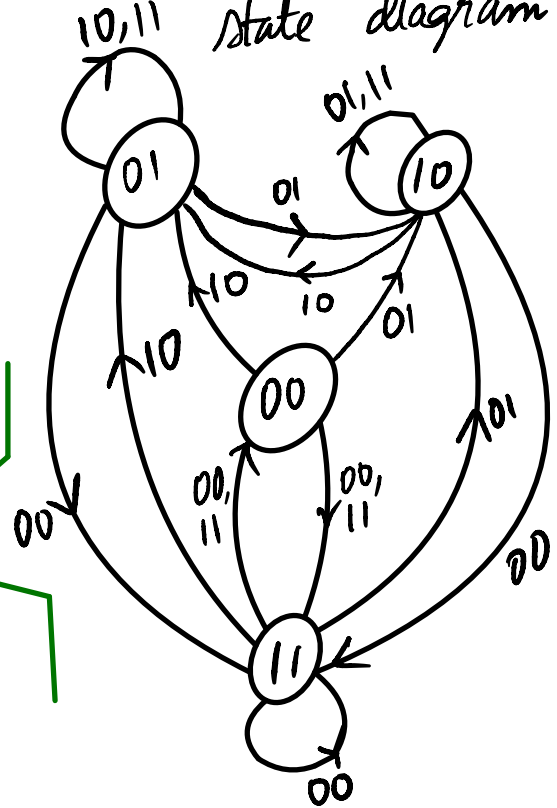
We may thus map in the following manner to recover the behavior of the SR latch:

$a - \bar{S}$
 $b - R$
 $c - Q$

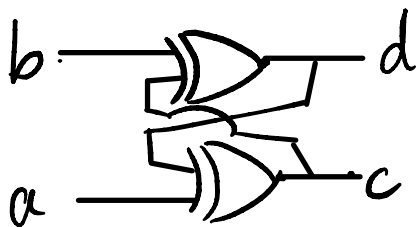
to give

$$Q(t+1) = S + \bar{R} Q(t)$$

State diagram :



(2)



$$c = a \oplus d$$

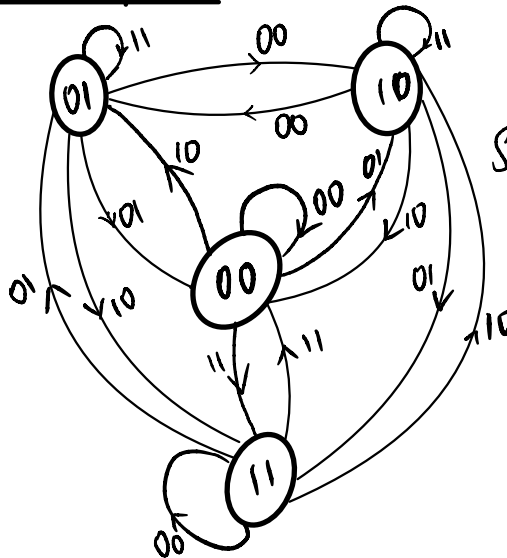
$$d = b \oplus c$$

id	b	a	c	d	c	d	c	d	c	d
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	1	1	0
2	0	0	1	0	0	1	1	0	0	1
3	0	0	1	1	1	1	1	1	1	1
4	0	1	0	0	1	0	1	1	0	1
5	0	1	0	1	0	0	1	0	1	1
6	0	1	1	0	1	1	0	1	0	0
7	0	1	1	1	0	1	0	0	1	0
8	1	0	0	0	0	1	1	1	1	0
9	1	0	0	1	1	1	1	0	0	0
10	1	0	1	0	0	0	0	1	1	1
11	1	0	1	1	1	0	0	0	0	1
12	1	1	0	0	1	1	0	0	1	1
13	1	1	0	1	0	1	0	1	0	1
14	1	1	1	0	1	0	1	0	1	0
15	1	1	1	1	0	0	1	1	0	0

State table for cd

cd \ ab	00	01	10	11
00	00	10	01	11
01	10	00	11	01
10	01	11	00	10
11	11	01	10	00

In the figure the state/input combinations that stabilise are given in black



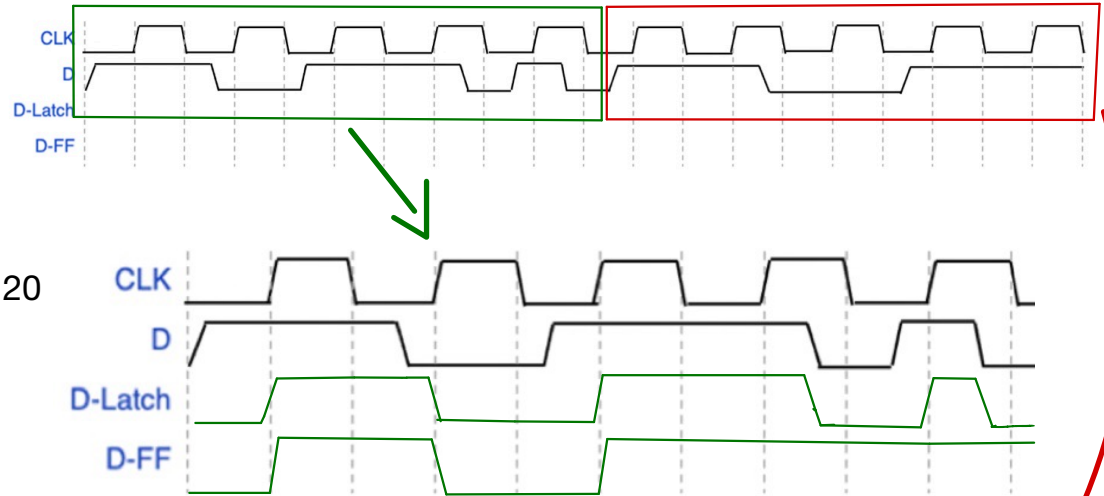
State diagram

As it can be seen above except for the state/input combinations:
00/00; 01/11; 10/11; 11/00

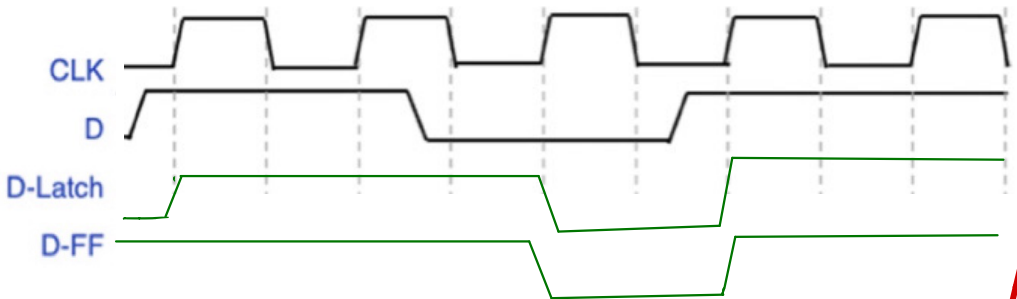
the XOR based latch does not reach a steady state. Thus it cannot be used as an SR latch

3 Timing Diagram of Latch and Flip-Flop

Timing Diagram of Latch and Flip-Flop: Given the input waveforms shown below, sketch the output D-Latch of the latch and the output D-FF of the flip-flop.



Rubric: grade based on each rising edge (2 per each)



For the latter D-latch, the following is also acceptable

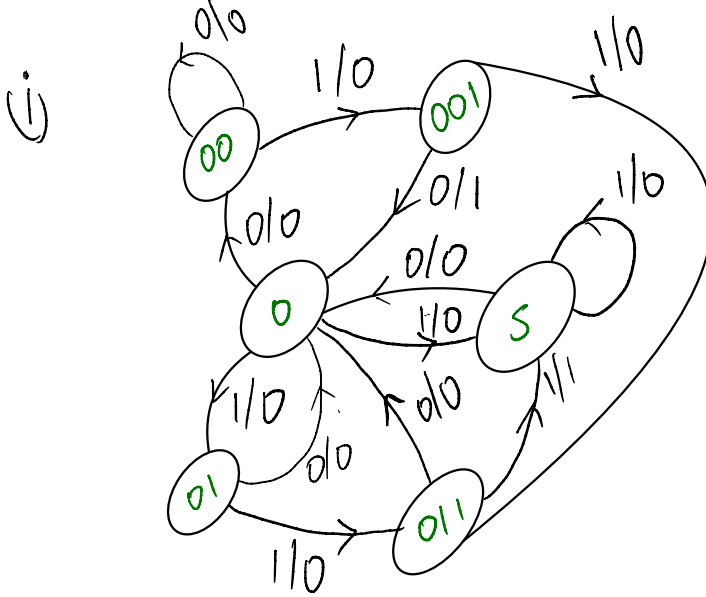


4 Pattern Recognizer

A sequential network has one binary input $x(t)$ and one binary output $y(t)$. The network produces $y = 1$, whenever input pattern $x(t-3, t) = 0010$ or 0111 . Otherwise, the output $y = 0$.

(i) Draw the state diagram.

(ii) Write the state table.



Identifies 0010 via
 $S \rightarrow 0 \rightarrow 00 \rightarrow 001 \rightarrow 0$

Identifies 0111 via
 $S \rightarrow 0 \rightarrow 01 \rightarrow 011 \rightarrow S$

ii)

Current State	Next State		Output	
	$x(t)=0$	$x(t)=1$	$x(t)=0$	$x(t)=1$
S	0	S	0	0
0	00	01	0	0
00	00	001	0	0
001	0	011	1	0
01	0	011	0	0
011	0	S	0	1

5 Sequential Circuit Analysis

Given a state machine has one input $x(t)$ and two-bit state $(Q_1(t), Q_0(t))$. The machine is described by the following state equations.

$$Q_1(t+1) = x(t)Q_0'(t) + Q_1(t),$$

$$Q_0(t+1) = x(t)Q_1'(t)Q_0(t) + x'(t)Q_1(t).$$

Use two D flip-flops and a minimal sum-of-products network to implement the machine.

(i). Write the state table of the system.

(ii). Describe the design using a logic diagram. Show your derivation using K maps.

(i)

Current state $Q_1 Q_0$	Next state $Q_1 Q_0$	
	$x(t)=0$	$x(t)=1$
00	00	10
01	00	01
10	11	10
11	11	10

Kmap for $Q_1(t+1)$

(ii)

		$Q_1(t)Q_0(t)$			
		00	01	11	10
$x(t)$	0	0	0	1	1
	1	1	0	1	1

$$Q_1(t+1) = Q_1(t) + x(t) \overline{Q_0}(t)$$

Kmap for $Q_0(t+1)$

		$Q_1(t)Q_0(t)$			
		00	01	11	10
$x(t)$	0	0	0	1	1
	1	0	1	0	0

$$Q_0(t+1) = \overline{x(t)}Q_1(t) + x(t)\overline{Q_1}(t)Q_0(t)$$

are the minimal SOP expressions

Implementation with D flip flops

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