

This is a take-home exam. You are allowed to check books, notes, and conduct an internet search. However, you are expected to work on the solution by yourself. No discussion with anyone else is allowed.

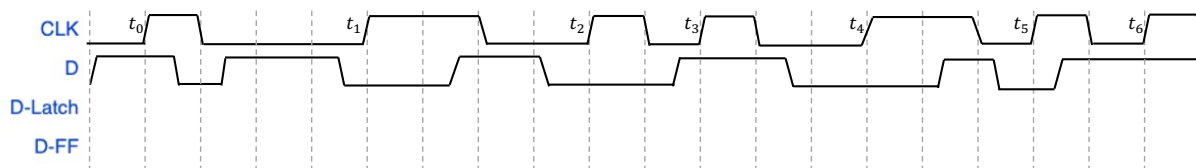
There are two parts to the exam. Part A weighs 90 points. Part B weighs 10 points. However, in Part B, the total weight of the problems is higher than 10 points. You are encouraged to earn up to 10 points. In other words, there is no penalty on wrong solutions in Part B, but the maximum points to earn are limited to 10 points.

Please read the following instructions carefully. If you are unclear about any of the questions on the exam, make the most plausible assumption to answer the question. Instructors and proctors will not answer questions on the exam material. **All the Best!**

Part A: (90 pts)

1 Timing Diagram of Latch and Flip-Flop

Given the input waveforms shown below, sketch the output D-Latch of the latch and the output D-FF of the flip-flop. Label your drawing at the time points of the rising edges of the clock as shown in the figure. (20 pts)



2 Finite State Machine

A pattern recognizer inputs a string of binary bits $x(t)$ and outputs $y(t) = 1$ whenever $x(t-3, t) = 1011$ or 1010 ; $y(t) = 0$ otherwise. (30 pts)

1. Draw the state diagram for the state machine using a minimal number of states.
2. Write the state table for a state machine using 2 D Flip Flops.
3. Describe $y(t), D_1(t), D_0(t)$ as functions of variables $(x, Q_1(t), Q_0(t))$ in minimal sum-of-products expressions. No need to draw the logic diagram.

3 Mealy and Moore Machine Conversion

Given a state table as below, each entry of the table is the next state and output. (20 pts)

id	$Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	S0	S0,0	S1,1
1	S1	S0,1	S3,0
2	S2	S1,0	S3,1
3	S3	S2,0	S4,1
4	S4	S2,1	S3,0

1. Fill the following table as the machine starts at state S0 and process through the given input x from CLK (Clock) sequence =1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

2. Convert the above machine into a Moore machine. Write the state table.

3. Use the Moore machine to fill the table starting at state $S0$ and process through the given input x from CLK (Clock) sequence 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

4 Timing and Retiming

For the following circuit (figure 4, the timing characteristics of the components are summarized below.(20 pts)

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 20\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 15\text{ps}$, setup time $t_{setup} = 10\text{ps}$, hold time $t_{hold} = 20\text{ps}$
- Logic gate (e.g. Buffer, AND, OR, XOR, etc): propagation delay $t_{pd}(\text{gate}) = 15\text{ps}$, contamination delay $t_{cd}(\text{gate}) = 10\text{ps}$.

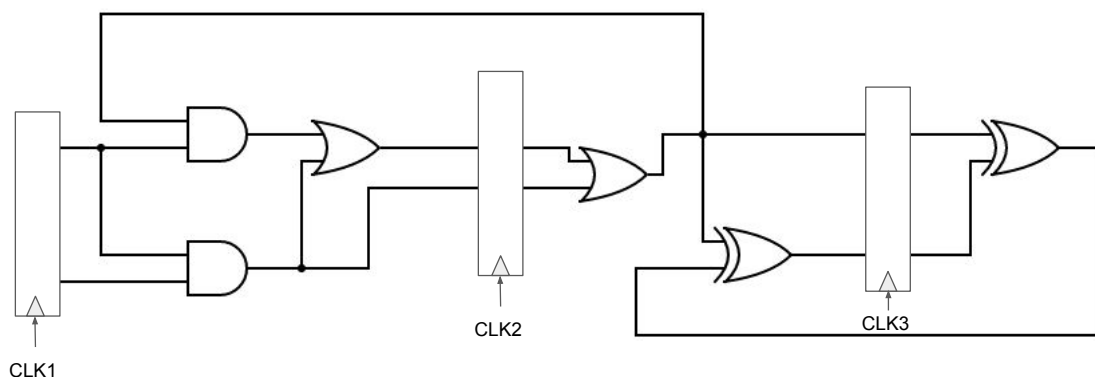


Figure 1: A4. sequential circuit for retiming.

1. Derive the minimal clock cycle time T , suppose that there is no clock skew.
2. Derive the minimal clock cycle time T using a designated skew.

Part B: (10 pts) 8 In Part B, the total weight of the problems is higher than 10 points. You are encouraged to earn up to 10 points. In other words, there is no penalty on wrong solutions, but the maximum points to earn are limited to 10 points. Note that some problems are open, i.e. exact (perfect) solutions may be challenging to derive. Nonetheless, the principles taught in the class can be used to start the exploration.

B.1. Latch: With reference to the SR latch of slide 14 of lecture 7, replace the NOR gate at the bottom with a NAND gate. Complete the state table 1. (5 pts)

id	S	R	Q_t	y_t	Q_{t+1}	y_{t+1}	Q_{t+2}	y_{t+2}	Q_{t+3}	y_{t+3}
0	0	0	0	0						
1	0	0	0	1						
2	0	0	1	0						
3	0	0	1	1						
4	0	1	0	0						
5	0	1	0	1						
6	0	1	1	0						
7	0	1	1	1						
8	1	0	0	0						
9	1	0	0	1						
10	1	0	1	0						
11	1	0	1	1						
12	1	1	0	0						
13	1	1	0	1						
14	1	1	1	0						
15	1	1	1	1						

Table 1: B.1 State Table

B.2. Finite State Machine: With reference to page 4 of lecture 8 slides, we have a pattern-matching game with a fair coin (50% chance on either tail or head for each toss). The coin is tossed in sequence. Each person chooses a pattern of 4 consecutive tosses. The pattern that appears the first wins. Design a pattern so that you have the best chance to win. Explain your solution. (5 pts)

B.3. Timing and Retiming: For the following circuit (figure 4), the timing characteristics of the components are the same as problem A.4. (5 pts)

1. Derive the minimal clock cycle time T , suppose that there is no clock skew.
2. Derive the minimal clock cycle time T using a designated skew. Use $CLK1$ as the reference, write the amounts of skew of the rest of the clock signals, i.e. $CLK2$, $CLKS3$ and $CLK4$ with respect to $CLK1$.

