

CSE140 - HW #3

Due Monday May 6, 11:59PM

Introduction

The purpose of this assignment is to get a better understanding of basic memory elements and the design of sequential circuits. In the first problem, we search and compare the memory devices. For the second problem, we learn to analyze circuits with feedback loops. In the third problem we draw a timing diagram for D-latch and D-flip-flop. In the fourth problem, we translate a pattern recognizer into state diagrams and state tables. Finally, in the fifth problem, we synthesize a sequential circuit.

1 Memory Devices

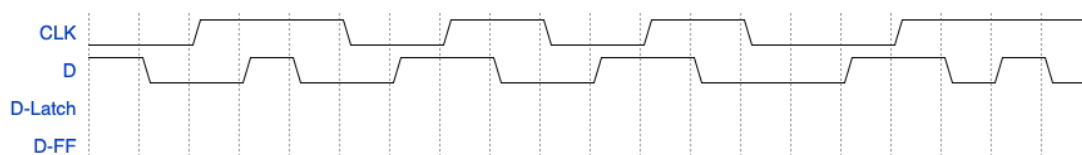
Use a table to list and compare the cost and performance of ten different memory devices (hint: feel free to search available references).

2 Latch

- (1). Given a SR latch of NOR gates, replace the two NOR gates with two NAND gates. Write the state table, state diagram and the characteristic expression of the revised circuit (hint: follow the steps in slides 17, 18, 20 and 26 of lecture 7).
- (2). Given a SR latch of NOR gates, replace the NOR gates at the bottom (slide 17 of lecture 7) with one NAND gate. Analyze the circuit.

3 Timing Diagram of Latch and Flip-Flop

Timing Diagram of Latch and Flip-Flop: Given the input waveforms shown below, sketch the output D-Latch of the latch and the output D-FF of the flip-flop.



4 Pattern Recognizer

A sequential network has one binary input $x(t)$ and one binary output $y(t)$. The network produces $y = 1$, whenever input pattern $x(t-3, t) = 1101$ or 1011 . Otherwise, the output $y = 0$.

- (i) Draw the state diagram.
- (ii) Write the state table.

5 Sequential Circuit Analysis

Given a state machine has one input $x(t)$ and two-bit state $(Q_1(t), Q_0(t))$. The machine is described by the following state equations.

$$Q_1(t+1) = x(t)Q_0(t) + Q_1'(t),$$

$$Q_0(t+1) = Q_1(t)Q_0'(t) + x'(t)Q_1'(t).$$

Use two D flip-flops and a minimal sum-of-products network to implement the machine.

- (i). Fill the state table of the system.

id	$Q_1(t)$	$Q_0(t)$	$x(t)$	$Q_1(t+1)$	$Q_0(t+1)$	D_1	D_0
0	0	0	0				
1	0	0	1				
2	0	1	0				
3	0	1	1				
4	1	0	0				
5	1	0	1				
6	1	1	0				
7	1	1	1				

- (ii). Describe the design using a logic diagram. Show your derivation (K maps).