

CSE140 - Exercise

No due date

The exercises are posted to facilitate us to prepare for the final exam. There is no need to hand in the work for any credit.

1. Serial Adder/Subtractor: Design a serial subtractor that inputs (a_i, b_i) , i.e. the i th bit of two numbers, and outputs the difference d_i at time step i for $i = 0$ to $n - 1$. Show the logic diagram of the circuit.
2. Counter: Given a modulo 16 counter, construct a counter that counts in a repeated sequence of (2, 3, 5, 6, 7, 10, 11, 15, 1) with minimal networks of AND, OR gates. Assume that NOT gates are free. Show the logic diagram of the circuit.
3. Cascaded Counter: Given modulo 16 counters, construct a counter that counts from 15 to 150 with minimal networks of AND, OR gates. Assume that NOT gates are free. Show the logic diagram of the circuit.
4. According to IEEE floating number standard 754 for 32 bit width numbers, we have 1 sign bit, 8 bits for exponent and 23 bits for mantissa. Write the solution of the following.
 - 4.1 How many distinct numbers can the system represent (excluding Inf, NaN)?
 - 4.2 What is the expected relative error for the system to represent a real number?
 - 4.3 $1.101_2 \times 2^{-110} \times 1.011_2 \times 2^{-80}$
 - 4.4 $1.110_2 \times 2^{110} \times 1.101_2 \times 2^{80}$
 - 4.5 $1.101_2 \times 2^{10} - 1.01101011010_2 \times 2^{-10}$ (rounding to the nearest even)
 - 4.6 $(1.101_2 \times 2^{110}) / (1.011_2 \times 2^{-70})$