

Midterm 1 Review Session

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Checklist

- ☐ Boolean Algebra
- ☐ Designing Combinational Circuit
- ☐ Consensus Theorem, Shannon's Expansion
- ☐ CMOS Designs
- ☐ Karnaugh Map, [Sum of Products , Product of Sums] Expressions
- ☐ Universal Logic

Boolean Algebra – True or False, and Why

(Q1) For Boolean algebra, given an equation $xyz=xz$, we can deduce that $y= 1$.

(Q2) For Boolean algebra, the statement $a+a=a$ is true and can be proven by the laws of Boolean algebra.

(Q3) For a switching function of three inputs, i.e. $f(a, b, c)$ and its corresponding K-map, the number of prime implicants can be 5 or more.

Boolean Algebra

(Q1) For Boolean algebra, given an equation $xyz=xz$, we can deduce that $y= 1$.

- False. $y=x+z+W$ is a valid choice.

(Q2) For Boolean algebra, the statement $a+a=a$ is true and can be proven by the laws of Boolean algebra.

- True. $a+a=a$ can be proven true by distributive law and identity law of Boolean algebra.

(Q3) For a switching function of three inputs, i.e. $f(a, b, c)$ and its corresponding K-map, the number of prime implicants can be 5 or more.

- True. An example is $\Sigma m(0,1,2,5,6,7)$, in which we can find 6 prime implicants

Designing Combinational Circuit

A circuit has four inputs and one output. The inputs (a_3, a_2, a_1, a_0) represent a number from 0 to 15. Output Y is true if the number is a multiple of 2 or 3 but not both (0 is counted as a multiple of both 2 and 3).

- A. Describe the truth table.
- B. Write the function in sum-of-products canonical form.
- C. Write the function in product-of-sums canonical form

Designing Combinational Circuit

A circuit has four inputs and one output. The inputs (a_3, a_2, a_1, a_0) represent a number from 0 to 15. Output Y is true if the number is a multiple of 2 or 3 but not both (0 is counted as a multiple of both 2 and 3).

Id	a_3	a_2	a_1	a_0	Y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	1

Canonical SOP

$$\sum m(2, 3, 4, 8, 9, 10, 14, 15)$$

$$= a_3'a_2'a_1a_0' + a_3'a_2'a_1a_0 + a_3'a_2a_1'a_0' + a_3'a_2a_1'a_0 + a_3a_2'a_1'a_0' + a_3a_2'a_1a_0 + a_3a_2a_1a_0' + a_3a_2a_1a_0$$

Canonical POS

$$\prod M(0, 1, 5, 6, 7, 11, 12, 13)$$

$$= (a_3 + a_2 + a_1 + a_0) \cdot (a_3 + a_2 + a_1 + a_0') \cdot (a_3 + a_2' + a_1 + a_0') \cdot (a_3 + a_2' + a_1' + a_0) \cdot (a_3 + a_2' + a_1' + a_0') \cdot (a_3' + a_2' + a_1 + a_0) \cdot (a_3' + a_2' + a_1 + a_0')$$

Consensus Theorem– List all the consensuses in each boolean expression

(Q1) $abd + a'cd + bfg$

(Q2) $a'b'cd + a'd'e' + bde'$

(Q3) $(a+c'+e)(a+c+e)(a'+c+d)$

Consensus Theorem

(Q1) $abd + a'cd + bfg$, Consensus(es): bcd

(Q2) $a'b'cd + a'd'e' + bde'$, Consensus(es): $a'b'ce'$, $a'cde'$, $a'be'$

(Q3) $(a+c'+e)(a+c+e)(a'+c+d)$, Consensus(es): $(a+e), (c+d+e)$

Shannon's Expansion – simplify the expression

$$f(x, y) = (x' + y) \oplus (x + y') \oplus xy \oplus x'y' \oplus x'$$

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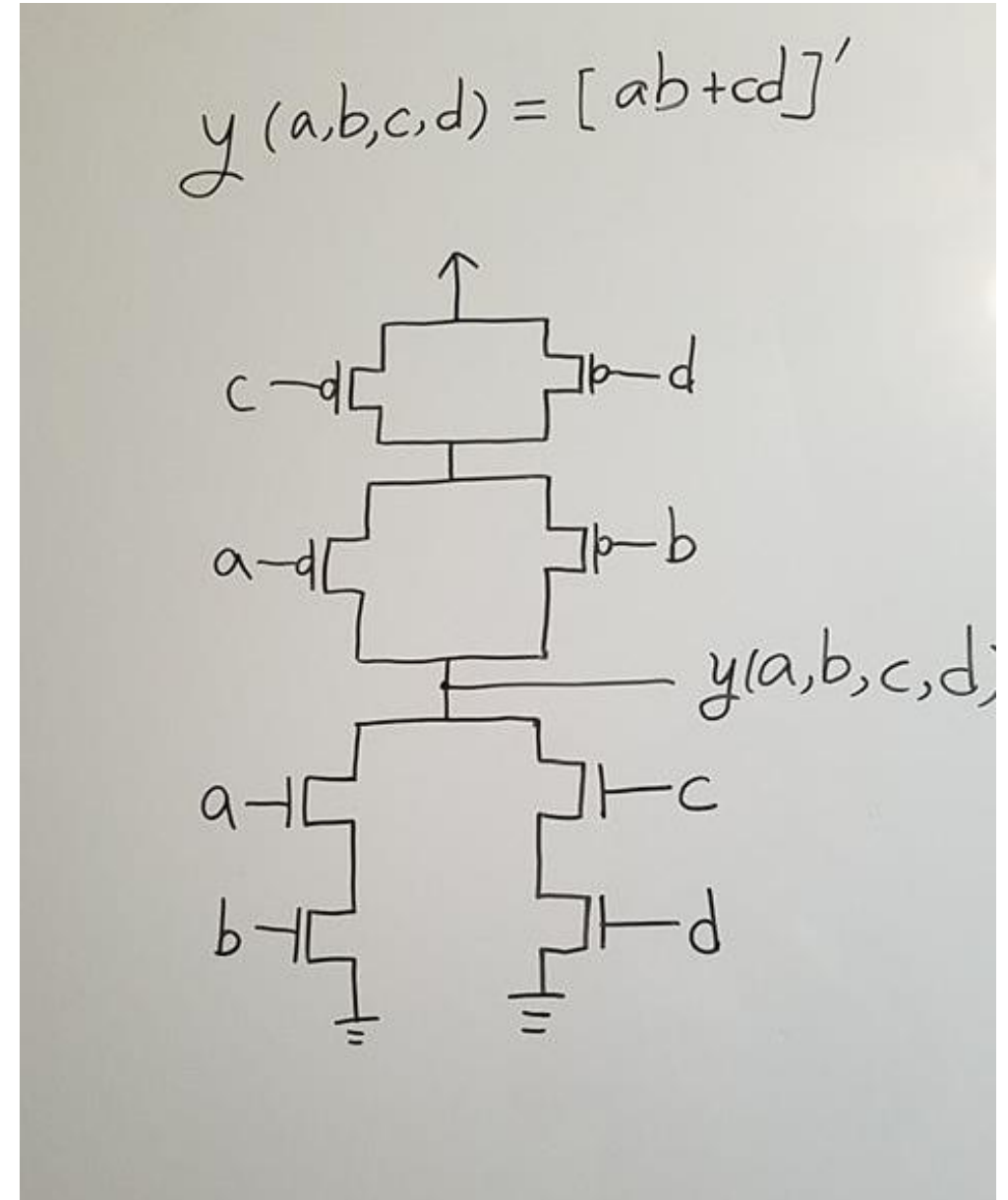
$$\begin{aligned}f(x, y) &= (x'+y)\oplus(x+y')\oplus xy\oplus x'y'\oplus x' \\&= x f(1,y) + x' f(0,y) \\&= x((0+y)\oplus(1+y')\oplus 1y\oplus 0y'\oplus 0) + x'((1+y)\oplus(0+y')\oplus 0y\oplus 1y'\oplus 1) \\&= x(y\oplus 1\oplus y\oplus 0\oplus 0) + x'(1\oplus y'\oplus 0\oplus y'\oplus 1) \\&= x\end{aligned}$$

CMOS Design

- Design a CMOS gate with function $y(a, b, c, d) = [ab+cd]'$. Draw the schematic diagram using NMOS and PMOS transistors as the basic elements.

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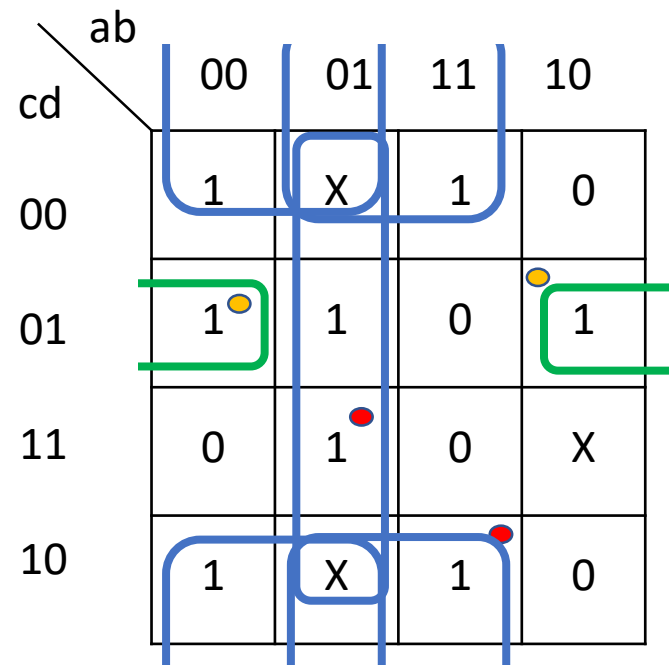


Karnaugh Map, [Sum of Products (SOP) , Product of Sums (POS)]
Expressions – List all the minimal SOP expression

$$f(a, b, c, d) = \sum m(0,1,2,5,7,9,12,14) + \sum d(4,6,11)$$

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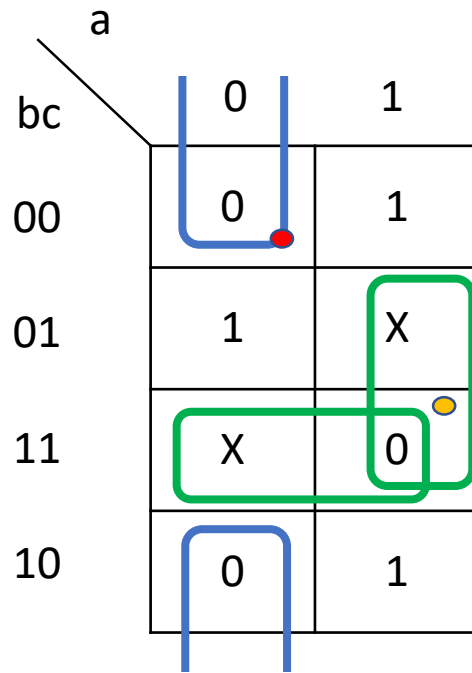
$$f = bd' + a'd' + a'b + b'c'd$$

Karnaugh Map, [Sum of Products (SOP) , Product of Sums (POS)] Expressions – List all the minimal POS expression

$$f(a, b, c) = \sum m(1,4,6) + \sum d(3,5)$$

Karnaugh Map, [Sum of Products (SOP) , Product of Sums (POS)] Expressions – List all the minimal POS expression

$$f(a, b, c) = \sum m(1, 4, 6) + \sum d(3, 5)$$



$$f = (a + c) (a' + c')$$

$$f = (a + c) (b' + c')$$

Universal Logic

(Q1) {AND,NOT} is a universal set of gates.

(Q2) {NOT,XOR} is a universal set of gates.

(Q3) $\{f(a, b, c) = a'b' + b'c' + a'c'\}$ is a universal set of gates.

Universal Logic

(Q1) {AND,NOT} is a universal set of gates.

True. One can use DeMorgan's law to implement OR from {AND,NOT}, so the {AND,NOT} is a universal set.

(Q2) {NOT,XOR} is a universal set of gates.

False. A universal set should be able to implement {AND,OR,NOT}; however, AND is unable to be constructed by {NOT,XOR}.

(Q3) $\{f(a, b, c) = a'b' + b'c' + a'c'\}$ is a universal set of gates.

True. f can implement NOT with $f(a,0,1) = a'$, and OR with $f(f(a,b,1),0,1)$; given {OR,NOT} is a universal set, f is a universal set of gates