

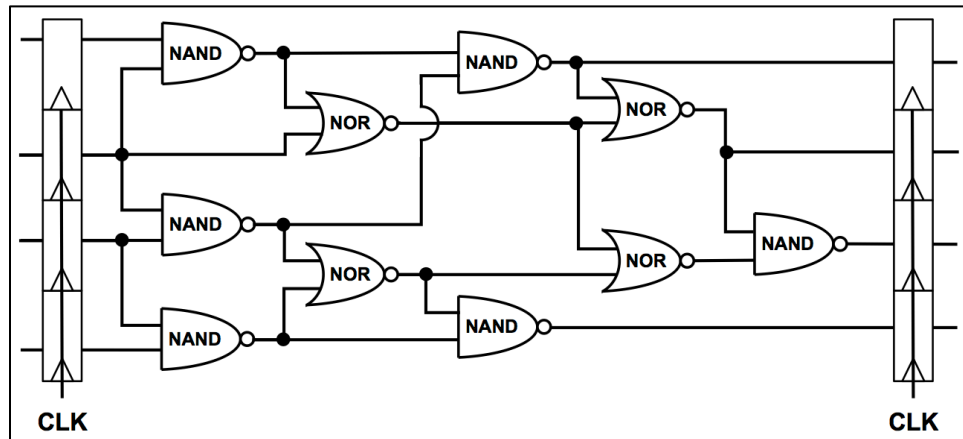
CSE140 Final Solution

Total 100 points (points)

Question 1. Timing and Retiming. (25 points)

For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 30ps$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 20ps$, setup time $t_{setup} = 20ps$, hold time $t_{hold} = 20ps$.
- Logic gate (each NAND, NOR): propagation delay $t_{pd} = 25ps$, contamination delay $t_{cd} = 20ps$.



I.1. Suppose that there is no clock skew. What is the maximum clock frequency of this circuit? (15 points)

15 points for the correct answer.

- 6 points for the correct formula. (Blue font)
Deduct 3 points for incorrect inequality sign.
- 6 points for correctly substituting values into formula.
- 3 points for achieving the correct final answer.
Deduct 1 point for incorrect, or missing units.

$$t_{pcq} + t_{pd(MAX)} + t_{setup} \leq T_c$$

$$30ps + 4 \times 25ps + 20ps \leq T_c$$

$$150ps \leq T_c$$

$$f \leq \frac{1s}{T_c} = \frac{1s}{150ps} \approx 6.67GHz$$

The maximum operating frequency is about 6.67GHz.

I.2. If there is retiming using designated skew, what is the maximum operating frequency of the circuit? (10 points)

10 points for the correct answer.

- 4 points for the correct formula. (Blue font)
Deduct 2 points for incorrect inequality sign.
- 3 points for correctly substituting values into formula.
- 3 points for achieving the correct final answer.
(Deduct 1 point for incorrect, or missing units)

$$150ps - t_{skew} \leq T_c$$

$$t_{ccq} + t_{cd(min)} \geq t_{hold} + t_{skew}$$

$$20ps + 2 \times 20ps \geq 20ps + t_{skew}$$

$$40ps \geq t_{skew}$$

The maximum applicable skew is 40ps.

$$150ps - 40ps = 110ps \leq T_c$$

$$f \leq \frac{1s}{T_c} = \frac{1s}{110ps} \approx 9.09GHz$$

The maximum operating frequency is about 9.09GHz.

Question 2. Decoders. (20 points)

Given three three-input Boolean functions,

$$f_1(a, b, c) = \sum m(1, 3, 5, 7) + \sum d(2, 6),$$

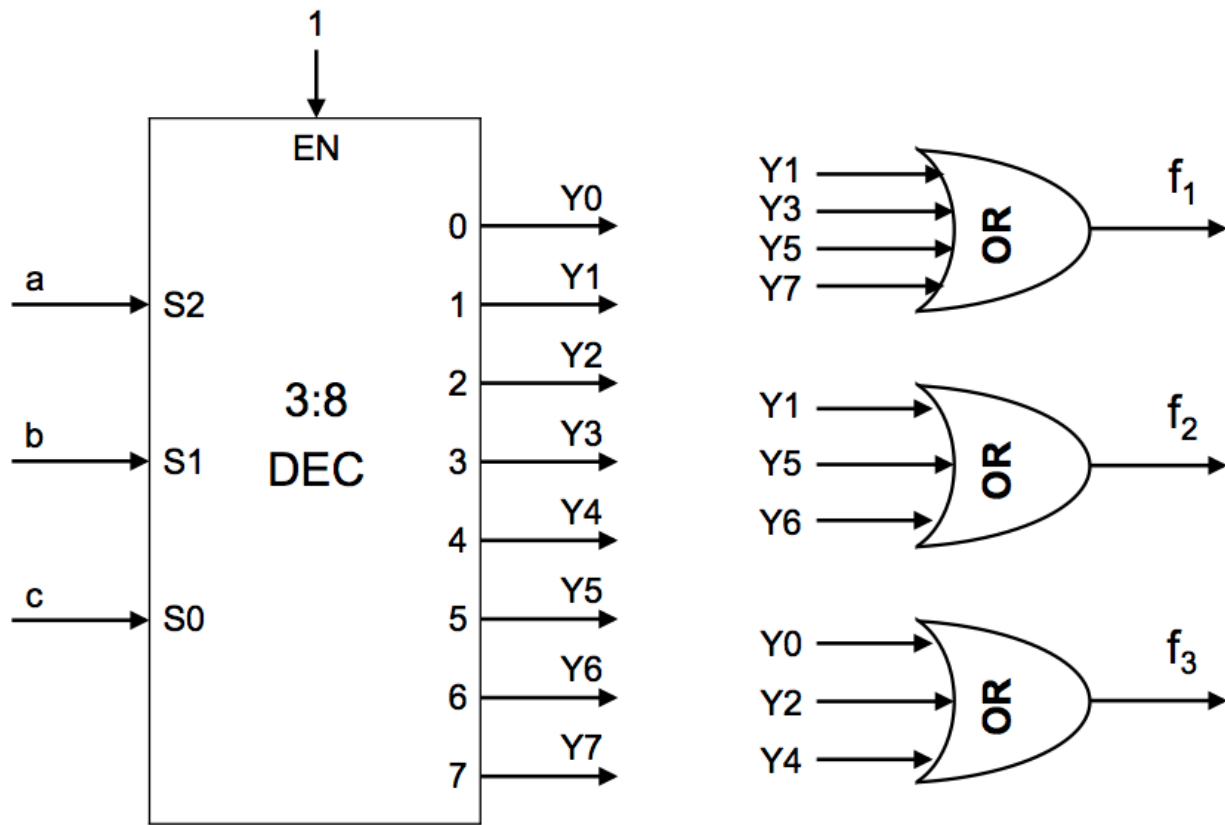
$$f_2(a, b, c) = \sum m(1, 5, 6) + \sum d(2),$$

$$f_3(a, b, c) = \sum m(0, 2, 4).$$

II.1. Implement the functions using a minimal network of 3:8 decoders and OR gates. (10 points)

10 points for the correct answer.

- -1 points for no or incorrect labeling.
- -1 points for each wrong decoder inputs (lack of input or having irrelevant input variables).
- -5 points for using more than one 3:8 decoder or design does not yield the correct output.
- -3 points for not connecting the output to each of the three functions.

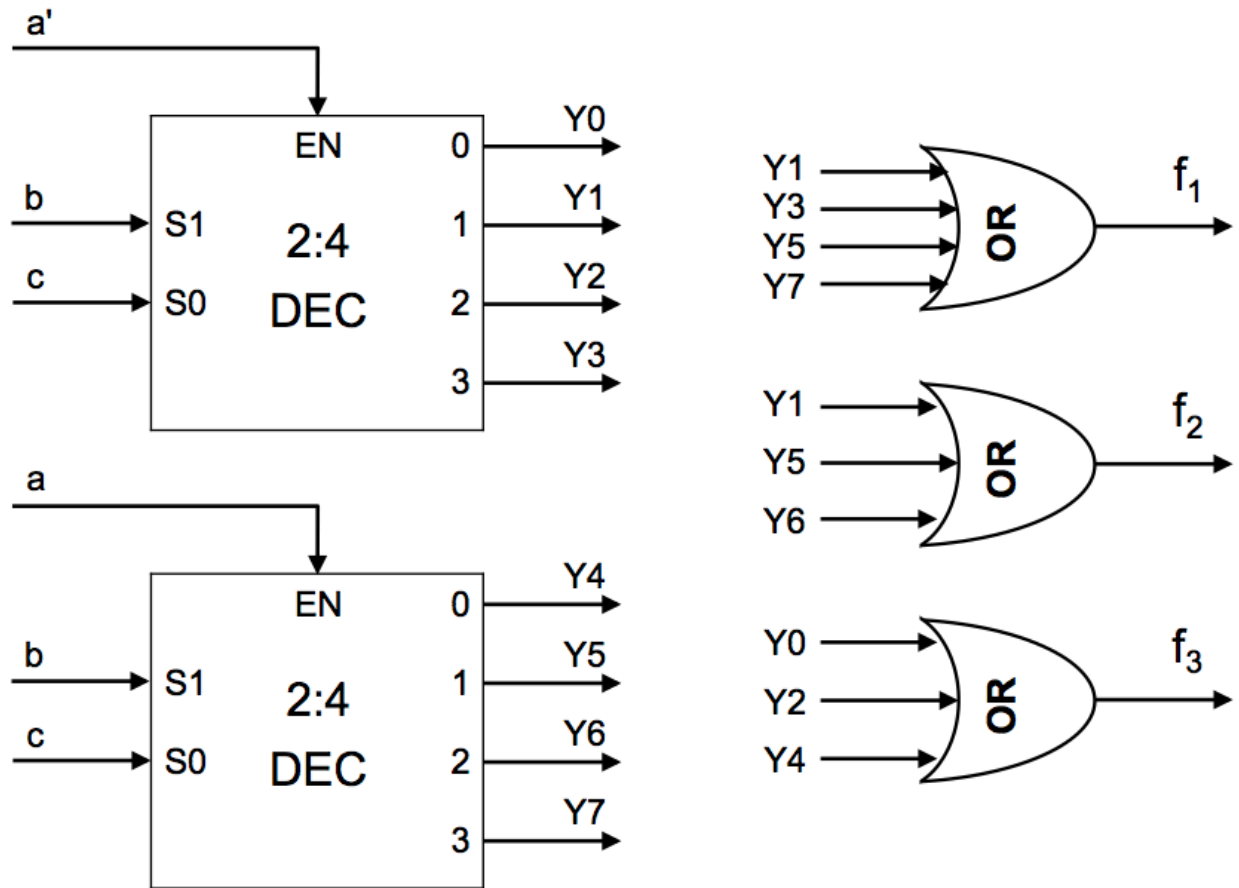


a : MSB, **c** : LSB.

II.2. Implement the functions using a minimal network of 2:4 decoders and OR gates. (10 points)

10 points for the correct answer.

- -1 points for no or incorrect labeling.
- -1 points for each wrong decoder inputs (lack of input or having irrelevant input variables).
- -5 points if the design is completely different from standard solution.
E.g., using 3:8 decoders, 1:2 decoders, or MUXes. Or an implementation that yields incorrect outputs.
- -3 points for not connecting the output to each of the three functions.



a : MSB, c : LSB.

Question 3. Multiplexers (MUXes). (25 points)

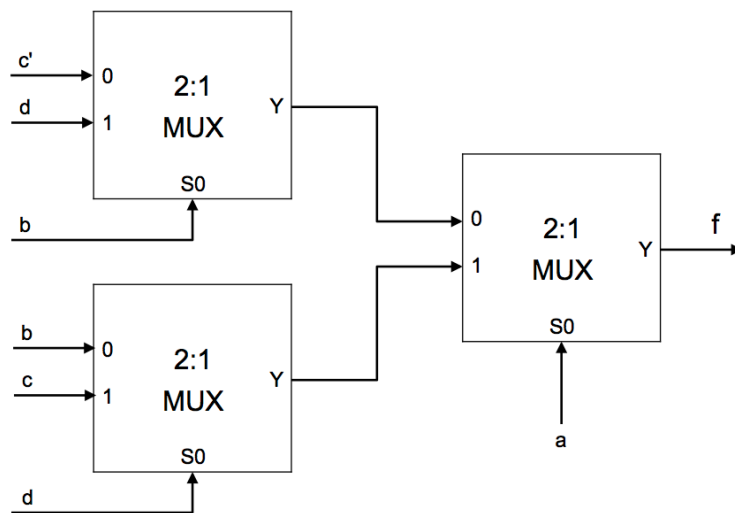
Given a three three-input Boolean function,

$$f(a,b,c,d) = \sum m(0,1,5,7,11,14) + \sum d(3,6,12,15),$$

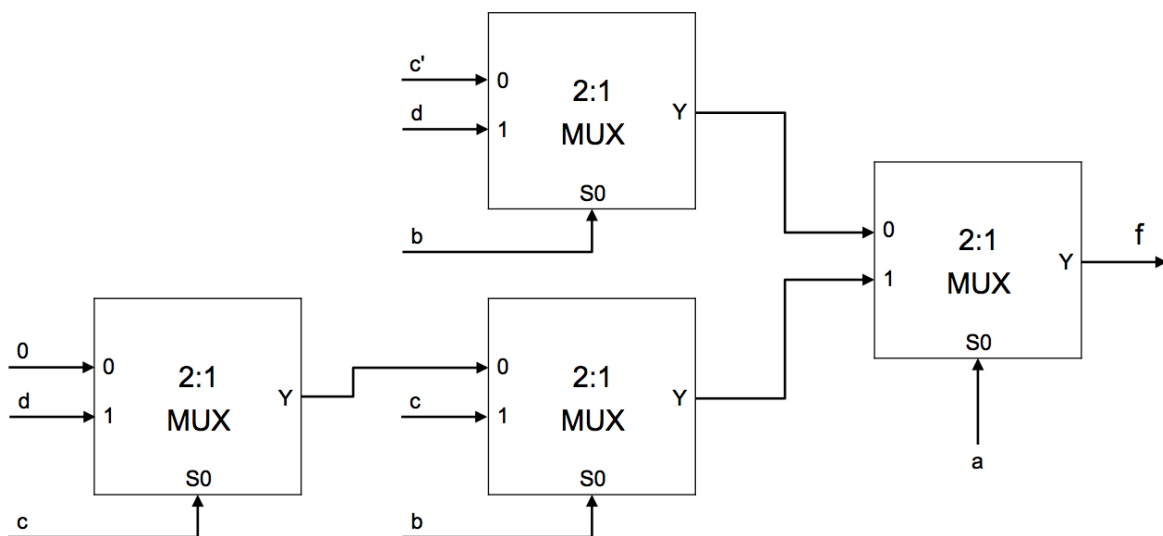
Implement the function using a minimal network of 2:1 multiplexers by drawing the logic diagram.

25 points for the correct answer.

- There are many possible solutions. If the final diagram is correct, give full credits.
- When the diagram is not correct:
 1. -5 points for each extra MUX, up to -10 points.
 2. -3 points for each missing MUX, up to -10 points.
 - 3 points for each incorrect input for MUX, up to -10 points.
 - 3 points for each incorrect selector of MUX, up to -10 points.
 - 1 point for each missing labeling, up to -10 points.
 3. 5 points for attempt.



Solution 1: The optimal solution.



Solution 2: The minimal solution when one decomposes in alphabetical order.

Question 4. System Designs. (30 points)

Implement the following algorithm:

```
Alg(X, Y, Z, start, W, done);
Input X[7:0], Y[7:0], Z[7:0], start;
Output W[7:0], done;
Local-object A[7:0], B[7:0], C[7:0];
S0: If start' goto S0 || done  $\leftarrow$  1;
S1: A  $\leftarrow$  X || B  $\leftarrow$  Y || C  $\leftarrow$  Z || done  $\leftarrow$  0;
S2: if (A[7]) goto S4;
S3: A  $\leftarrow$  A+B || B  $\leftarrow$  B+C;
S4: if C'[7] goto S2 || C  $\leftarrow$  Inc(C);
S5: A  $\leftarrow$  Inc(A) || if B[7] goto S3;
S6: W  $\leftarrow$  A || goto S0;
End Alg
```

IV.1. Design a data subsystem that is adequate to execute the algorithm by answering the following questions. (15 points)

IV.1.1. Use a table to list the instructions and the corresponding components that should be used in the data path subsystem.

5 points for the correct answer.

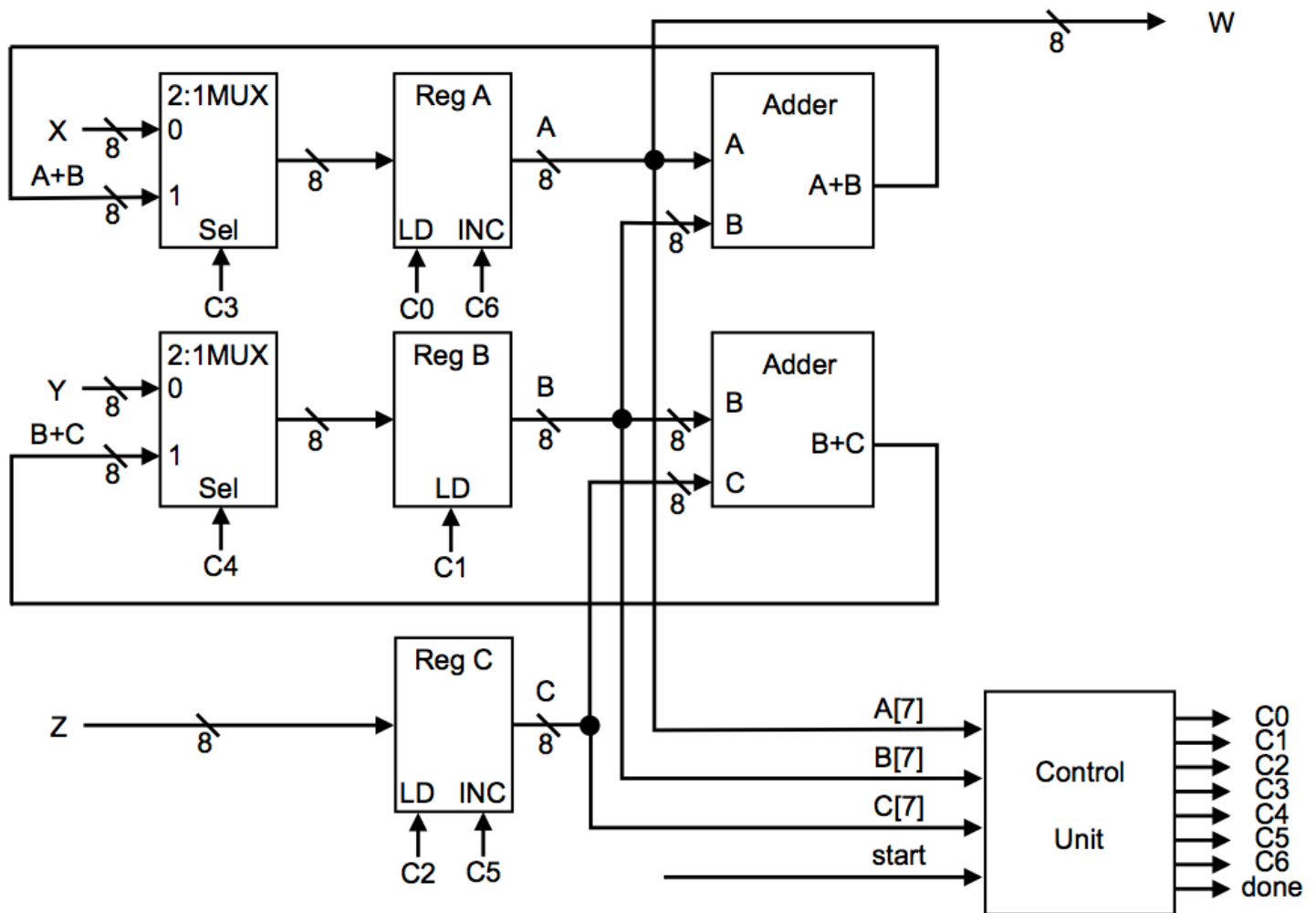
- Here, the column of control signal is not mandatory.
- Here, the rows in blue font are mandatory.
- Deduct 1 point for incorrect row (up to 5 points) from only rows in blue font.
- Deduct 1 point for missing state column.

State	Statement	Operation	Control
S0	done $\leftarrow$ 1		done=1
S1	A $\leftarrow$ X	A $\leftarrow$ Load(X)	C0=1, C3=0
S1	B $\leftarrow$ Y	B $\leftarrow$ Load(Y)	C1=1, C4=0
S1	C $\leftarrow$ Z	C $\leftarrow$ Load(Z)	C2=1
S3	A $\leftarrow$ A+B	A $\leftarrow$ Add(A, B)	C0=1, C3=1
S3	B $\leftarrow$ B+C	B $\leftarrow$ Add(B, C)	C1=1, C4=1
S4	C $\leftarrow$ Inc(C)	C $\leftarrow$ Inc(C)	C5=1
S5	A $\leftarrow$ Inc(A)	A $\leftarrow$ Inc(A)	C6=1
S6	W $\leftarrow$ A	wire	

IV.1.2. Draw the schematic diagram to show the data path subsystem. Label the inputs, outputs, and control signals of all components.

10 points for the correct answer.

- There are many possible solutions. If the schematic diagram is correct, give full credits.
- Assume the system is dual-rail system.
- Deduct 1 point for each missing module. (Up to 4 points)
- Deduct 1 point for each wrong wire or missing control input for module. (Up to 2 points)
- Deduct 1 point for missing labeling, i.e., the system is not readable by human.
- Deduct 3 points for missing control unit.
E.g., Deduct 1 point per each missing control signal, input and output. (Up to 3 points)



IV.2. Design the control subsystem by answering the following questions. (15 points)

IV.2.1. Use a table to list the value of control signals for every state.

4 points for the correct answer.

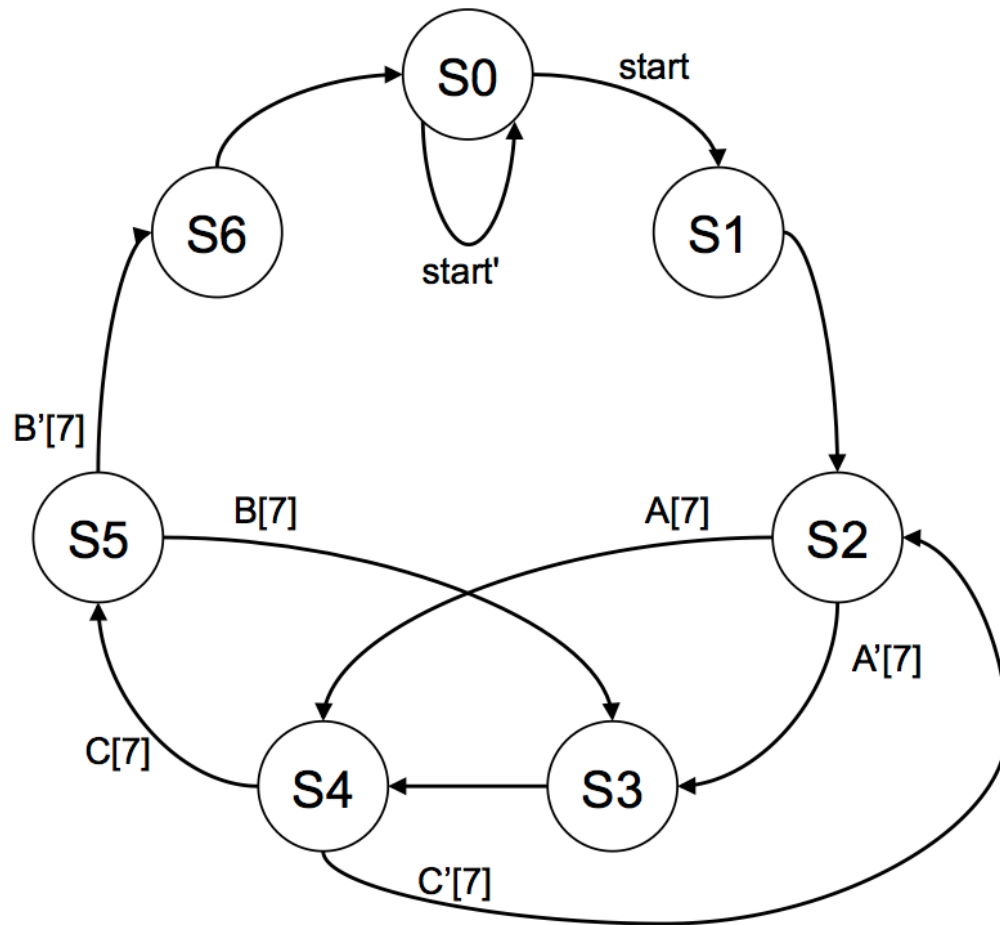
- There are many possible solutions, but the table depends on IV.1's design. If the table is correct, give full credits.
- Deduct 0.5 point for each incorrect column (up to 4 points).

	C0	C1	C2	C3	C4	C5	C6	done
S0	0	0	0	-	-	0	0	1
S1	1	1	1	0	0	0	0	0
S2	0	0	0	-	-	0	0	0
S3	1	1	0	1	1	0	0	0
S4	0	0	0	-	-	1	0	0
S5	0	0	0	-	-	0	1	0
S6	0	0	0	-	-	0	0	0

IV.2.2. Draw the state diagram.

3 points for the correct answer.

- Deduct 1 point if there is one error.
- Deduct 2 point if there are more than one error.



IV.2.3. Implement the control subsystem using a one hot encoding design. Draw the logic diagram.

8 points for the correct answer.

- There are many possible solutions. If the diagram is correct, give full credits.
- Deduct 1 point for each missing AND gate. (up to 3 points)
- Deduct 1 point for each missing OR gate. (up to 3 points)
- Deduct 1 point for each missing control signal output. (up to 3 points)
- Deduct 1 point for each incorrect wire. (up to 3 points)
- Deduct 1 point for each missing label, i.e., unrecognizable wire or module. (up to 3 points)

