

Name _____

CSE140 Final, 3-6PM, Monday March 14, 2016

Please read the following instructions carefully:

If you are unclear about any of the questions on the exam, please make the most plausible assumption to answer the question. Instructors and proctors will not answer questions on the exam material. Please write your name on the top of each page. Write the names of the students to your left and right in the space provided.

Name of student to your left: _____

Name of student to your right: _____

	Total Points	Points Awarded
Problem I	25	
Problem II	20	
Problem III	25	
Problem IV	30	
Total	100	

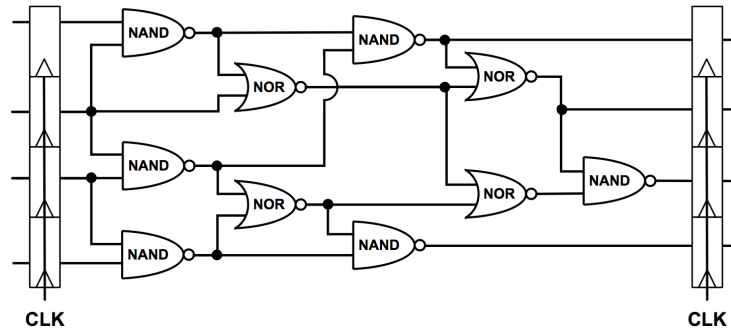
Please note that cheating on the exam will have serious consequences.

Don't risk your academic career.

All the Best!!

(I) (Timing and Retiming) For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 30\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 20\text{ps}$, setup time $t_{setup} = 20\text{ps}$, hold time $t_{hold} = 20\text{ps}$
- Logic gate (each NAND, NOR): propagation delay $t_{pd} = 25\text{ps}$, contamination delay $t_{cd} = 20\text{ps}$.



I.1. Suppose that there is no clock skew. What is the maximum clock frequency of this circuit? (15 points)

I.2. If there is retiming using designated skew, what is the maximum operating frequency of the circuit? (10 points)

(II) (Decoders) Given three three-input Boolean functions (20 points)

$$f_1(a, b, c) = \sum m(1, 3, 5, 7) + \sum d(2, 6),$$

$$f_2(a, b, c) = \sum m(1, 5, 6) + \sum d(2),$$

$$f_3(a, b, c) = \sum m(0, 2, 4).$$

II.1. Implement the functions using a minimal network of 3:8 decoders and OR gates.

II.2. Implement the functions using a minimal network of 2:4 decoders and OR gates.

(III) (Multiplexers) Given a four-input Boolean function (25 points)

$$f(a, b, c, d) = \sum m(0, 1, 5, 7, 11, 14) + \sum d(3, 6, 12, 15).$$

Implement the function using a minimal network of 2:1 multiplexers by drawing the logic diagram.

(IV). (System Designs) Implement the following algorithm:

```
Alg(X, Y, Z, start, W, done);  
Input X[7:0], Y[7:0], Z[7:0], start;  
Output W[7:0], done;  
Local-object A[7:0], B[7:0], C[7:0];  
S0: If start' goto S0 || done  $\Leftarrow$  1;  
S1: A  $\Leftarrow$  X || B  $\Leftarrow$  Y || C  $\Leftarrow$  Z || done  $\Leftarrow$  0;  
S2: if (A[7]) goto S4;  
S3: A  $\Leftarrow$  A+B || B  $\Leftarrow$  B+C;  
S4: if C'[7] goto S2 || C  $\Leftarrow$  Inc(C);  
S5: A  $\Leftarrow$  Inc(A) || if B[7] goto S3;  
S6: W  $\Leftarrow$  A || goto S0;  
End Alg
```

IV.1. Design a data subsystem that is adequate to execute the algorithm by answering the following questions. (15 points)

IV.1.1. Use a table to list the instructions and the corresponding components that should be used in the data path subsystem.

IV.1.2. Draw the schematic diagram to show the data path subsystem. Label the inputs, outputs, and control signals of all components.

IV.2. Design the control subsystem by answering the following questions. (15 points)

IV.2.1. Use a table to list the value of control signals for every state.

IV.2.2. Draw the state diagram.

IV.2.3. Implement the control subsystem using a one hot encoding design. Draw the logic diagram.