

Name _____

CSE140 Midterm 2, Wednesday February 17, 2016

Please read the following instructions carefully:

If you are unclear about any of the questions on the exam, please make the most plausible assumption to answer the question. Instructors and proctors are supposed not to answer questions on the exam material. Please write your name on the top of each page. Write the names of the students to your left and right in the space provided.

Name of student to your left: _____

Name of student to your right: _____

	Total Points	Points Awarded
Problem 1	15	
Problem 2	10	
Problem 3	15	
Problem 4	30	
Problem 5	30	
Total	100	

All the Best!!

1. Universal Set of Gates: Check if the set in the following list is universal and explain your decision in less than 10 words. Assuming constants 0 and 1 are available as inputs (15 points).

1.1. {AND, OR}

True False

1.2. {XOR, NOT}

True False

1.3. {NOR}

True False

1.4. $\{f(x, y)\}$, where $f(x, y) = xy + x'y'$

True False

1.5. $\{f(a, b, c)\}$, where $f(a, b, c) = (a' + b + c)(a + b' + c)(a + b + c')$

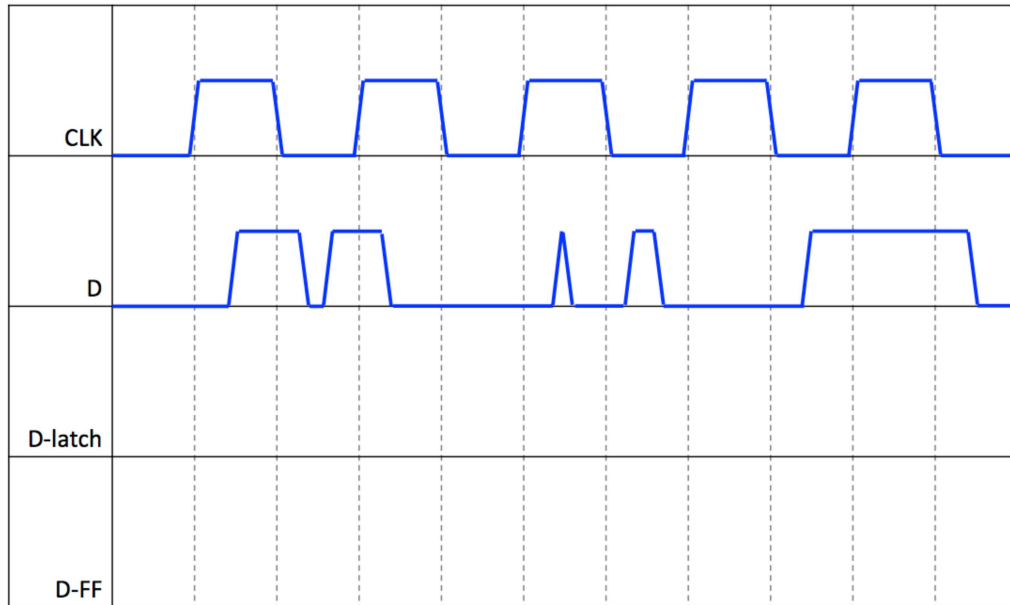
True False

2. Other Types of Gates: Consider the function $f(x, y)$ where $\oplus$ is an Exclusive OR operator: $f(x, y) = (xy) \oplus (x'y') \oplus x \oplus x' \oplus (x + y')$.

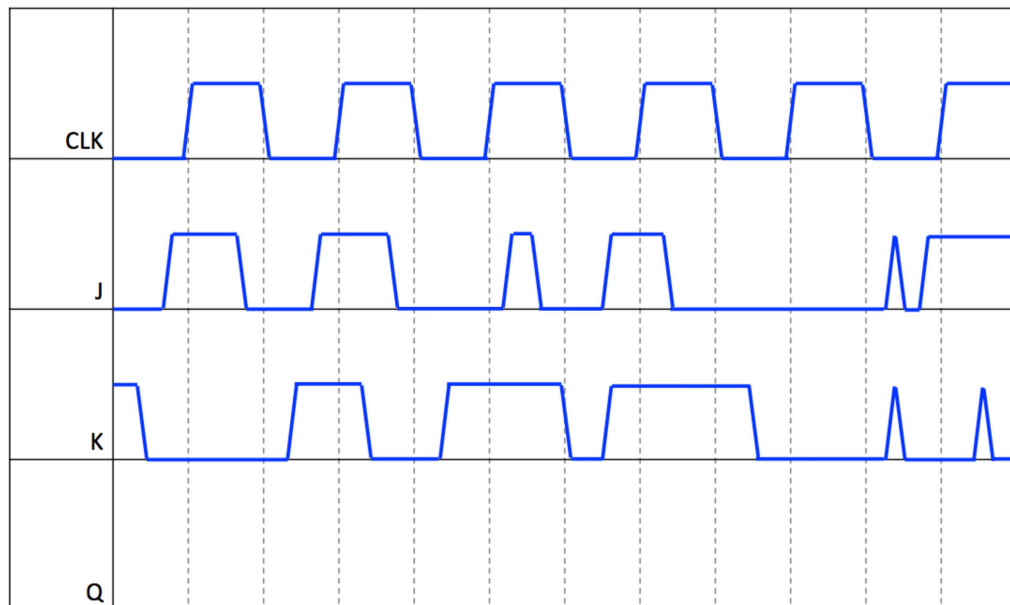
Simplify the function into a minimal sum of products expression using switching function techniques e.g. Shannon's expansion. Show your derivation. (10 points).

3. Timing Diagram of Latch and Flip-Flop:

3.1 Given the input waveforms shown below, sketch the output, Q, of a D latch and a D flip-flop (10 points).



3.2 Given the input waveforms shown below, sketch the output, Q, of a JK flip-flop. The flip flop is triggered at the rising edge of the clock. (5 points).



4. (Finite State Machine: State Diagram) A pattern recognizer produces output $y = 1$ whenever its input $x(t-4, t) = 01010$, otherwise output $y = 0$.

4.1 Implement the system with a Mealy machine using a minimal number of states.

(i) Use a state diagram to demonstrate the design. Label the *initial state* (the state when the machine is turned on and before any input is read) as S_0 (10 points).

(ii) Fill the following table as the machine starts at state S_0 and process through the given input x from CLK (Clock) sequence =1 to 10 (5 points).

CLK	1	2	3	4	5	6	7	8	9	10
x	0	0	1	0	1	0	1	0	1	0
state	S_0									
y										

4.2 Implement the system with a Moore machine with a minimal number of states.

(i) Use a state diagram to demonstrate the design. Again, label the initial state as S_0 (10 points).

(ii) Fill the following table as the machine starts at state S_0 and process through the given input x from CLK (Clock) sequence =1 to 10 (5 points).

CLK	1	2	3	4	5	6	7	8	9	10
x	1	0	1	0	1	0	1	0	1	1
state	S_0									
y										

5. A state machine has one input $x(t)$ and two-bit state $(Q_1(t), Q_0(t))$. The machine is described by the following state equations.

$$Q_1(t+1) = x'(t)Q_1'(t)Q_0(t),$$

$$Q_0(t+1) = Q_1(t)Q_0(t).$$

Use two **T flip-flops** and a minimal sum-of-products network to implement the machine.

(i). Fill the state table of the system. (15 points).

id	$Q_1(t)$	$Q_0(t)$	$x(t)$	$Q_1(t+1)$	$Q_0(t+1)$	T_1	T_0
0	0	0	0				
1	0	0	1				
2	0	1	0				
3	0	1	1				
4	1	0	0				
5	1	0	1				
6	1	1	0				
7	1	1	1				

(ii). Describe the design using a logic diagram. Show your derivation (K maps) (15 points).