

MT2 Rubric

5 Problems

Problem 1 - 20 points

Problem 2 - 30 points

Problem 3 - 25 points

Problem 4 - 25 points

Problem 5 - 50 points

Total - 150

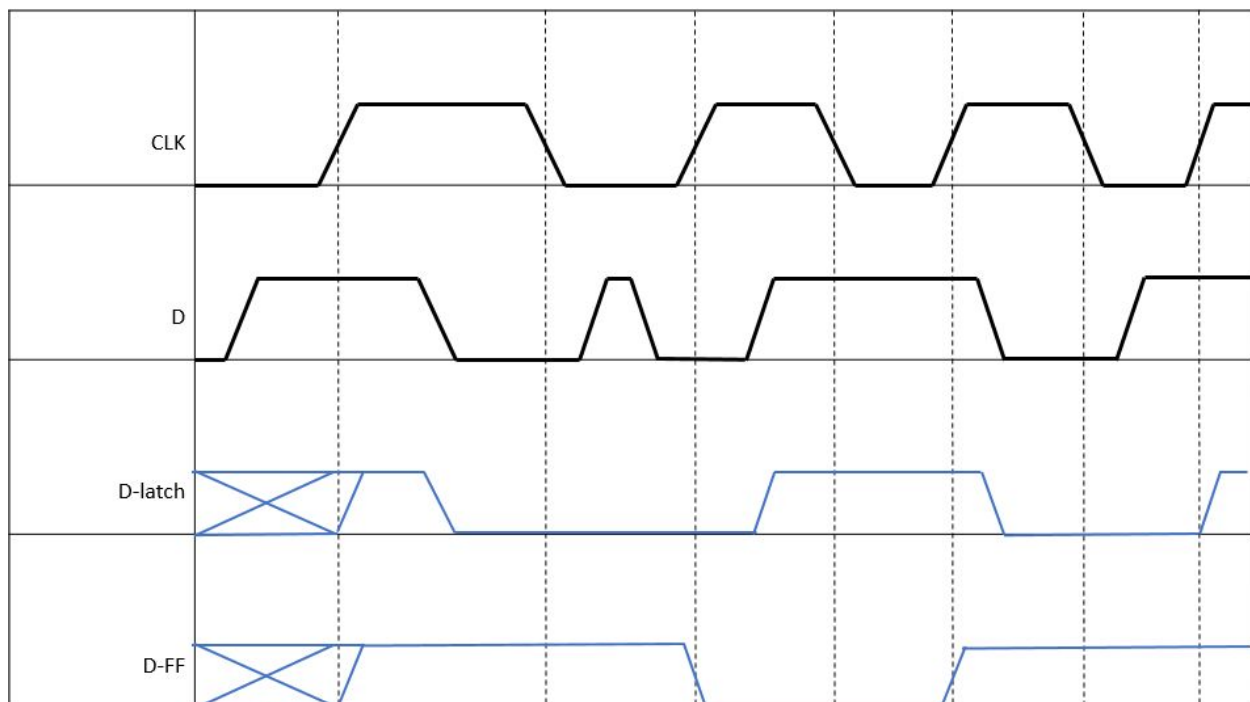
Problem 1

1.1 D-latch (10 points)

- -3 points per error between rising edges of clock

1.2 D-FF (10 points)

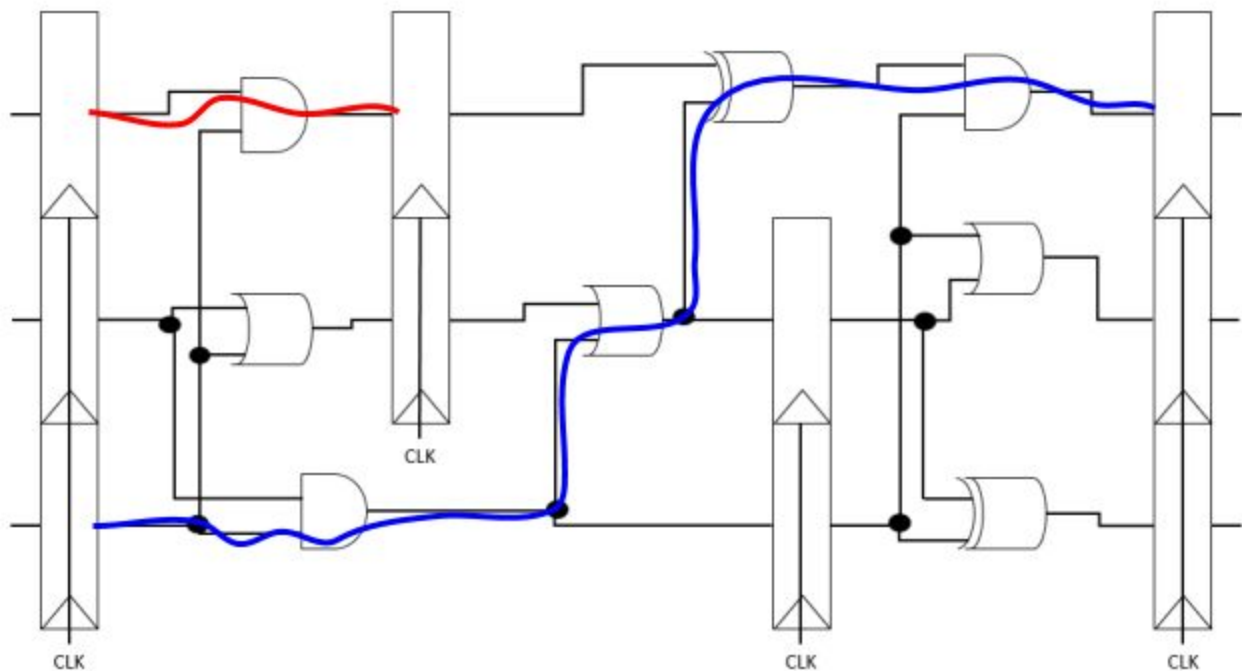
- -3 points per error between rising edges of clock
- -10 points total if D-latch and D-FF output are swapped, but otherwise correct



Problem 2

2. (Timing and Retiming) For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay) $tpcq = 30ps$, clock-to-Q minimum delay (contamination delay) $tccq = 20ps$, setup time $tsetup = 20ps$, hold time $thold = 30ps$
- Logic gate (each AND, OR, XOR): propagation delay $tpd = 25ps$, contamination delay $tcd = 15ps$.



2.1. Suppose that there is no clock skew. What is the maximum clock frequency of this circuit? (15 points)

- 5 points for correct equation
- 5 points for correct $tpd(max)$
- 5 points for correct answer
- -2 points if left as clock period or the conversion from clock period to frequency is wrong
- -1 point if specified as min frequency instead of max frequency

$t_{pd}(\max) = 4 \text{ gates} * 25\text{ps each} = 100\text{ps}$ (blue path above)

$T_c \geq t_{pcq} + t_{pd}(\max) + t_{setup} = 30 + 100 + 20 = 150$

$T_c \geq 150 \text{ ps}$

clock frequency = $1/T_c \leq 6.66 \text{ GHz}$

2.2. How much clock skew can the circuit tolerate before it experiences a hold time violation? (15 points)

- 5 points for correct equation
- 5 points for correct $t_{cd}(\min)$
- 5 points for correct answer

$t_{cd}(\min) = 1 \text{ gate} * 15\text{ps each} = 15\text{ps}$ (red path above)

$t_{hold} + t_{skew} < t_{ccq} + t_{cd}(\min) \Rightarrow t_{skew} < t_{ccq} + t_{cd}(\min) - t_{hold}$

$t_{skew} < 20 + 15 - 30 = 5$

$t_{skew} < 5\text{ps}$

Problem 3

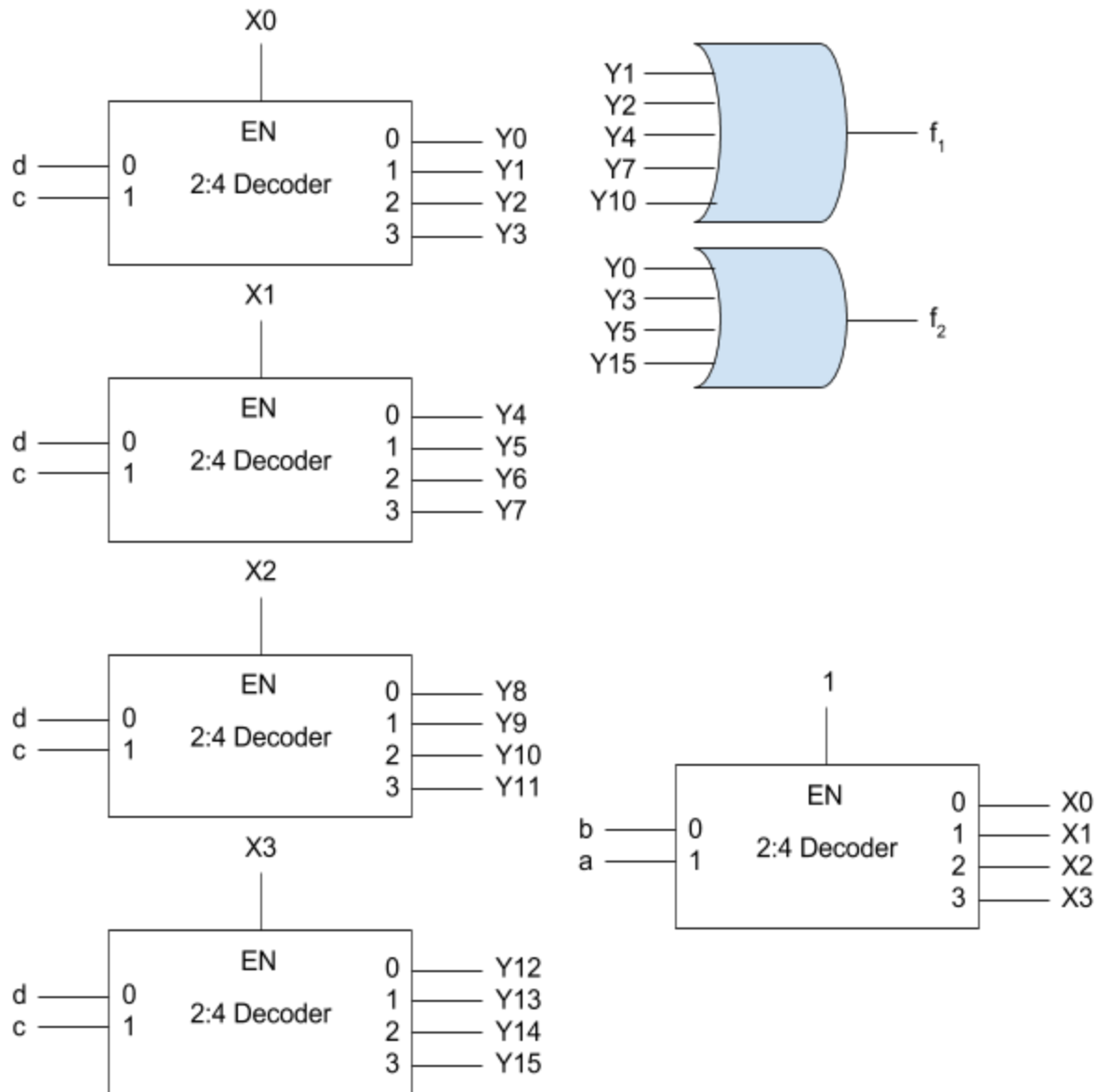
3. (Decoders) Given two four-input Boolean functions

$$f_1(a, b, c, d) = \sum m(1, 2, 4, 7, 10) + \sum d(3),$$

$$f_2(a, b, c, d) = \sum m(0, 3, 5, 15) + \sum d(7),$$

implement the functions using a minimal network of 2:4 decoders and OR gates. Describe the design with a logic diagram (25 points).

- 5 points for using only decoder and OR gates
- -3 points for each incorrect/missing input on f_1 or f_2 (-10 max for each of f_1 and f_2)
- -5 total points if inputs or outputs of decoders are missing or order is reversed
- -5 points for missing/unproduced/incorrect enable inputs
- -10 points if ab and cd are swapped
- -5 points for not labeled OR gate outputs
 - -1 point if one is labeled, but not the other
- -10 points if only their highest level decoder has additional “select” inputs but



Problem 4

4. (Multiplexers) Given a three-input Boolean function

$$f(a, b, c) = \sum m(0, 2, 3, 5, 6) + \sum d(7),$$

implement the function using a minimal network of 2:1 multiplexers. Describe the design with a logic diagram (25 points).

- 5 points for each 2nd level input (20 points total)
- 5 points if there exists a 1st level mux

- -5 points for missing or out of order inputs to the muxes
- -1 point for no output of “f”
- -5 points for correct but non-minimal

a	b=0 c=0	b=0 c=1	b=1 c=0	b=1 c=1	D(b,c,d)
0	1	0	1	1	$b + c'$
0	0	1	1	X	$b + c$

D0

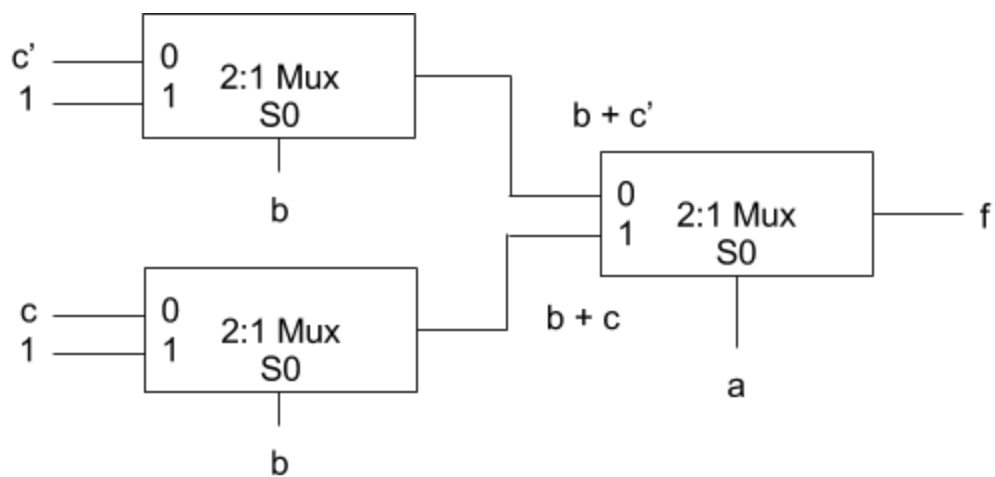
c\b	0	1
0	1	1
1	0	1

$$D0 = b + c'$$

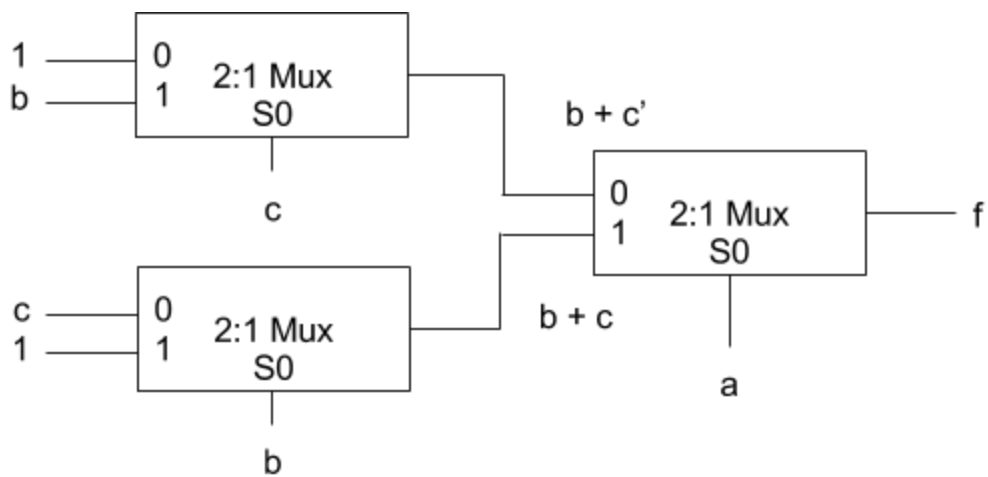
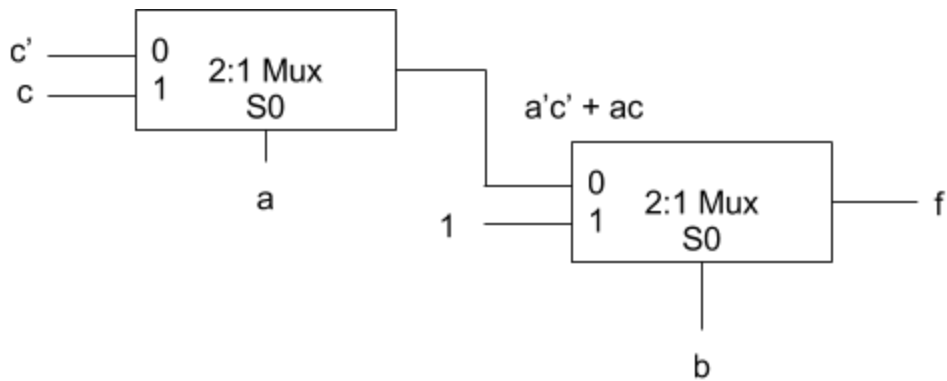
D1

c\b	0	1
0	0	1
1	1	X

$$D1 = b + c$$



Other correct answers



Problem 5

(Finite State Machine) A state machine is described by the following state equations.

$$Q1(t + 1) = Q0(t),$$

$$Q0(t + 1) = Q'1(t)x(t),$$

$$y(t) = Q1(t)Q'0(t)x(t).$$

5.1. Write the state table (10 points).

- -0.5 points per wrong entry for $Q1(t+1)$, $Q0(t+1)$ and $y(t)$; min 0 points (24 entries)

$Q1(t)$	$Q0(t)$	$x(t)$	$Q1(t+1)$	$Q0(t+1)$	$y(t)$
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	1	0	0

$Q1(t)Q0(t) \setminus \text{INPUT}$	0	1
$S0 = 00$	$S0,0$	$S1,0$
$S1 = 01$	$S2,0$	$S3,0$
$S2 = 10$	$S0,0$	$S0,1$
$S3 = 11$	$S2,0$	$S2,0$

5.2. Design the system with two JK flip-flops. Describe $y(t)$; $J1(t)$; $K1(t)$; $J0(t)$; $K0(t)$ as functions of variables $(Q1(t); Q0(t); x)$ in minimal sum-of-products expressions. No need to draw the logic diagram (20 points).

- -4 points for each of $J1$, $K1$, $J0$, $K0$, and y not being correct or missing
- -2 points for each non-minimal, but correct equation

$Q1(t)$	$Q0(t)$	$x(t)$	$Q1(t+1)$	$J1(t)$	$K1(t)$	$Q0(t+1)$	$J0(t)$	$K0(t)$	$y(t)$
0	0	0	0	0	-	0	0	-	0
0	0	1	0	0	-	1	1	-	0
0	1	0	1	1	-	0	-	1	0
0	1	1	1	1	-	1	-	0	0
1	0	0	0	-	1	0	0	-	0
1	0	1	0	-	1	0	0	-	1
1	1	0	1	-	0	0	-	1	0
1	1	1	1	-	0	0	-	1	0

$$J1 = Q0$$

$x \backslash Q1Q0$	00	01	11	10
0	0	1	X	X
1	0	1	X	X

$$K1 = Q0'$$

$x \backslash Q1Q0$	00	01	11	10
0	X	X	0	1
1	X	X	0	1

$$J0 = Q1'x$$

x\Q1Q0	00	01	11	10
0	0	X	X	0
1	1	X	X	0

$$K0 = Q1 + x'$$

x\Q1Q0	00	01	11	10
0	X	1	1	X
1	X	0	1	X

$$y = Q1Q0'x$$

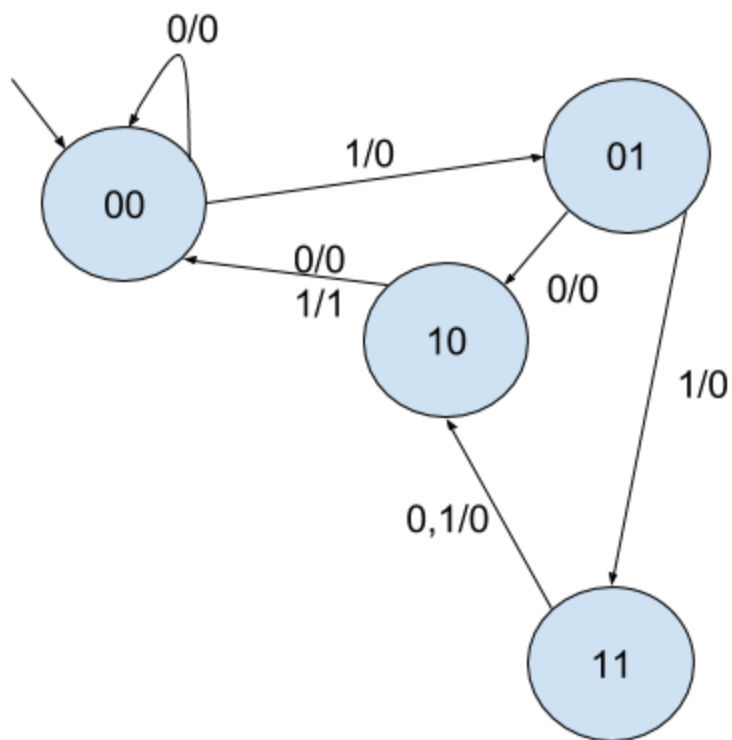
x\Q1Q0	00	01	11	10
0	0	0	0	0
1	0	0	0	1

5.3. Implement the system with a Moore machine with a minimal number of states.

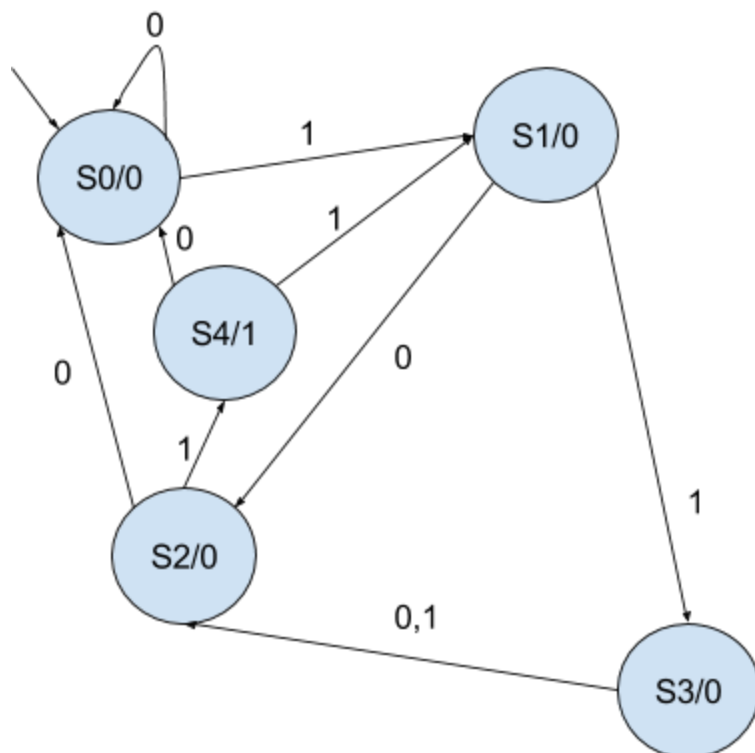
(i) Use a state diagram to demonstrate the design. Label the initial state as S0 (10 points).

- 5 points for drawing a Moore machine
- 5 points for Moore machine being correct
 - - 1 point for each error (bad transitions or outputs, etc.)
- *3 points total if correct mealy machine

Mealy form



Moore form



(ii) Fill the following table as the machine starts at state S_0 and process through the given input x from CLK (Clock) sequence =1 to 10 (10 points).

- 0.5 points for each correct entry of state and output

Time	1	2	3	4	5	6	7	8	9	10
Input	1	1	0	1	0	1	0	1	0	0
State	S_0	S_1	S_3	S_2	S_4	S_0	S_1	S_2	S_4	S_0
Output	0 or 1	0	0	0	1	0	0	0	1	0