

CSE140 Midterm 2, June 8, 2017, Name_____

1. Timing Diagram of Latch and Flip-Flop:

1.1 Given the input waveforms shown below, sketch the output, Q , of a **D latch** (10 points).

1.2 Given the input waveforms shown below, sketch the output, Q , of a **D flip-flop** (10 points).

2. (Finite State Machine) A state machine is described by the following state equations.

$$Q_1(t+1) = Q_0(t),$$

$$Q_0(t+1) = Q_1'(t)x(t),$$

$$y(t) = Q_1(t)Q_0'(t)x(t).$$

2.1. Write the state table (10 points).

2.2. Design the system with two JK flip-flops. Describe $y(t)$, $J_1(t)$, $K_1(t)$, $J_0(t)$, $K_0(t)$ as functions of variables $(x, Q_1(t), Q_0(t))$ in minimal sum-of-products expressions. No need to draw the logic diagram (20 points).

2.3. Implement the system with a Moore machine with a minimal number of states.
(i) Use a state diagram to demonstrate the design. Label the initial state as S_0 (10 points).

(ii) Fill the following table as the machine starts at state S_0 and process through the given input x from CLK (Clock) sequence =1 to 10 (5 points).

3. (Timing and Retiming) For the following circuit, the timing characteristics of the components are summarized below. (25 points)

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 30\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 20\text{ps}$, setup time $t_{setup} = 20\text{ps}$, hold time $t_{hold} = 30\text{ps}$
- Logic gate (each AND, OR, XOR): propagation delay $t_{pd} = 25\text{ps}$, contamination delay $t_{cd} = 15\text{ps}$.

3.1. Suppose that there is no clock skew. What is the maximum clock frequency of this circuit?

3.2. How much clock skew can the circuit tolerate before it experiences a hold time violation?

4. (Decoders) Given two four-input Boolean functions

$$f_1(a, b, c, d) = \sum m(1, 2, 4, 7, 10) + \sum d(3),$$

$$f_2(a, b, c, d) = \sum m(0, 3, 5, 15) + \sum d(7),$$

implement the functions using a minimal network of 2:4 decoders and OR gates.

Describe the design with a logic diagram (20 points).

5. (Multiplexers) Given a three-input Boolean function

$$f(a, b, c) = \sum m(0, 2, 6, 7) + \sum d(4),$$

implement the function using a minimal network of 2:1 multiplexers. Describe the design with a logic diagram (20 points).