

1 True or False (15 points)

Circle your choice of true or false. Use one sentence to explain your choice.

- 3pts for correct answer
- 1.5pt for incorrect answer but reasonable explanation
- 0pt for incorrect answer without explanation or no attempt

1. The state table of SR latches has Don't Care entries when input $SR = 11$. Thus, we are allowed to feed input $SR = 11$.

False

The input SR cannot be 11 to avoid the invalid states.

2. For a D flip-flop, we use $D(t) = Q(t+1)$ to denote that the content of the flip-flop is updated according to the input signal after the rising edge of the clock.

True/False (depending on explanation)

When CLK rises from 0 to 1, D passes through to Q . Otherwise, Q holds its previous value.

∗: only different interpretation of the timing of edge-trigger receives full credits for choosing "False".

3. For digital circuits, it takes more than three clock cycles to propagate a signal over a 1 cm distance at 5GHz clock rate assuming that the circuit is slower than the speed of light by a factor of 10.

True/False (depending on explanation)

The distance that a signal can propagate within one clock cycle at 5GHz with speed $v = \frac{c}{\sqrt{\epsilon}} \frac{1}{10} = 1.5 \times 10^7 m/s$ is

$$d = \frac{v}{f} = \frac{1.5 \times 10^7}{5 \times 10^9} = 0.003m$$

So it takes more than 3 clock cycles to propagate a signal over 1cm.

∗: showing derivation of the calculation receives full credits for choosing "False".

4. For a Mealy machine, the timing of the output is independent of the input.

False

The output of a Mealy machine can be dependent of the input, but the output of a Moore machine is independent of the input.

5. For a sequential network, we need only to take care of the timing of the regions separated by the registers, e.g. regions between two registers, between primary input and registers, and between registers and primary output.

True/False (depending on explanation)

All the cases mentioned should be considered for timing.

∗: showing considerations on top of regions separations receives full credits for choosing "False".

3 Finite State Machine (30 points)

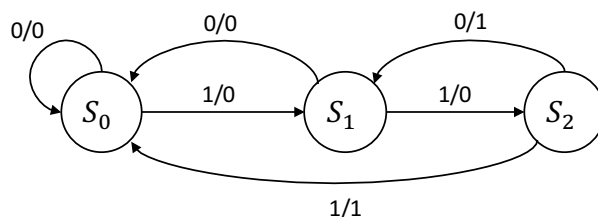
Given a state table as below, each entry of the table is the next state and output, i.e. $Q_1(t+1) Q_0(t+1), y$.

id	$Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	0 0	00,0	01,0
1	0 1	00,0	10,0
2	1 0	01,1	00,1

- 10pts for correct state diagram; 10pts for correct K-maps from excitation table; 10pts for correct expressions and logic diagram
- For 3.1 logic diagram, -2 pts for each missing input, output or state transition. Either using binary bits or state "S" is fine
- For 3.2 K-maps, -2 pts for each wrong K-map (totally 3 K-maps). If there is no K-map but a correct excitation table, gives 5pts; if there is only one incorrect excitation table, gives 2pts; 0pt for no attempt.
- For 3.2 minimal expressions, -2 pts for each wrong expression (totally 3 expressions and 6 pts).
- For the logic diagram, 2pts for correctly using D Flip-Flop and 2 pts for correct combinational logic; adjustable deduction 1-2 pts for any missing terms or incorrect implementation depending on wrong expressions. 0pt for no attempt.

1 Draw the state diagram.

If we assign states $S_0 = 00, S_1 = 01, S_2 = 10$, the corresponding state diagram is as follows



2 Design the state machine with 2 D flip-flops. Show the K-maps and the logic diagram with minimal expressions.

The excitation table is derived from the state table. Since we are using D Flip-Flops to design the state machine, the state expressions for the 2 D Flip-Flops are

$$D_1(t) = Q_1(t+1)$$

$$D_0(t) = Q_0(t+1)$$

id	$Q_1(t)$	$Q_0(t)$	$x(t)$	$Q_1(t+1)$	$Q_0(t+1)$	$y(t)$
0	0	0	0	0	0	0
1	0	0	1	0	1	0
2	0	1	0	0	0	0
3	0	1	1	1	0	0
4	1	0	0	0	1	1
5	1	0	1	0	0	1
6	1	1	0	X	X	X
7	1	1	1	X	X	X

K-maps are used to simplify the expression. With the following K-map for $D_1(t)$, we have $D_1(t) = Q_0(t)X(t)$.

$X(t) \setminus Q_1(t)Q_0(t)$	00	01	11	10
0	0 ₀	0 ₂	X ₆	0 ₄
1	0 ₁	1 ₃	X ₇	0 ₅

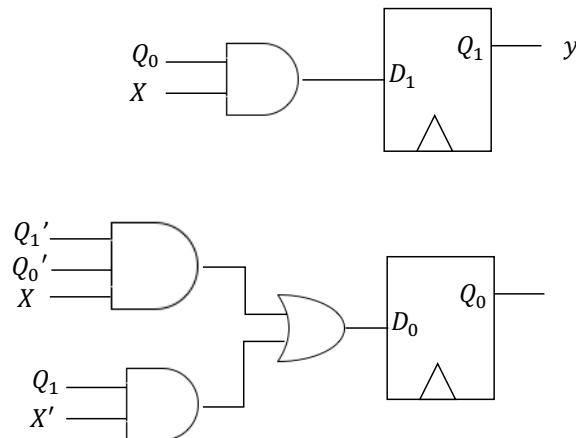
For $D_0(t)$, we have $D_0(t) = Q_1'(t)Q_0'(t)X(t) + Q_1(t)X'(t)$.

$X(t) \setminus Q_1(t)Q_0(t)$	00	01	11	10
0	0 ₀	0 ₂	X ₆	1 ₄
1	1 ₁	0 ₃	X ₇	0 ₅

For $y(t)$, we have $y(t) = Q_1(t)$.

$X(t) \setminus Q_1(t)Q_0(t)$	00	01	11	10
0	0 ₀	0 ₂	X ₆	1 ₄
1	0 ₁	0 ₃	X ₇	1 ₅

The logic diagram



4 Mealy and Moore Machine Conversion (25 points)

Given a state table as below, each entry of the table is the next state and output, i.e. $Q_1(t+1) Q_0(t+1), y$.

id	$Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	0 0	10,0	01,0
1	0 1	00,0	10,0
2	1 0	01,1	11,0
3	1 1	00,0	10,1

- For 4.1, 5pts for correct outputs; -1pt for each error in y
- For 4.2, 15pts for correct state table with Moore machine (including 5pts for each extra state/output, 2.5pts for each transition/output from existing states to new states); -2.5pts for missing output column but correct outputs in 4.3; -7.5pts if there is no state table but a state diagram
- For 4.3, 5 pts for correct outputs; -1pt for each error in y ; -2.5pts for incorrect answer but consistent to state table in 4.2

1 Fill the following table as the machine starts at state $Q_1(t=1) Q_0(t=1) = 00$ and process through the given input x from CLK (Clock) sequence =1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	1	1	1	1	0	1	1	0	1	1
state	00	01	10	11	10	01	10	11	00	01
y	0	0	0	1	1	0	0	0	0	0

2 Convert the above machine into a Moore machine. Write the state table.

We need 3bits to encode all the states. Either using binary bits or state symbol S is fine.

id	$Q_2(t) Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$	$y(t)$
0	0 0 0	010	001	0
1	0 0 1	000	010	0
2	0 1 0	100	011	0
3	0 1 1	000	101	0
4	1 0 0	000	010	1
5	1 0 1	100	011	1

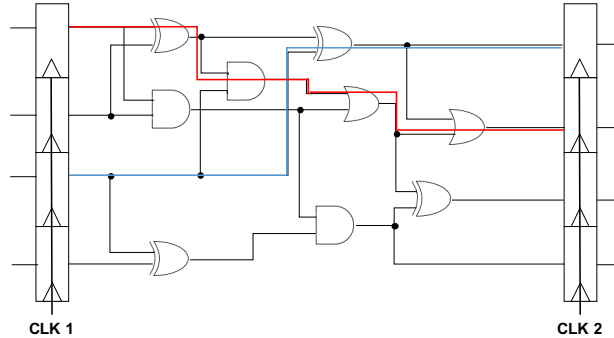
3 Use the Moore machine to fill the table starting at state $Q_1(t=1) Q_0(t=1) = 00$ and process through the given input x from CLK (Clock) sequence 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	1	1	1	1	0	1	1	0	1	1
state	000	001	010	011	101	100	010	011	000	001
y	0	0	0	0	1	1	0	0	0	0

5 Timing and Retiming (20 points)

For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 30\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 20\text{ps}$, setup time $t_{setup} = 20\text{ps}$, hold time $t_{hold} = 50\text{ps}$
- Logic gate (each AND, OR, XOR): propagation delay $t_{pd}(\text{gate}) = 30\text{ps}$, contamination delay $t_{cd}(\text{gate}) = 15\text{ps}$.



- For 5.1, 5pts for each correct expression; 0pt for no attempt
- For 5.2, 5pts for correct answer; -2.5pts for incorrect answer due to wrong $t_{pd(max)}$
- For 5.3, 5pts for correct answer; -2.5pts for incorrect answer due to wrong $t_{cd(min)}$
- 0pt for completely incorrect answers or no attempt

1. Write the expressions of the setup time constraint and the hold time constraint. Use the symbol T : clock period, and $t_{cd}(com)$, $t_{pd}(com)$: the contamination delay and the propagation delay of the combination logic, respectively.

Setup time constraint:

$$T_c \geq t_{pcq} + t_{pd}(com) + t_{setup}$$

Hold time constraint:

$$t_{ccq} + t_{cd}(com) \geq t_{hold}$$

2. Derive the minimal clock period T , suppose that there is no clock skew.

The longest path of combinational logic between 2 flip-flops passes 4 logic gates.

$$t_{pd(max)} = 4 \times t_{pd(gate)} = 120\text{ps}$$

The clock period should satisfy the setup time constraint

$$T_c \geq t_{pcq} + t_{pd(max)} + t_{setup} = 30 + 120 + 20 = 170\text{ps}$$

So the minimal clock period is $170ps$.

3. Suppose that we utilize the designated clock skew, t_{skew} , to reduce the clock period. What is the minimal clock period, T and the corresponding skew t_{skew} ?

The minimum contamination delay of the combinational logic passes one logic gate.

$$t_{cd(min)} = 1 \times t_{cd(gate)} = 15ps$$

Consider clock skew, the hold time constraint gives

$$t_{ccq} + t_{cd(min)} = 20 + 15 = 35ps \geq t_{hold} + t_{skew} = 50 + t_{skew}$$

So $t_{skew} \leq 35 - 50 = -15ps$. There exists a hold time violation.

If we use a clock skew $t_{skew} = -15ps$ to fix the hold time violation, we cannot improve the performance because the clock period is increased.

$$T_c \geq t_{pcq} + t_{pd(max)} + t_{setup} - t_{skew} = 185ps$$