

## 1 True or False (15 points)

Circle your choice of true or false. Use one sentence to explain your choice.

1. The state table of SR latches has Don't Care entries when input  $SR = 11$ . Thus, we are allowed to feed input  $SR = 11$ .

True False

Explanation:

2. For a D flip-flop, we use  $D(t) = Q(t+1)$  to denote that the content of the flip-flop is updated according to the input signal after the rising edge of the clock.

True False

Explanation:

3. For digital circuits, it takes more than three clock cycles to propagate a signal over a 1 cm distance at 5GHz clock rate assuming that the circuit is slower than the speed of light by a factor of 10.

True False

Explanation:

4. For a Mealy machine, the timing of the output is independent of the input.

True False

Explanation:

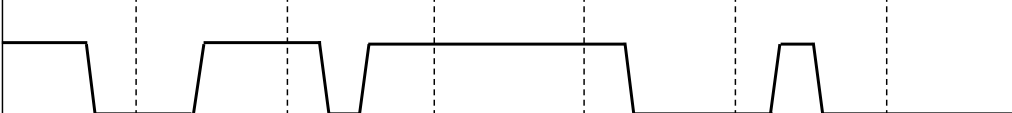
5. For a sequential network, we need only to take care of the timing of the regions separated by the registers, e.g. regions between two registers, between primary input and registers, and between registers and primary output.

True False

Explanation:

## 2 Timing Diagram of Latch and Flip-Flop (10 points)

Given the input waveforms shown below, sketch the output, Q of a **D latch**, and Q of a **D flip-flop**.

|                 |                                                                                    |
|-----------------|------------------------------------------------------------------------------------|
| clk             |  |
| D               |  |
| Q (D-latch)     |                                                                                    |
| Q (D Flip-Flop) |                                                                                    |

**3 Finite State Machine (30 points)**

Given a state table as below, each entry of the table is the next state and output, i.e.  $Q_1(t+1) Q_0(t+1), y$ .

| $id$ | $Q_1(t) Q_0(t)$ | $x(t) = 0$ | $x(t) = 1$ |
|------|-----------------|------------|------------|
| 0    | 0 0             | 00,0       | 01,0       |
| 1    | 0 1             | 00,0       | 10,0       |
| 2    | 1 0             | 01,1       | 00,1       |

1 Draw the state diagram.

2 Design the state machine with 2 D flip-flops. Show the K-maps and the logic diagram with minimal expressions.

**4 Mealy and Moore Machine Conversion (25 points)**

Given a state table as below, each entry of the table is the next state and output, i.e.  $Q_1(t+1) Q_0(t+1), y$ .

| $id$ | $Q_1(t) Q_0(t)$ | $x(t) = 0$ | $x(t) = 1$ |
|------|-----------------|------------|------------|
| 0    | 0 0             | 10,0       | 01,0       |
| 1    | 0 1             | 00,0       | 10,0       |
| 2    | 1 0             | 01,1       | 11,0       |
| 3    | 1 1             | 00,0       | 10,1       |

1 Fill the following table as the machine starts at state  $Q_1(t=1) Q_0(t=1) = 00$  and process through the given input  $x$  from CLK (Clock) sequence =1 to 10.

| CLK   | 1  | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|-------|----|---|---|---|---|---|---|---|---|----|
| $x$   | 1  | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1  |
| state | 00 |   |   |   |   |   |   |   |   |    |
| $y$   |    |   |   |   |   |   |   |   |   |    |

2 Convert the above machine into a Moore machine. Write the state table. the given input  $x$  from CLK (Clock) sequence =1 to 10.

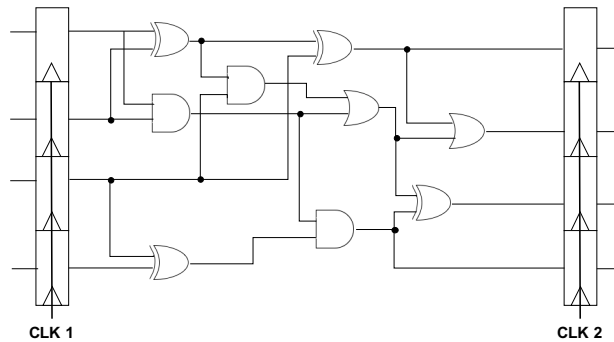
3 Use the Moore machine to fill the table starting at state  $Q_1(t=1) Q_0(t=1) = 00$  and process through the given input  $x$  from CLK (Clock) sequence 1 to 10.

| CLK   | 1  | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|-------|----|---|---|---|---|---|---|---|---|----|
| $x$   | 1  | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1  |
| state | 00 |   |   |   |   |   |   |   |   |    |
| $y$   |    |   |   |   |   |   |   |   |   |    |

## 5 Timing and Retiming (20 points)

For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay)  $t_{pcq} = 30\text{ps}$ , clock-to-Q minimum delay (contamination delay)  $t_{ccq} = 20\text{ps}$ , setup time  $t_{setup} = 20\text{ps}$ , hold time  $t_{hold} = 50\text{ps}$
- Logic gate (each AND, OR, XOR): propagation delay  $t_{pd}(gate) = 30\text{ps}$ , contamination delay  $t_{cd}(gate) = 15\text{ps}$ .



1. Write the expressions of the setup time constraint and the hold time constraint. Use the symbol  $T$ : clock period, and  $t_{cd}(com)$ ,  $t_{pd}(com)$ : the contamination delay and the propagation delay of the combination logic, respectively.
2. Derive the minimal clock period  $T$ , suppose that there is no clock skew.
3. Suppose that we utilize the designated clock skew,  $t_{skew}$ , to reduce the clock period. What is the minimal clock period,  $T$  and the corresponding skew  $t_{skew}$ ?