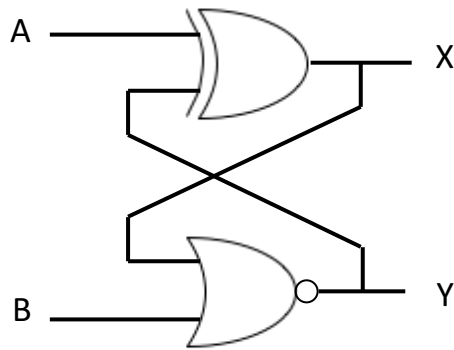


1 SR Latches (25 points)

We revise a two-NOR SR latch by replacing a NOR gate with an XOR gate, i.e. $f(x, y) = x'y + xy'$ as follows. Complete the state table.



<i>id</i>	<i>A</i>	<i>B</i>	<i>X_t</i>	<i>Y_t</i>	<i>X_{t+1}</i>	<i>Y_{t+1}</i>	<i>X_{t+2}</i>	<i>Y_{t+2}</i>	<i>X_{t+3}</i>	<i>Y_{t+3}</i>
0	0	0	0	0						
1	0	0	0	1						
2	0	0	1	0						
3	0	0	1	1						
4	0	1	0	0						
5	0	1	0	1						
6	0	1	1	0						
7	0	1	1	1						
8	1	0	0	0						
9	1	0	0	1						
10	1	0	1	0						
11	1	0	1	1						
12	1	1	0	0						
13	1	1	0	1						
14	1	1	1	0						
15	1	1	1	1						

2 Finite State Machine (30 points)

A pattern recognizer inputs a string of binary bits $x(t)$ and outputs $y(t) = 1$ whenever $x(t-2, t) = 011$ or 010 ; $y(t) = 0$ otherwise.

1. Design the state machine with less than 4 states. Draw the state diagram.
2. Design the state machine with 2 D flip-flops. Write the state table.
3. Design the system with two D flip-flops. Describe $y(t), D_1(t), D_0(t)$ as functions of variables $(x, Q_1(t), Q_0(t))$ in minimal sum-of-products expressions. No need to draw the logic diagram.

3 Mealy and Moore Machine Conversion (20 points)

Given a state table as below, each entry of the table is the next state and output, i.e. $Q_1(t+1) Q_0(t+1), y$.

id	$Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	0 0	00,0	01,0
1	0 1	00,0	10,0
2	1 0	01,1	11,0
3	1 1	00,1	10,0

- Fill the following table as the machine starts at state $Q_1(t=1) Q_0(t=1) = 00$ and process through the given input x from CLK (Clock) sequence =1 to 8.

CLK	1	2	3	4	5	6	7	8
x	1	0	1	1	0	1	1	1
state	00							
y								

- Convert the above machine into a Moore machine. Write the state table. the given input x from CLK (Clock) sequence =1 to 10.

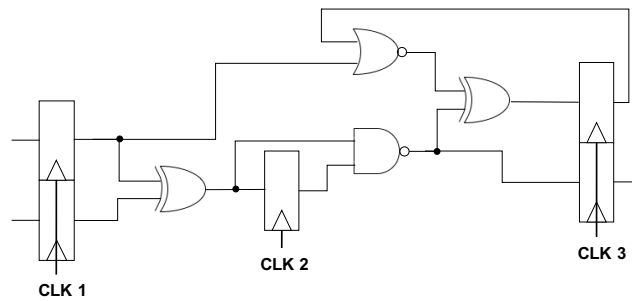
- Use the Moore machine to fill the table starting at state $Q_1(t=1) Q_0(t=1) = 00$ and process through the given input x from CLK (Clock) sequence 1 to 10.

CLK	1	2	3	4	5	6	7	8
x	1	0	1	1	0	1	1	1
state	00							
y								

4 Timing and Retiming (25 points)

For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 30\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 20\text{ps}$, setup time $t_{setup} = 20\text{ps}$, hold time $t_{hold} = 30\text{ps}$
- Logic gate (each AND, OR, XOR): propagation delay $t_{pd}(\text{gate}) = 25\text{ps}$, contamination delay $t_{cd}(\text{gate}) = 15\text{ps}$.



1. Derive the minimal clock period T , suppose that there is no clock skew.
2. How much clock skew can the circuit tolerate before it experiences a hold time violation?