

CSE 140 Spring 2017: Final, Due 10PM 6/15/2017

This is an open book final. The exam contains **four problems**. Web searches are encouraged. If there is any uncertainty about the problems, make and state your assumptions. Each person is supposed to work by oneself. Thus, no discussion is allowed.

1. (Boolean Algebra) Prove the following Boolean theorem using Boolean laws only, i.e. no theorem is allowed for the proof. State the name of the law for each step of your proof.

$$x + 1 = 1 \tag{1}$$

2. (Switching Function) A set of switching variables a, b, c, d, e has the values defined by the following simultaneous switching equations.

$$a + b + c = 1 \tag{2}$$

$$b' + c' + d = 1 \tag{3}$$

$$c + d' + e = 1 \tag{4}$$

$$a + c + e' = 1 \tag{5}$$

$$a' + b' + d = 1 \tag{6}$$

Use a switching function $f(a, b, c, d, e)$ to cover the values of the variables as its On-Set F . In other words, a min-term m_i belongs to F if and only if the corresponding binary code $(a, b, c, d, e) = i$ satisfies the above equations.

2.1 Check which of the following min-terms belong to On-Set F .

$$m_0, m_5, m_{10}, m_{15}, m_{30}. \tag{7}$$

2.2 Express function $f(a, b, c, d, e)$ in a minimal sum of products form. Describe the number of product terms and the number of literals.

3. (Retiming) Check the digital correlator circuit in paper, C. Leiserson and J. Saxe, "Retiming Synchronous Circuitry," *Algorithmica*, pp. 6:5-35, 1991. (The paper is posted with the exam. You are encouraged to read the approaches and references of the paper, but it is not required.) Suppose that each comparator δ propagation delay is changed to 10 picosecond and each adder + propagation delay is changed to 50 picosecond (changed from the numbers in the paper).

3.1 For the digital correlator circuit in figure 1 of the paper, what is the clock period of the circuit (the delay of a longest path of combinational rippling)?

3.2 For the circuit in figure 2 of the paper, what is the clock period of the circuit (the delay of a longest path of combinational rippling)?

3.3 For the same path between figure 1 and figure 2, that starts from and loops back to the Host, the loop traverses the same number of registers. Explain that the host

should experience the same responses from the two circuits in figures 1 and 2. State your explanation in no more than four sentences.

3.4 With aggressive retiming, what is the minimal clock period that can be achieved for the digital correlator in this paper? Hint: check figures 3 and 4 of the paper.

4. (System Designs) Follow the style of the routine *Multiple* in slide 5 of lecture 14 to describe your design. Suppose that module *Multiple*($X, Y, Z, start, done$) is used for the multiplication operation. Design a system that inputs a 3-bit binary number n and outputs its factorial $n!$.

4.1. Write the program. Explain the interface with module *Multiple*($X, Y, Z, start, done$).

4.2. Describe the data subsystem with a schematic diagram. You can treat module *Multiple*($X, Y, Z, start, done$) as a black box.

4.3. Draw the state diagram of the control subsystem and describe the control signals using a truth table.