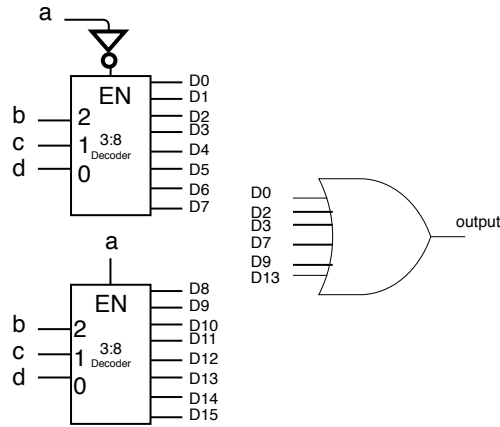


(I) (Standard Interconnect Modules) Assume a dual-railed system, where you have access to any variable and its complement. Given a four-input Boolean function

$$f(a, b, c, d) = \sum m(0, 2, 3, 7, 9, 13) + \sum d(1, 5, 8, 14).$$

I.1. Implement the function using a minimal network of 3:8 decoders and OR gates by drawing the logic diagram. (10 points)



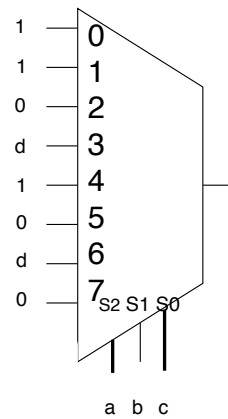
Grading Rubrics for (I.1)

10 points for correct answer

- -1 point for each wrong labeling of one box (decoder and OR gate)
- -1 point for missing / extra wires / connection
- -5 points for using wrong number of decoders, or not using 3:8 decoder
- -2 points for not having a minimal network of OR Gates (based on the number of inputs used)

I.2 Implement the function using a minimal network of 8:1 multiplexers by drawing the logic diagram. (10 points)

abc	$d = 0$	$d = 1$	$l(d)$
000	1	X	$l(d) = 1, d'$
001	1	1	$l(d) = 1$
010	0	X	$l(d) = 0, d$
011	0	1	$l(d) = d$
100	X	1	$l(d) = 1, d$
101	0	0	$l(d) = 0$
110	0	1	$l(d) = d$
111	X	0	$l(d) = 0, d'$



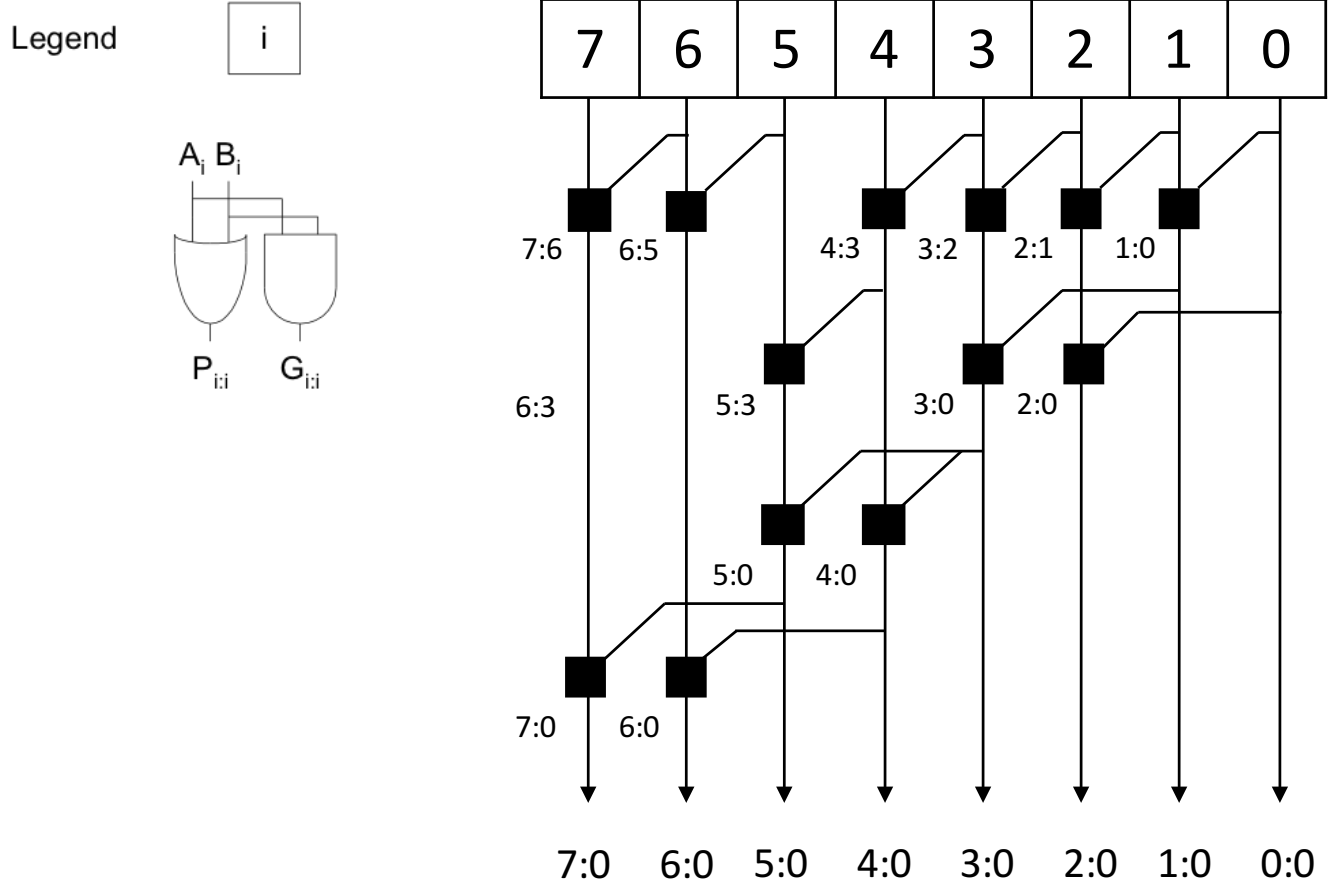
Grading Rubrics for (I.2)

10 points for correct answer

- -1 point for each wrong labeling of MUX
- -1 point for missing / extra wires / connection
- -5 points for using wrong number of MUX or different MUX instead of 8:1 MUX
- -10 points for relying on an enable to solve the problem

(II) (Standard Logic Modules) Manually simulate the operation of the following logic modules.

II.1. For the prefix adder as below, manually simulate the addition of 28 and 14. Write the value of $(P_{i,j}, G_{i,j})$ output of each black box. Show the sum $S_i = A_i \oplus B_i \oplus G_{i-1,-1}$. Write the value directly on the schematic diagram. (10 points)



i	7	6	5	4	3	2	1	0
28	0	0	0	1	1	1	0	0
14	0	0	0	0	1	1	1	0
$i : i$	7 : 7	6 : 6	5 : 5	4 : 4	3 : 3	2 : 2	1 : 1	0 : 0
(p, g)	(0,0)	(0,0)	(0,0)	(1,0)	(1,1)	(1,1)	(1,0)	(0,0)
$i : j$	7 : 6	6 : 5		4 : 3	3 : 2	2 : 1	1 : 0	
(p, g)	(0,0)	(0,0)		(1,1)	(1,1)	(1,1)	(0,0)	
$i : j$			5 : 3		3 : 0	2 : 0		
(p, g)			(0,0)		(0,1)	(0,1)		
$i : j$	7 : 0	6 : 0	5 : 0	4 : 0				
(p, g)	(0,0)	(0,0)	(0,0)	(0,1)				
s_i	0	0	1	0	1	0	1	0

Grading Rubrics for (II.1)

10 points for correct answer

- -0.5 point for each wrong $(P_{i,j}, G_{i,j})$
- -0.5 point for each wrong S_i
-

II.2. Given an eight bit carry save adder, manually simulate the addition of four numbers: $n_1 = 11$, $n_2 = 17$, $n_3 = 9$, $n_4 = 12$. Write the results in the following table. Note that the end of the table has *Total* represented in nonredundant binary code. (10 points)

id	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
n_1	00	00	00	00	10	00	10	10
n_2	0	0	0	1	0	0	0	1
$A = n_1 + n_2$	00	00	00	10	10	00	11	00
n_3	0	0	0	0	1	0	0	1
$B = A + n_3$	00	00	00	11	00	01	00	10
n_4	0	0	0	0	1	1	0	0
$C = B + n_4$	00	00	01	00	11	00	00	10
<i>Total</i>	0	0	1	1	0	0	0	1

Grading Rubrics for (II.2)

10 points for correct answer

- -0.5 point for each wrong entry
-

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III. A sequential subtractor inputs x_i, y_i , the i 'th bit of two binary numbers in each clock cycle for $i = 0$ to $n - 1$ and outputs the difference d_i . Implement the subtractor with a D flip-flop, and minimal networks of logic (AND, OR, NOT, XOR) gates. (15 points)

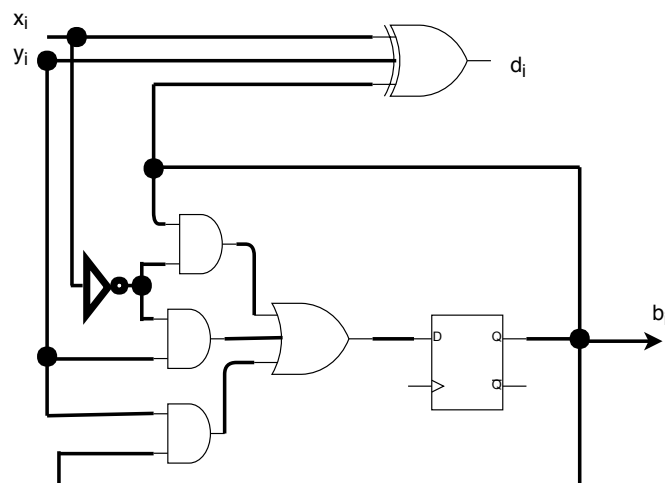
III.1. Write the state table to describe the next states and outputs as functions of present state and inputs.

x_i	y_i	b_i	b_{i+1}	d_i
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

III.2. Draw the schematic diagram.

$$d_i = x_i \oplus y_i \oplus b_i$$

$$b_{i+1} = x'_i y_i + x'_i b_i + y_i b_i$$



Grading Rubrics for (III)

15 points for correct answer

- 8 points for the table, 7 points for the diagram
- -1 point for each wrong row of the state table
- -4 points for missing borrow bits or difference bit
- -1 point for each missing/incorrect/extra component (three major component: Register, Difference Bit combinational circuit, B_{out} combinational circuit)
- -0.5 point for each missing label inside the register
- -1 point for not minimal: use more than 4 gates for B_{out} combinational circuit (4 gates is minimal) or more than 2 gates in Difference Bit combinational circuit (one 3-input XOR or two 2-input XOR is minimal).
- -4 points if part 1 only have 4 rows and part 2 is correct based on part 1
- -7 points if implement a Borrow look ahead subtractor instead
- -0.5 point for each wrong label of the serial subtractor
- -0.5 point for each missing component of the serial subtractor
- -5 points for the schematic diagram based on the wrong equations
- -3 points for using the subtractor directly

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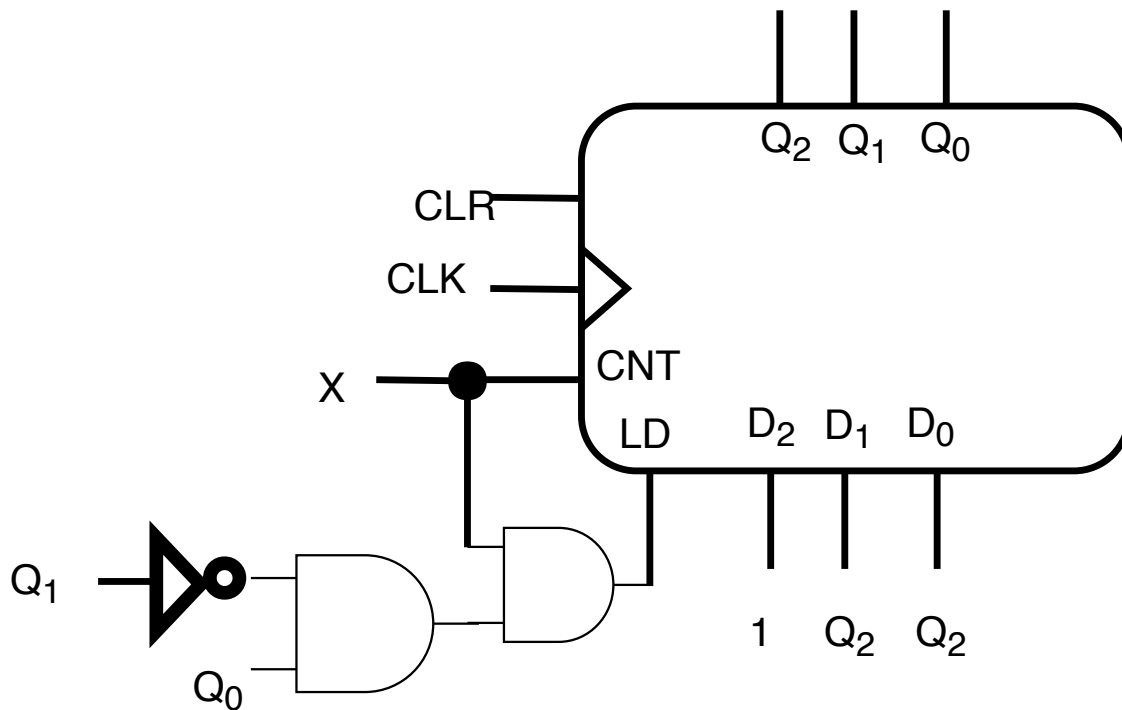
IV. Counter: Given a modulo 8 counter, construct a counter that counts in sequence 0, 1, 4, 5, 7 with minimal networks of AND, OR gates. (15 points)

IV.1. Write the truth table to describe the load LD , and (D_2, D_1, D_0) as functions of present state (Q_2, Q_1, Q_0) .

When $Q=1$, load $D=4$ When $Q=5$, load $D=7$

id	$Q_2Q_1Q_0$	Ld	D_2	D_1	D_0
0	000	0	—	—	—
1	001	1	1	0	0
2	010	—	—	—	—
3	011	—	—	—	—
4	100	0	—	—	—
5	101	1	1	1	1
6	110	—	—	—	—
7	111	0	—	—	—

IV.2. Draw the schematic diagram.



Grading Rubrics for (IV)

10 points for correct answer

- 8 points for the table, 7 points for the diagram
- -1 point for each incorrect row
- -1 point for wrong input to D0, D1, or D2
- -2 points for incorrect circuit as input to LD signal
- -1 point if correct gates but one wrong input
- -1 point if correct input but wrong gates
- -1 point if missing one of the second AND gate (for x AND Q1Q0)
- -0.5 point for each missing label amongst D0, D1, D2, CNT, LD, Q2, Q1, Q0 (max of -2 points)
- -7points for only giving equations or drawing only the circuit diagram without the counter schematic.

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(V). (System Designs) Implement the following algorithm:

```

Alg(X, Y, Z, start, W, done);
Input X[7:0], Y[7:0], Z[7:0], start;
Output W[7:0], done;
Local-object A[7:0], B[7:0], C[7:0];
S0: If start' goto S0 || done  $\leftarrow$  1;
S1: A  $\leftarrow$  X || B  $\leftarrow$  Y || C  $\leftarrow$  Z || done  $\leftarrow$  0;
S2: if (A[7]) goto S5 || B  $\leftarrow$  B+C;
S3: A  $\leftarrow$  A+B;
S4: if C'[7] goto S2 || C  $\leftarrow$  Inc(C);
S5: A  $\leftarrow$  Inc(A) || if C[7] goto S2;
S6: W  $\leftarrow$  C || goto S0;
End Alg

```

V.1. Design a data subsystem that is adequate to execute the algorithm by answering the following questions. (15 points)

V.1.1. Use a table to list the instructions and the corresponding components that should be used in the data path subsystem.

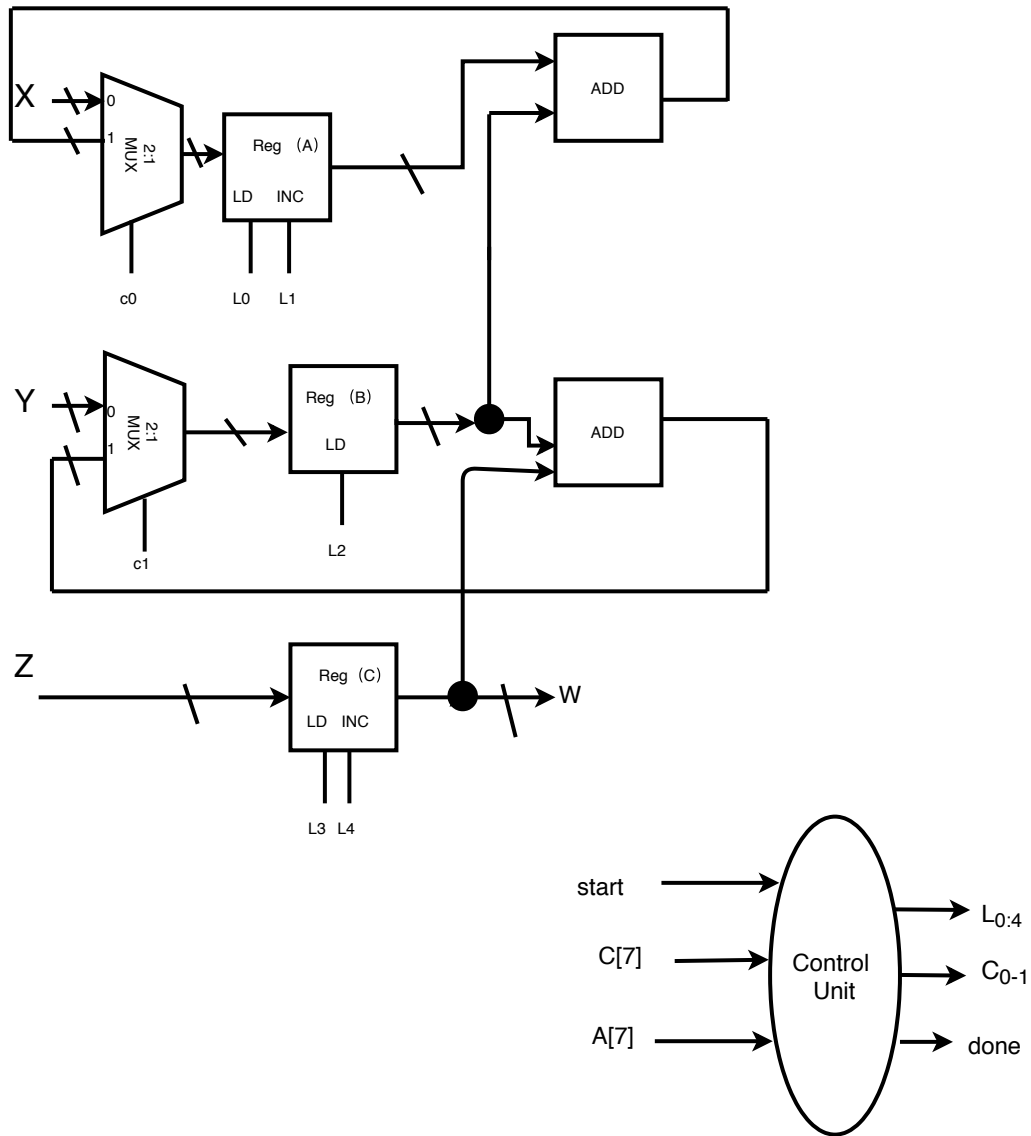
Required components that should be listed:

state	Instruction	Operation
S1	A $\leftarrow$ X	A $\leftarrow$ Load(X)
S1	B $\leftarrow$ Y	B $\leftarrow$ Load(Y)
S1	C $\leftarrow$ Z	C $\leftarrow$ Load(Z)
S2	B $\leftarrow$ B+C	B $\leftarrow$ Add(B,C)
S3	A $\leftarrow$ A+B	A $\leftarrow$ Add(A,B)
S4	C $\leftarrow$ Inc(C)	C $\leftarrow$ Inc(C)
S5	A $\leftarrow$ Inc(A)	A $\leftarrow$ Inc(A)

Other components that can be listed: (no points deducted without showing the components in the table below)

state	Instruction	Operation
S0	done $\leftarrow$ 1	
S6	W $\leftarrow$ C	Wire

V.1.2. Draw the schematic diagram to show the data path subsystem. Label the inputs, outputs, and control signals of all components.



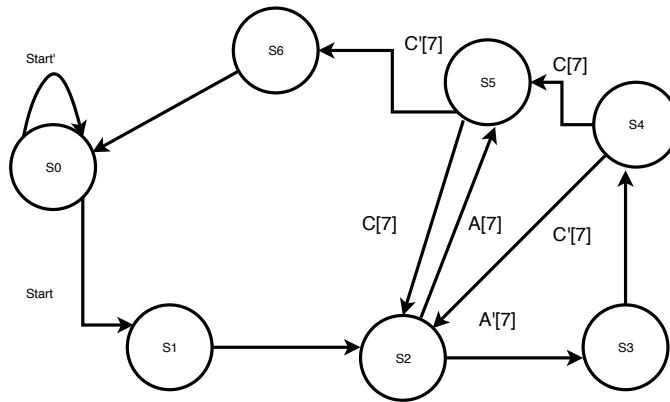
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V.2. Design the control subsystem by answering the following questions. (15 points)

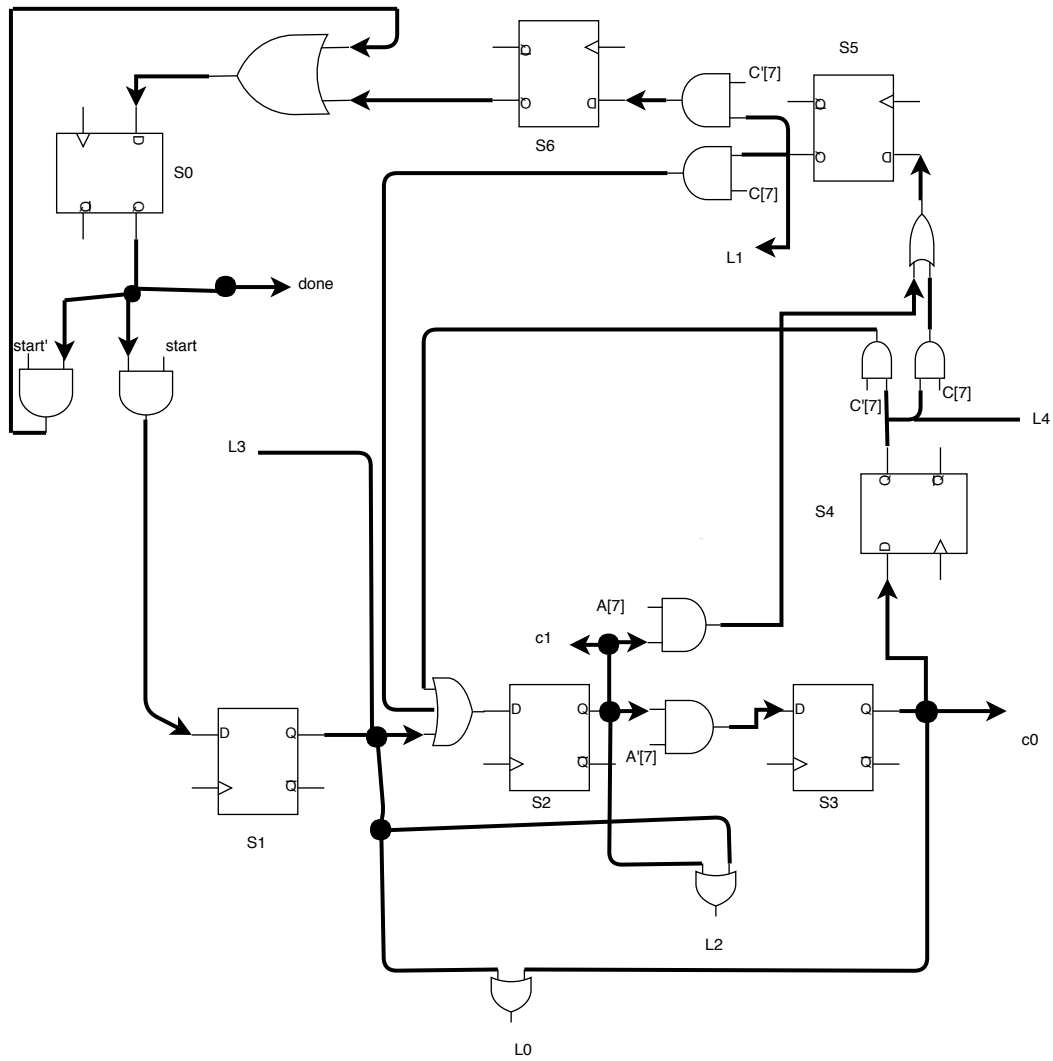
V.2.1. Use a table to list the value of control signals for every state.

<i>state</i>	<i>L0</i>	<i>L1</i>	<i>L2</i>	<i>L3</i>	<i>L4</i>	<i>c0</i>	<i>c1</i>	done
<i>S0</i>	0	0	0	0	0	-	-	1
<i>S1</i>	1	0	1	1	0	0	0	0
<i>S2</i>	0	0	1	0	0	-	1	0
<i>S3</i>	1	0	0	0	0	1	-	0
<i>S4</i>	0	0	0	0	1	-	-	0
<i>S5</i>	0	1	0	0	0	-	-	0
<i>S6</i>	0	0	0	0	0	-	-	0

V.2.2. Draw the state diagram.



V.2.3. Implement the control subsystem using a one hot encoding design. Draw the logic diagram.



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Grading Rubrics for (V.1.1)

7 points for correct answer

- -1 point for each wrong row of the table
- state column is optional

Grading Rubrics for (V.1.2)

8 points for correct answer (different people may have different designs)

- -0.5 point for each wrong label
- -1 point for each missing operation
- -0.5 point for each missing / extra connection / component
- the control unit is optional

Grading Rubrics for (V.2.1)

5 points for correct answer (different people may have different designs)

- -0.5 point for each wrong row
- if a specific control signal is missing / wrong, -0.5 for that signal

Grading Rubrics for (V.2.2)

5 points for correct answer (different people may have different designs)

- -0.5 point for each wrong transition
- -0.5 point for each missing condition
- -0.5 point for each missing state

Grading Rubrics for (V.2.3)

5 points for correct answer (different people may have different designs)

- -0.5 point for each missing / wrong logic gate
- -0.5 point for each wrong wire
- -0.5 point for missing label (capped at -2 if more than 4 missing label)
- -0.5 point for each missing state
- Same deduction as 5.2.2 if the answer is only correct based on previous answer.
- control unit's outputs are optional