

CSE140 - HW #3 Solution

Due Thursday February 4, 11:59PM

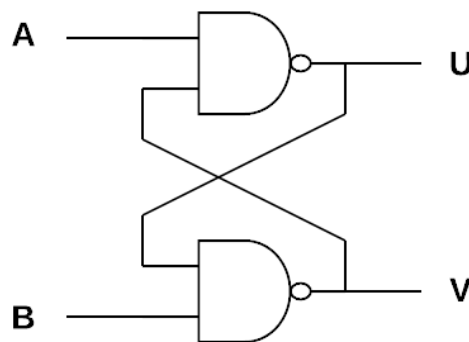
1 Introduction

The purpose of this assignment is to get a better understanding of basic memory elements and analysis of sequential circuits. In the first problem, we learn to analyze circuits with feedback loops. In the second problem we draw a timing diagram for D-latch and D-flip-flop. In the third problem, we translate a pattern recognizer into state diagrams and state tables. Finally, in the fourth problem, we analyze the behavior of a sequential circuit.

2 Latch

I. Given a SR latch of NOR gates, replace the two NOR gates with two NAND gates. Analyze the revised circuit. **(15 Points for completion)**

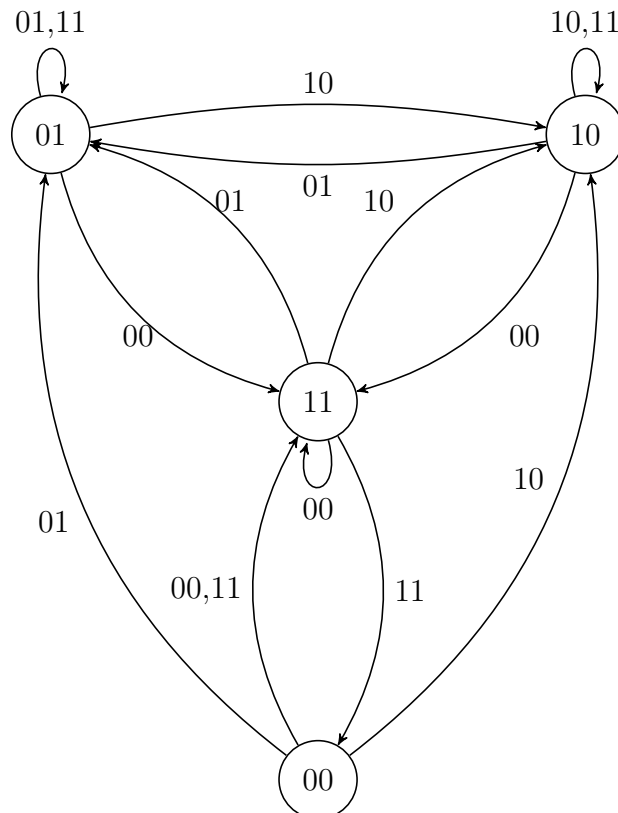
1. Write the truth table at times t_1 , t_2 and t_3 as the table in slide 17 of lecture 7. Here is the new circuit where we have changed the pin names to avoid confusion.



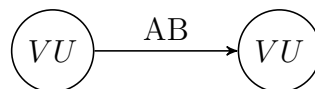
So, we can write the truth table:

id	A	B	$V(t_0)$	$U(t_0)$	$V(t_1)$	$U(t_1)$	$V(t_2)$	$U(t_2)$	$V(t_3)$	$U(t_3)$
0	0	0	0	0	1	1	1	1	1	1
1	0	0	0	1	1	1	1	1	1	1
2	0	0	1	0	1	1	1	1	1	1
3	0	0	1	1	1	1	1	1	1	1
4	0	1	0	0	1	1	0	1	0	1
5	0	1	0	1	0	1	0	1	0	1
6	0	1	1	0	1	1	0	1	0	1
7	0	1	1	1	0	1	0	1	0	1
8	1	0	0	0	1	1	1	0	1	0
9	1	0	0	1	1	1	1	0	1	0
10	1	0	1	0	1	0	1	0	1	0
11	1	0	1	1	1	0	1	0	1	0
12	1	1	0	0	1	1	0	0	1	1
13	1	1	0	1	0	1	0	1	0	1
14	1	1	1	0	1	0	1	0	1	0
15	1	1	1	1	0	0	1	1	0	0

2. Draw the state diagram.



Note that each node represents a state (VU) and the edges are inputs (AB):



Like the SR latch with NOR gates, we want the circuit to remain in the top two states in the diagram (01 and 10). We can achieve that by avoiding the input $AB = 00$. Assuming that, we can write the following state table for the circuit where we have organized the columns so that it can also be used as a K-map to derive the characteristic expression.

		$A(t)B(t)$			
		00	01	11	10
$U(t)$	0	-	1	0	0
	1	-	1	1	0

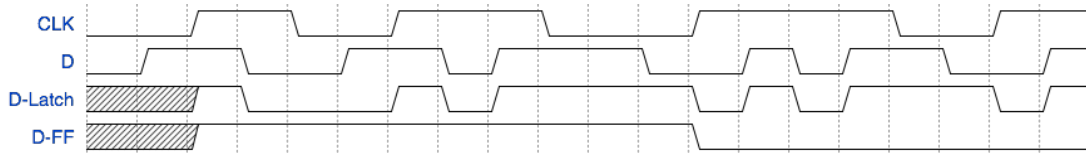
II. Replace the two NOR gates of the SR latch in problem I with two XNOR gates, i.e. $f(x, y) = xy + x'y'$. **(20 Points for correctness)**

Write the truth table at times t_1 , t_2 and t_3 as the table in slide 17 of lecture 7.

[illegible]

3 Timing Diagram of Latch and Flip-Flop

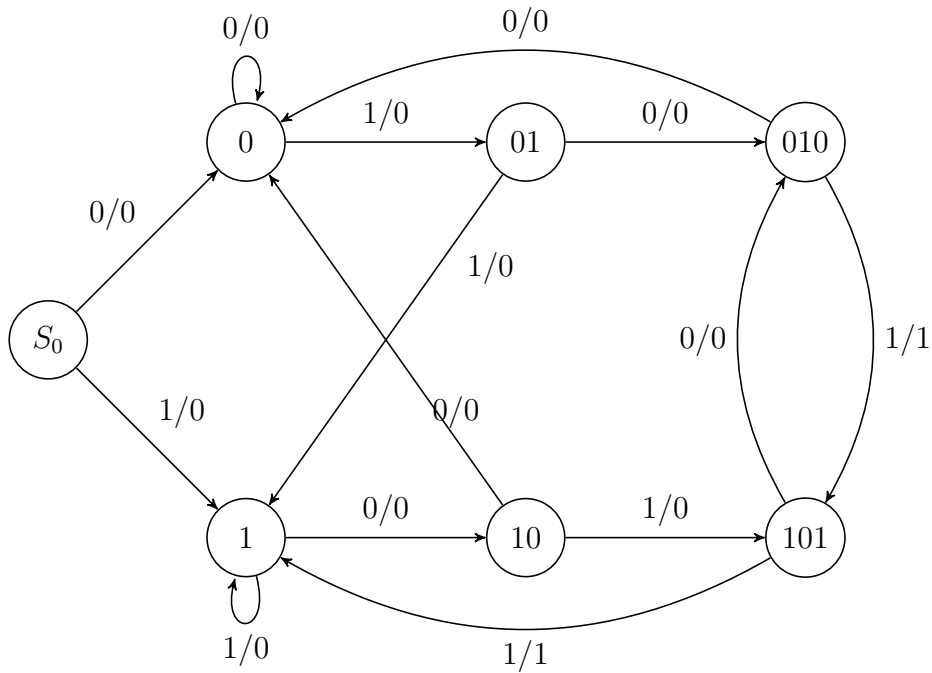
Given the input waveforms shown below, sketch the outputs. **(20 Points for correctness)**



4 Pattern Recognizer

A sequential network has one binary input $x(t)$ and one binary output $y(t)$. The network produces $y = 1$, whenever input pattern $x(t-3, t) = 0101$ or 1011 . Otherwise, the output $y = 0$.

(i) Draw the state diagram. **(20 Points for correctness)**



(ii) Write the state table. **(10 Points for completion)**

$PS - Input$	$x = 0$	$x = 1$
S_0	$S_1, 0$	$S_2, 0$
$S_1 = 0$	$S_1, 0$	$S_3, 0$
$S_2 = 1$	$S_4, 0$	$S_2, 0$
$S_3 = 01$	$S_5, 0$	$S_2, 0$
$S_4 = 10$	$S_1, 0$	$S_6, 0$
$S_5 = 010$	$S_1, 0$	$S_6, 1$
$S_6 = 101$	$S_5, 0$	$S_2, 1$

5 Sequential Circuit Analysis

Given a state machine has one input $x(t)$ and two-bit state $(Q_1(t), Q_0(t))$. The machine is described by the following state equations.

$$Q_1(t+1) = x(t)Q_1(t) + Q'_0(t),$$

$$Q_0(t+1) = Q_1(t)Q_0(t).$$

Use two **D flip-flops** and a minimal sum-of-products network to implement the machine.

(i). Fill the state table of the system. **(5 Points for completion)**

id	$Q_1(t)$	$Q_0(t)$	$x(t)$	$Q_1(t+1)$	$Q_0(t+1)$	D_1	D_0
0	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
2	0	1	0	0	0	0	0
3	0	1	1	0	0	0	0
4	1	0	0	1	0	1	0
5	1	0	1	1	0	1	0
6	1	1	0	0	1	0	1
7	1	1	1	1	1	1	1

Here is the K-map for D_0 , which gives: $D_0 = Q_1.Q_0$.

And here is the K-map for D_1 , which gives: $D_1 = x.Q_1 + Q'_0$.

So, we can draw the logic diagram like this:

