

CSE140 Week 6 Discussion

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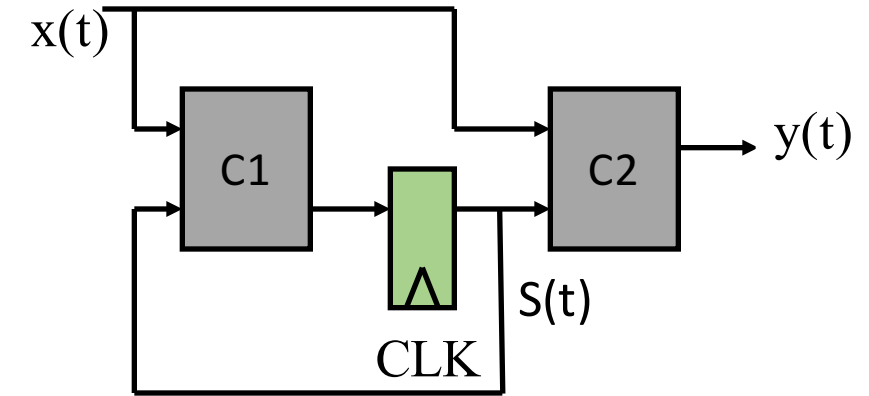
Outline

- Finite State Machines
- Timing and Retiming

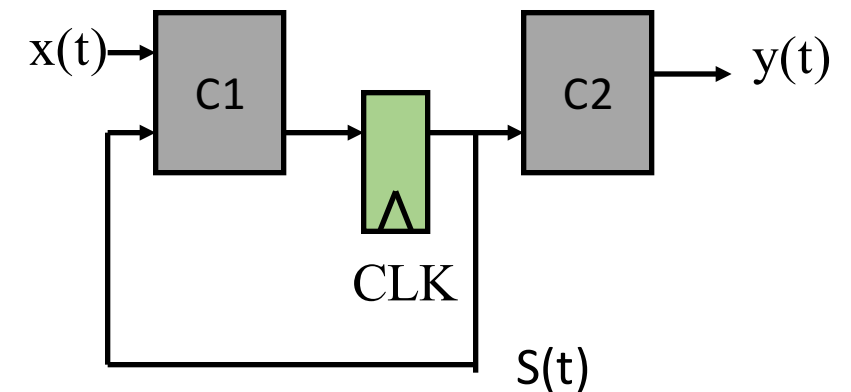
Mealy and Moore Machines

- Mealy Machine: general
 - $y_i(t) = f_i(X(t), S(t))$
- Moore Machine: Output is independent of current input
 - $y_i(t) = f_i(S(t))$
 - $S_i(t + 1) = g_i(X(t), S(t))$
- How to convert Mealy to Moore machine?

Mealy Machine



Moore Machine



Implementation

✓ **Given: State diagram**



Circuit implementation?

- Example: Lec8 and HW3 “pattern recognizer”

✓ **Given: Circuit implementation**



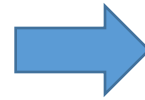
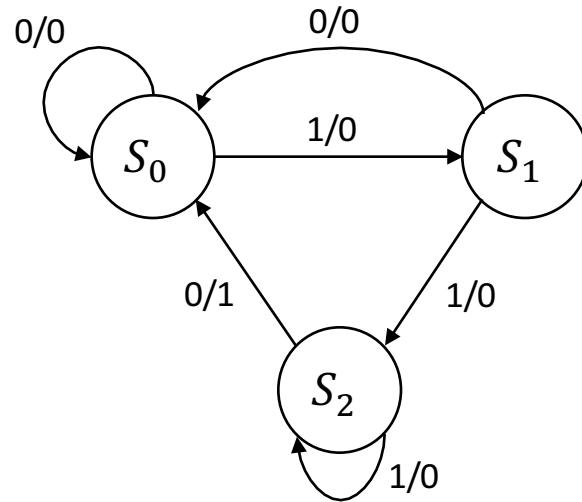
Input output relation?

Implementation

- ✓ **Given: State diagram**
 - Derive the state table and assign states
 - Excitation table
 - Equations(K-maps if needed)
 - Circuit implementation

Examples : given a state diagram

- **Step 1: Derive state table and assign states**



PS/Input	$X = 0$	$X = 1$
S_0	$S_0, 0$	$S_1, 0$
S_1	$S_0, 0$	$S_2, 0$
S_2	$S_0, 1$	$S_2, 0$

- $S_0 \Rightarrow 00$
- $S_1 \Rightarrow 01$
- $S_2 \Rightarrow 10$

Examples : given a state diagram

- **Step 2: Excitation table**

- $S_0 \Rightarrow 00$

- $S_1 \Rightarrow 01$

- $S_2 \Rightarrow 10$

PS/Input	$X = 0$	$X = 1$
S_0	$S_0, 0$	$S_1, 0$
S_1	$S_0, 0$	$S_2, 0$
S_2	$S_0, 1$	$S_2, 0$

- Excitation table

$Q_1(t)$	$Q_0(t)$	$X(t)$	$Q_1(t+1)$	$Q_0(t+1)$	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X



Examples : given a state diagram

- **Step 3:** Derive equations
 - Use **D Flip-Flop**: $Q(t+1) = D(t)$
 - K-maps

$X(t)/Q_1(t)Q_0(t)$	00	01	11	10
0	0	0	X	0
1	0	1	X	1

$$D_1(t) = X(t)Q_0(t) + X(t)Q_1(t)$$

$Q_1(t)$	$Q_0(t)$	$X(t)$	$Q_1(t+1)$	$Q_0(t+1)$	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X

Examples : given a state diagram

- **Step 3: Derive equations**
 - Use D Flip-Flop: $Q(t+1) = D(t)$
 - K-maps

$X(t)/Q_1(t)Q_0(t)$	00	01	11	10
0	0	0	X	0
1	1	0	X	0

$$D_0(t) = X(t)Q'_0(t)Q'_1(t)$$

$X(t)/Q_1(t)Q_0(t)$	00	01	11	10
0	0	0	X	1
1	0	0	X	0

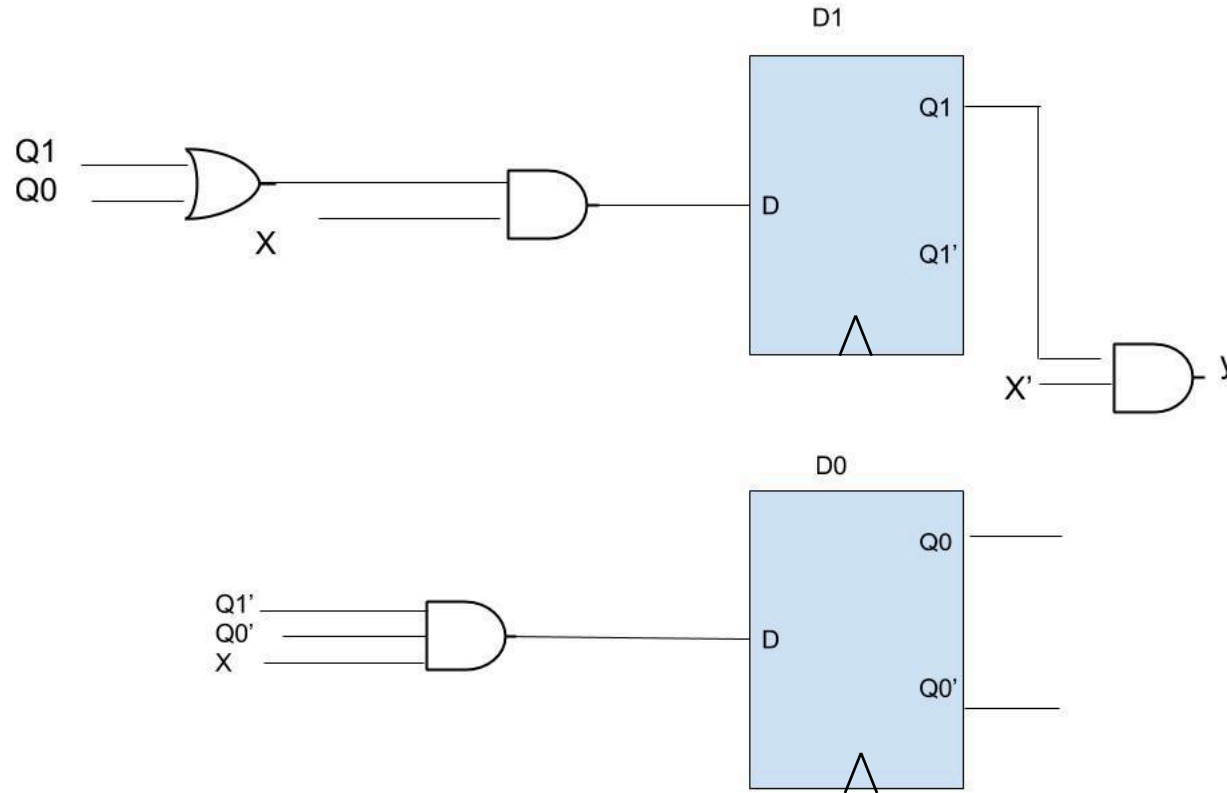
$$y = X'(t)Q_1(t)$$

$Q_1(t)$	$Q_0(t)$	$X(t)$	$Q_1(t+1)$	$D_0(t)$ $Q_0(t+1)$	<i>output</i> y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	X	X	X
1	1	1	X	X	X

Examples : given a state diagram

- **Step 4:** Circuit implementation

- Use D Flip-Flop: $Q(t+1) = D(t)$



$$D_1(t) = X(t)Q_0(t) + X(t)Q_1(t)$$

$$D_0(t) = X(t)Q'_0(t)Q'_1(t)$$

$$y = X'(t)Q_1(t)$$

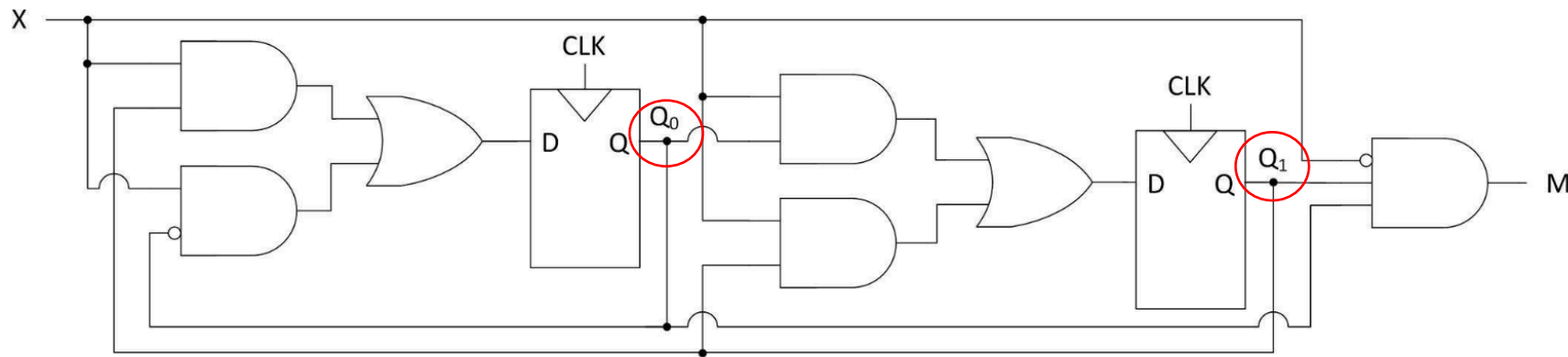
Implementation

- ✓ **Given: Circuit implementation**
 - Excitation table
 - Identify states and derive a state table
 - State diagram
 - Input output relation

Example: given a circuit implementation

- **Step 1: Excitation table**

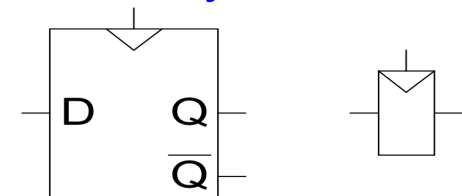
4. (Finite State Machine Specification) Analyze the following circuit.



4.1 Write the transition(excitation) table (8 points).

- D Flip-Flop: $Q(t+1) = D(t)$
 - $D(t)$ can be find with current input $X(t)$ and current state $Q_0(t)$, $Q_1(t)$

D Flip-Flop
Symbols



Examples : given a circuit implementation

- **Step 1: Excitation table**

- State Equations

$$Q_0(t+1) = XQ_1(t) + XQ_0(t)'$$

$$Q_1(t+1) = XQ_1(t) + XQ_0(t)$$

$$M = X'Q_1(t)Q_0(t)$$



- Excitation table

$Q_1(t)$	$Q_0(t)$	X	$Q_1(t+1)$	$Q_0(t+1)$	M
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	0

Examples : given a circuit implementation

- **Step 2: Identify states and derive state table**

- $S_0 \leftarrow 00$

- $S_1 \leftarrow 01$

- $S_2 \leftarrow 10$

- $S_3 \leftarrow 11$

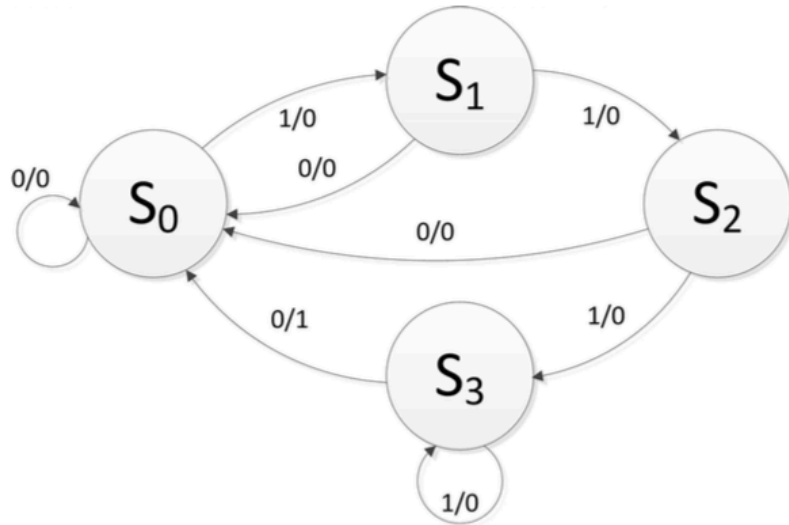
PS/Input	$X = 0$	$X = 1$
S_0	$S_0, 0$	$S_1, 0$
S_1	$S_0, 0$	$S_2, 0$
S_2	$S_0, 0$	$S_3, 0$
S_3	$S_0, 1$	$S_3, 0$

$Q_1(t)$	$Q_0(t)$	X	$Q_1(t+1)$	$Q_0(t+1)$	M
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	0



Examples : given a circuit implementation

- **Step 3: State diagram**



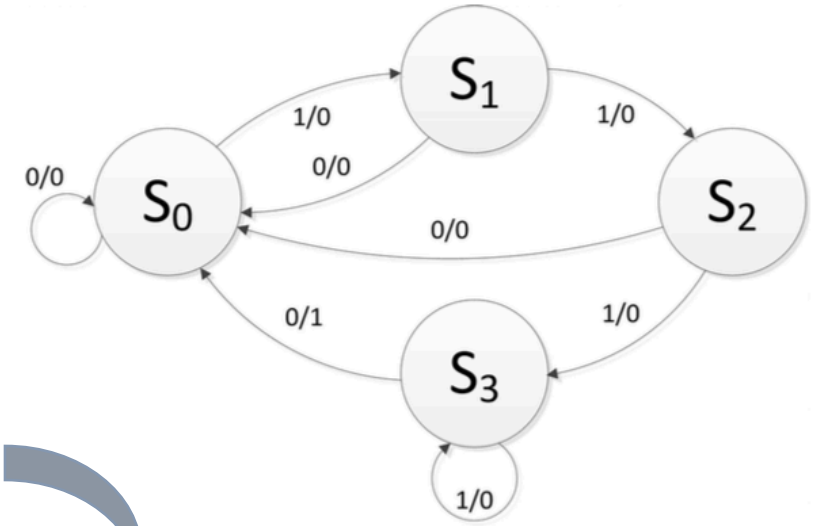
PS/Input	$X = 0$	$X = 1$
S_0	$S_0, 0$	$S_1, 0$
S_1	$S_0, 0$	$S_2, 0$
S_2	$S_0, 0$	$S_3, 0$
S_3	$S_0, 1$	$S_3, 0$

Examples : given a circuit implementation

- **Step 4: Input output relation**

cycle	1	2	3	4	5	6	7	8	9	10
X	1	1	1	0	0	0	1	1	1	0
state	S_0									
M										

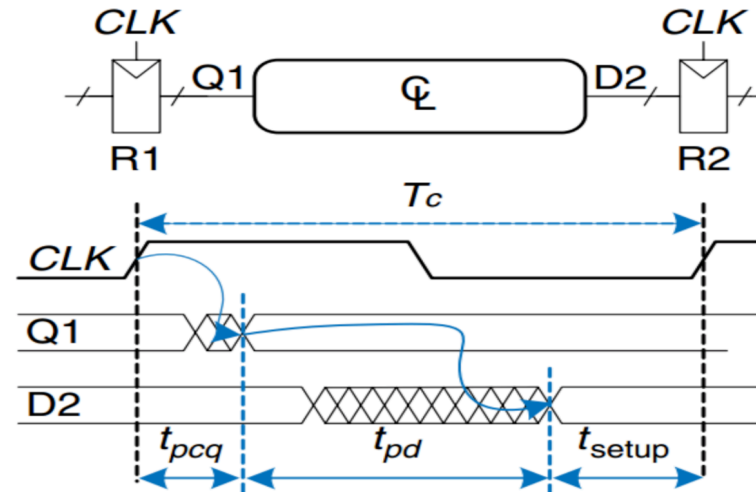
cycle	1	2	3	4	5	6	7	8	9	10
X	1	1	1	0	0	0	1	1	1	0
state	S_0	S_1	S_2	S_3	S_0	S_0	S_0	S_1	S_2	S_3
M	0	0	0	1	0	0	0	0	0	1



Sequential Networks: Timing Constraint (without skew)

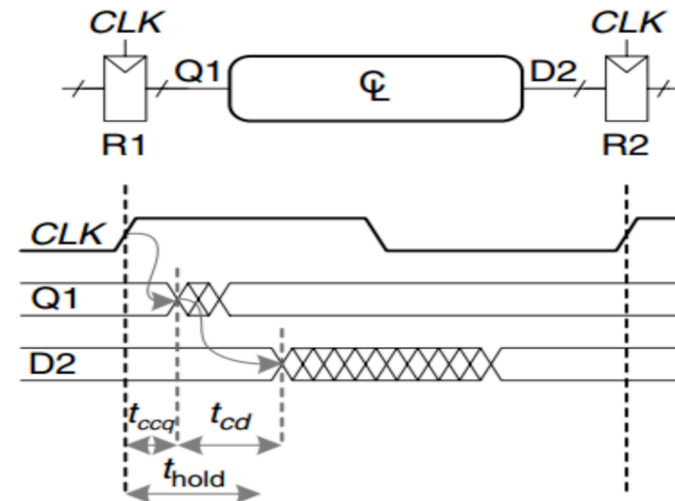
- **Setup Time Constraint**

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$



- **Hold Time Constraint**

$$t_{ccq} + t_{cd} \geq t_{\text{hold}}$$



Sequential Networks: Timing Constraint (with skew)

- **Time Skew**

- Difference between two clock edges
- $t_{skew} = CLK2 - CLK1$

- **Setup Time Constraint**

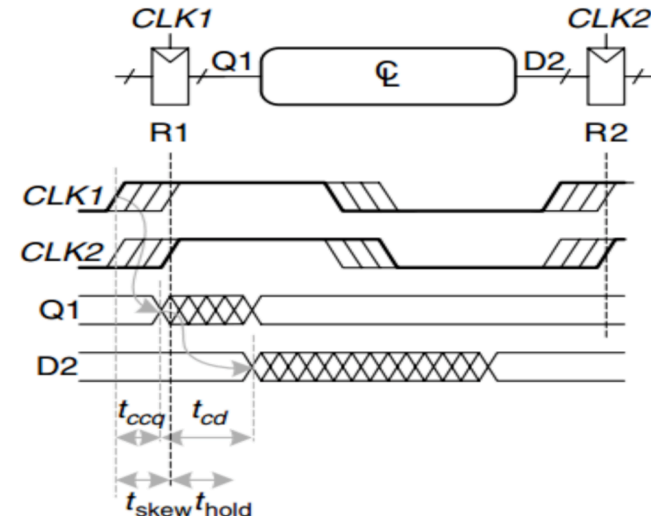
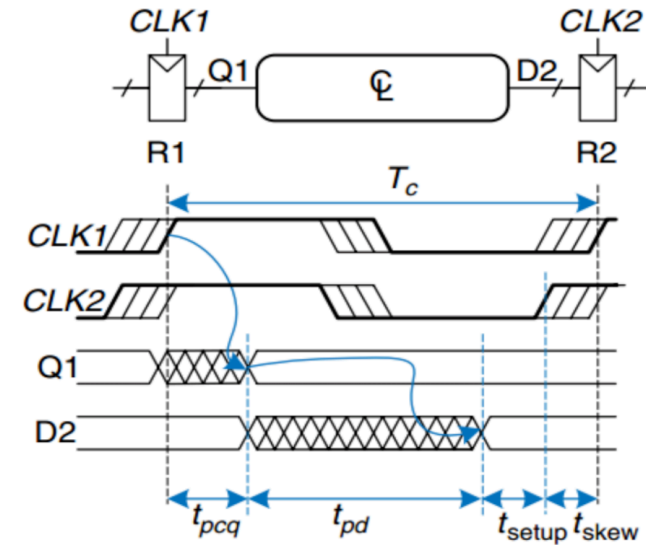
- CLK2 is earlier than CLK1 ($t_{skew} < 0$)

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}$$

- **Hold Time Constraint**

- CLK2 is later than CLK1

$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$



Example: Timing

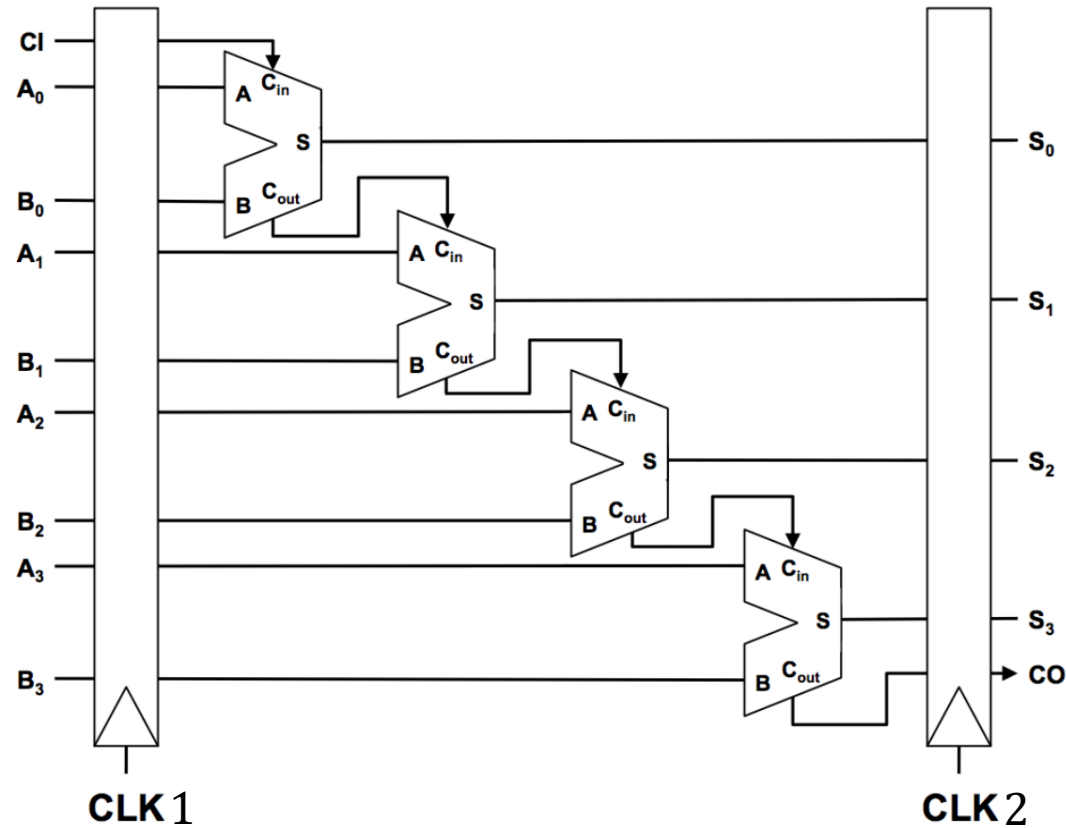


Figure 2: A four-bit addition machine.

- Propagation delay and contamination delay

✓ Adder

- C_{in} to C_{out}/S
 - $t_{pd} = 20ps$
 - $t_{cd} = 15ps$
- A/B to C_{out}
 - $t_{pd} = 25ps$
 - $t_{cd} = 22ps$
- A/B to S
 - $t_{pd} = 30ps$
 - $t_{cd} = 22ps$

**Maximum
frequency?**

✓ D-FF

- $t_{pcq} = 35ps$
- $t_{ccq} = 25ps$
- $t_{setup} = 30ps$
- $t_{hold} = 10ps$

Example: Timing (Without Clock Skew)

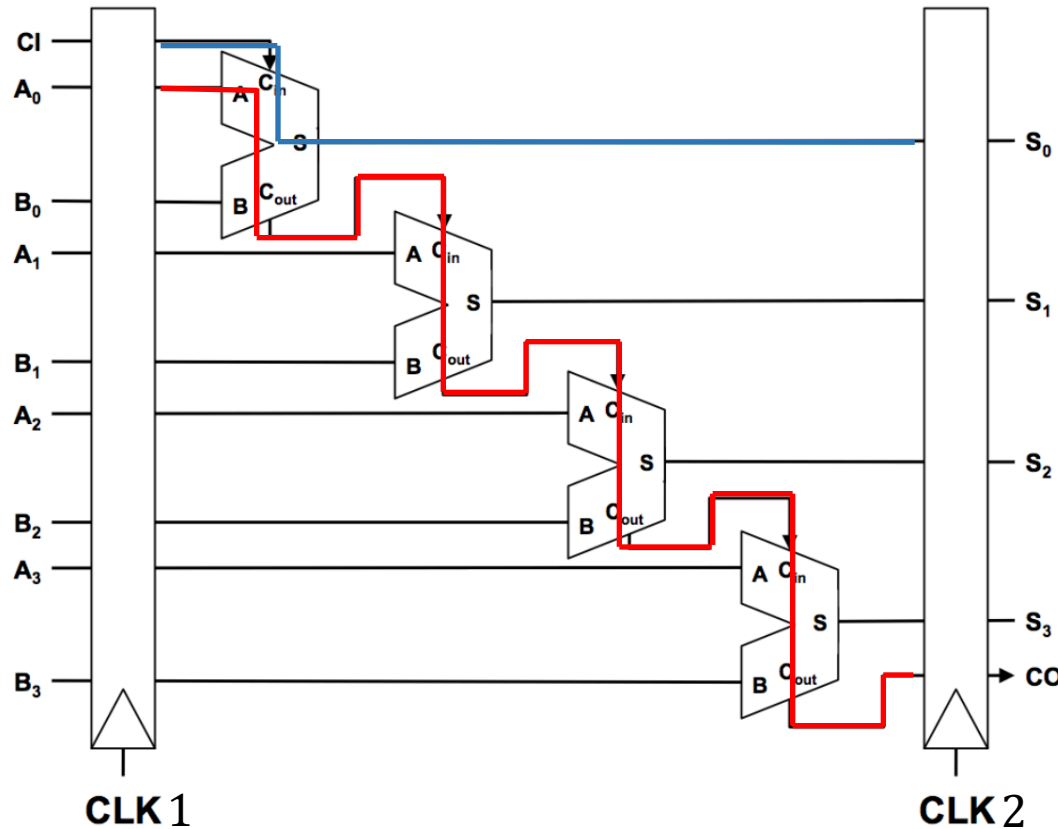


Figure 2: A four-bit addition machine.

- Find the longest path of combinational logic

$$t_{pd(max)} = 3 \times t_{pd}(C_{in} \text{ to } C_{out}) + t_{pd}(A, B \text{ to } C_{out})$$

- Setup Time Constraint

$$T_c \geq t_{pcq} + t_{pd} + t_{setup}$$

$$T_c \geq (35 + 3 \times 20 + 25 + 30) = 150ps$$

$$\text{the maximum frequency } \frac{1}{T} = 6.67GHz$$

- Hold Time Constraint

$$t_{cd(min)} = t_{cd}(C_{in} \text{ to } S) = 15ps$$

$$t_{ccq} + t_{cd(min)} = 25 + 15 = 40ps \geq t_{hold} = 10ps$$

Example: Timing (With Clock Skew)

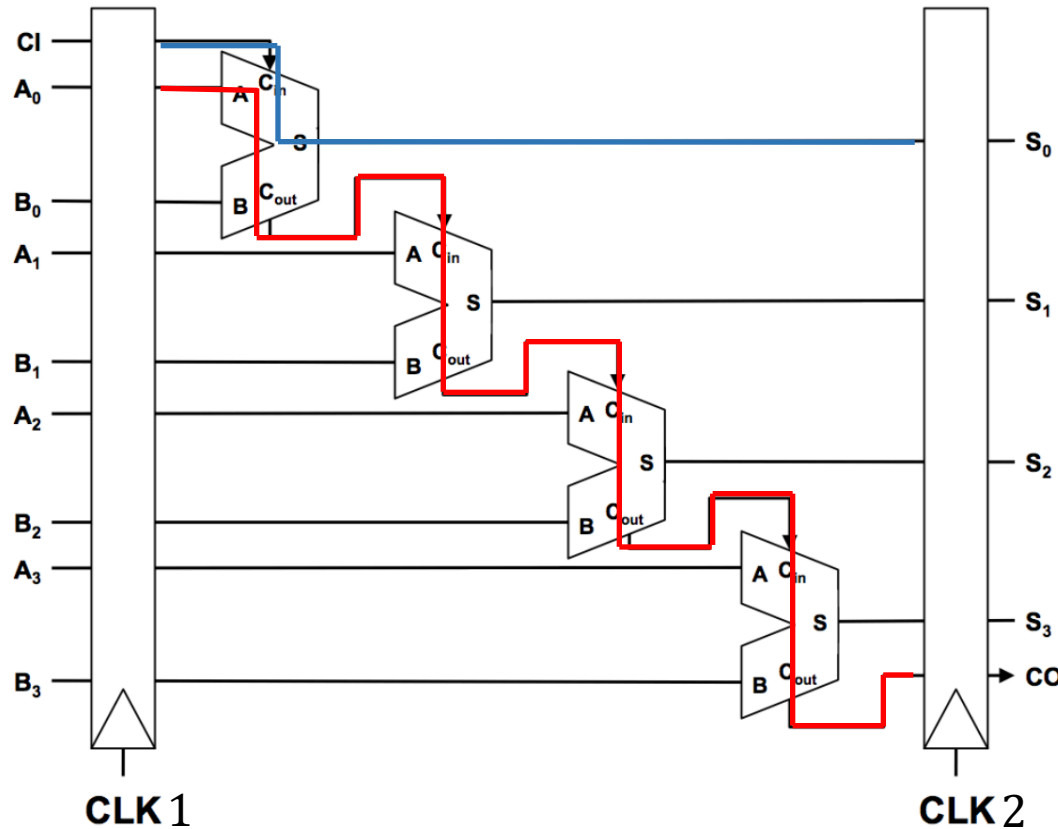


Figure 2: A four-bit addition machine.

- Hold Time Constraint

$$t_{ccq} + t_{cd(min)} = 25 + 15 = 40ps$$

$$\geq t_{hold} + t_{skew} = (10 + \Delta)ps$$

$$t_{skew} = 30ps \quad \text{CLK2 Later than CLK1 !!!}$$

- Setup Time Constraint

$$T_c + t_{skew} \geq t_{pcq} + t_{pd} + t_{setup}$$

$$T_c \geq (150 - 30) = 120ps$$

$$\text{the maximum frequency } \frac{1}{T} = 8.33GHz$$