CSE 243A (Section Id: 743533)

VLSI Computer-Aided Design

Synthesis Methodologies in VLSI Design

MoWe 2:00 - 3:20 PM; EBU3B 2154

Professor Alex Orailoğlu
EBU3B 3134
Tel: 858-534-0914 Fax: 858-534-7029
email: alex@cs.ucsd.edu

Course Contents

Synthesis Fundamentals: Circuits and Models Microelectronics. Semiconductor Technologies. Microelectronic Design Styles. Levels of Abstraction. Computer-Aided Synthesis and Optimization. Physical Design. Simulation. Verification. Test.

Architectural Models Design Styles. Combinatorial Logic. Finite State Machine with a Datapath. System Architecture.

Architectural Synthesis Design Representation. Behavioral Transformations. Partitioning. Time-Constrained Scheduling. Resource-Constrained Scheduling. Scheduling Pipelined Circuits. Allocation Tasks. Functional Unit Binding. Storage Unit Binding. Interconnection Binding.

Combinational Logic Optimization Two-level Combinational Logic Optimization. Logic Optimization Principles. Exact Logic Minimization. Heuristic Logic Minimization. Symbolic Minimization and Encoding Problems. Multiple-Level Combinational Logic Optimization.

Sequential Logic Optimization State Minimization. State Encoding.

Cell-Library Binding Problem Formulation and Algorithms. Structural-Matching based Technology Mapping. Boolean-Matching based Technology Mapping. Technology Mapping for FPGAs

Codesign and Embedded Systems Modeling. Performance Analysis. Power Analysis. Memory Hierarchies in Codesign. System-Level Partitioning. Interface Co-synthesis. Embedded Software. Hardware-Software Co-simulation. Reconfigurable Computing. Application Specific Processors.