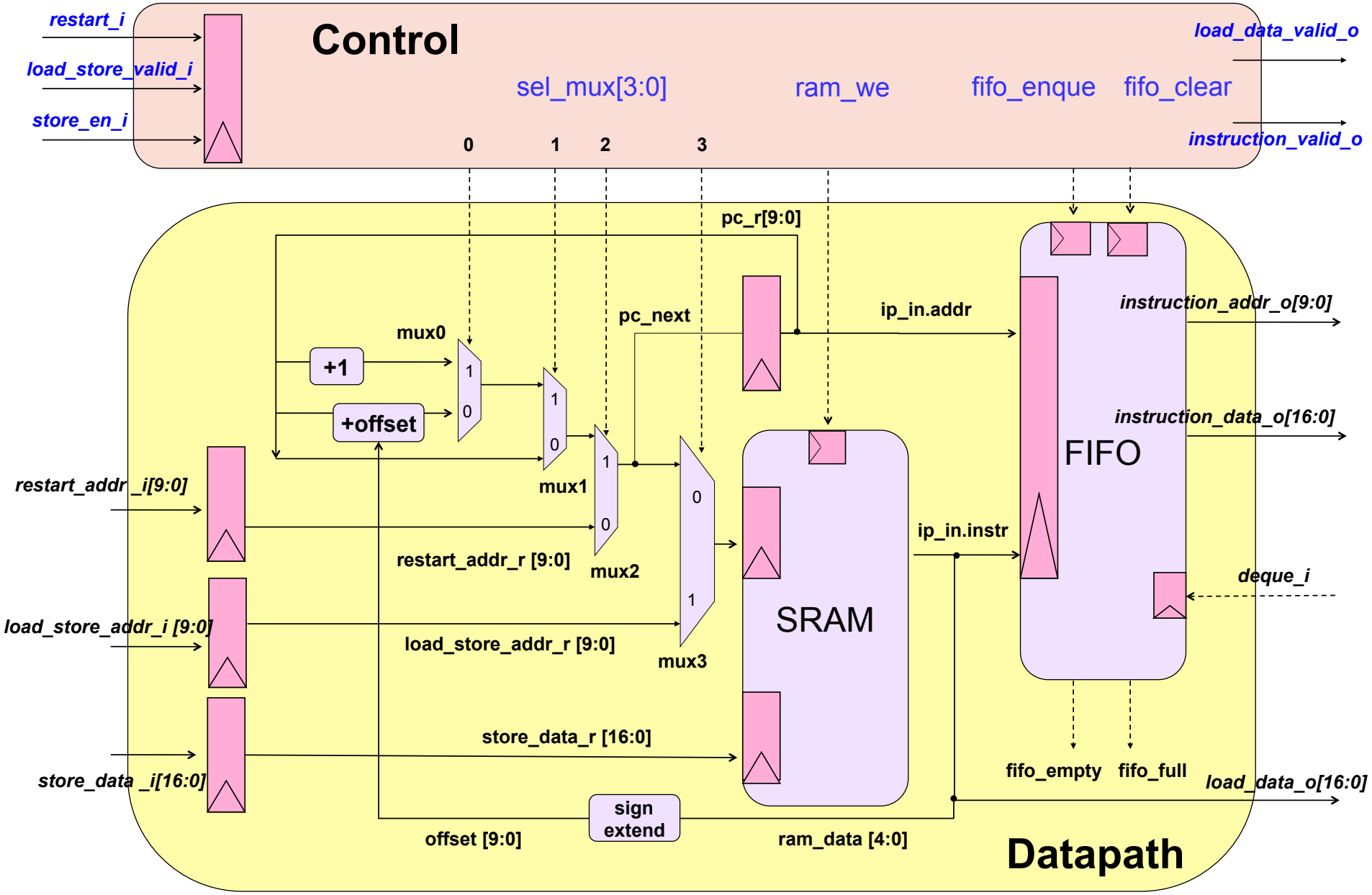
restart_i
load_store_valid_i
store_en_i
Control
sel_mux[3:0]
ram_we
fifo_enque
fifo_clear
load_data_valid_o
instruction_valid_o
0
1
2
3
pc_r[9:0]
mux0
+1
+offset
1
0
mux1
mux2
mux3
pc_next
ip_in.addr
instruction_addr_o[9:0]
instruction_data_o[16:0]
FIFO
restart_addr _i[9:0]
restart_addr_r [9:0]
load_store_addr_i [9:0]
load_store_addr_r [9:0]
store_data _i[16:0]
store_data_r [16:0]
SRAM
ip_in.instr
deque_i
fifo_empty
fifo_full
load_data_o[16:0]
sign extend
offset [9:0]
ram_data [4:0]
Datapath