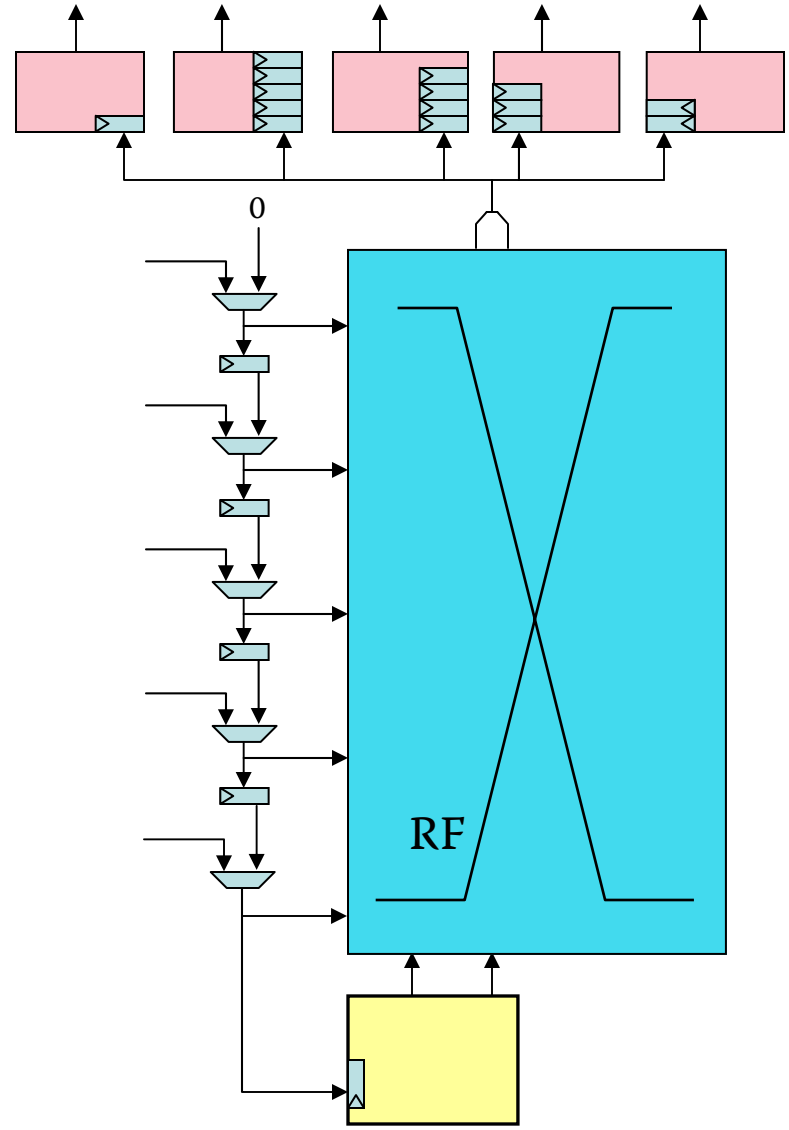
CSE 141:

Computer Architecture

Professor: Michael Taylor

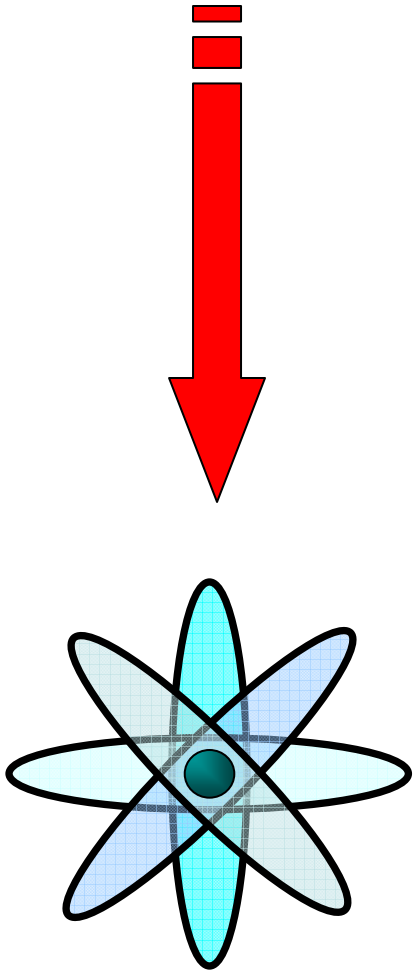


UCSD Department of Computer Science & Engineering

Computer Architecture from 10,000 feet

```
foo(int x)
  { .. }
```

Class of application



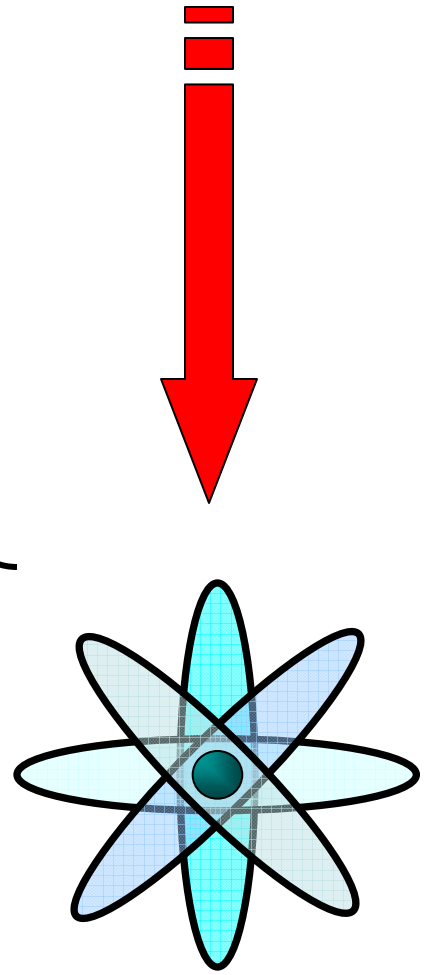
Physics

Computer Architecture from 10,000 feet

```
foo(int x)
  { .. }
```

Class of application

An impossibly large gap!



Physics

In the olden days:

"In 1942, just after the United States entered World War II, hundreds of women <u>were employed around the country as computers</u>..." (source: IEEE)

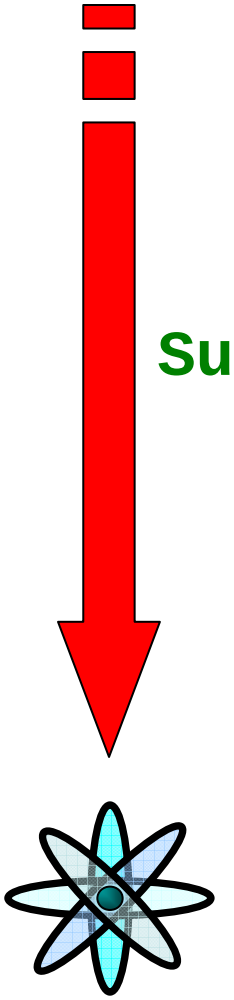
The Great Battles in Computer Architecture Are About How to Refine the Abstraction Layers

```
foo(int x) { .. }
```

Computation

- Language
- Compiler
- ISA
- Micro Architecture
- Register-Transfer Level
- Circuits
- Devices
- Materials Science

Physics



Fortran

IBM 360, VLIW

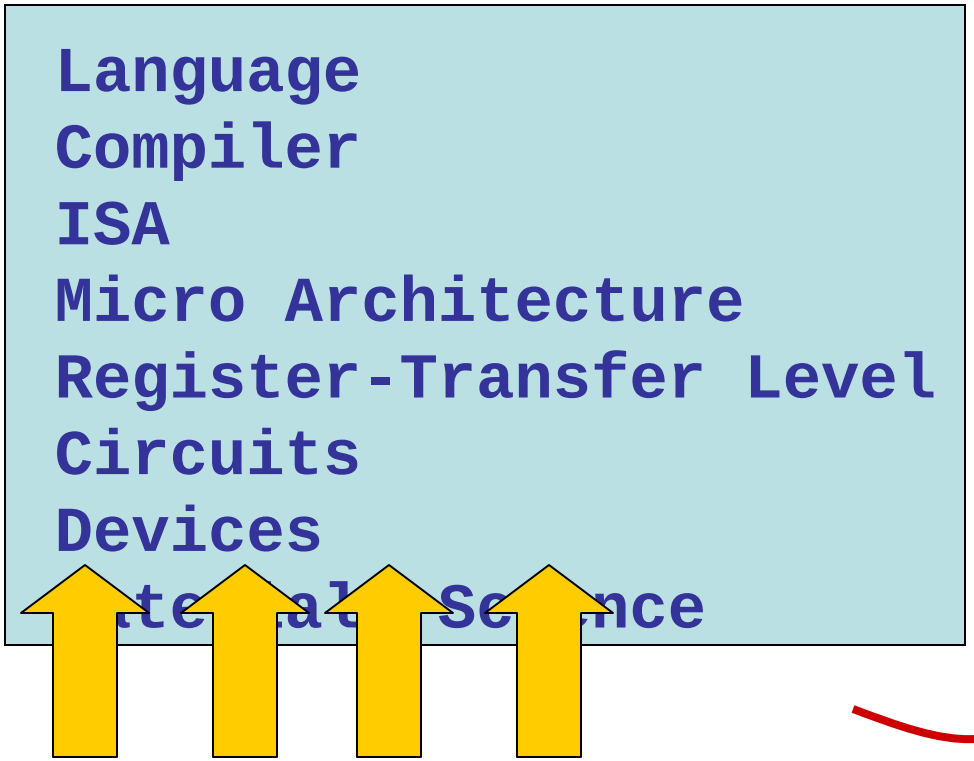
RISC, T'meta

Superscalar, caches

Mead & Conway

Abstractions protect us from change
-- but must also change as the world changes

Computation



Changes in fabrication capabilities

Slower Wires!

Denser VLSI gates!

More pins!

More Power/cm^2!

Abstraction Layers – reflected in organization of research communities

Computation

Language
Compiler
ISA
Micro Architecture
Reg-Transfer Level
Circuits
Devices
Materials Science

Physics

International Symposium on Computer Architecture (ISCA)

High Performance Computer Architecture (HPCA)

Architectural Support for Programming Languages and OS (ASPLOS)

International Symposium on Microarchitecture (MICRO)

Design Automation Conference (DAC)
Int. Conf. Computer Aided Design (ICCAD)

International Solid State Circuit Conference (ISSCC)

International Electron Devices Meeting (IEDM)

Classic ISSCC (Circuits) Paper: "How we designed a *chip* and how fast / low power it is."

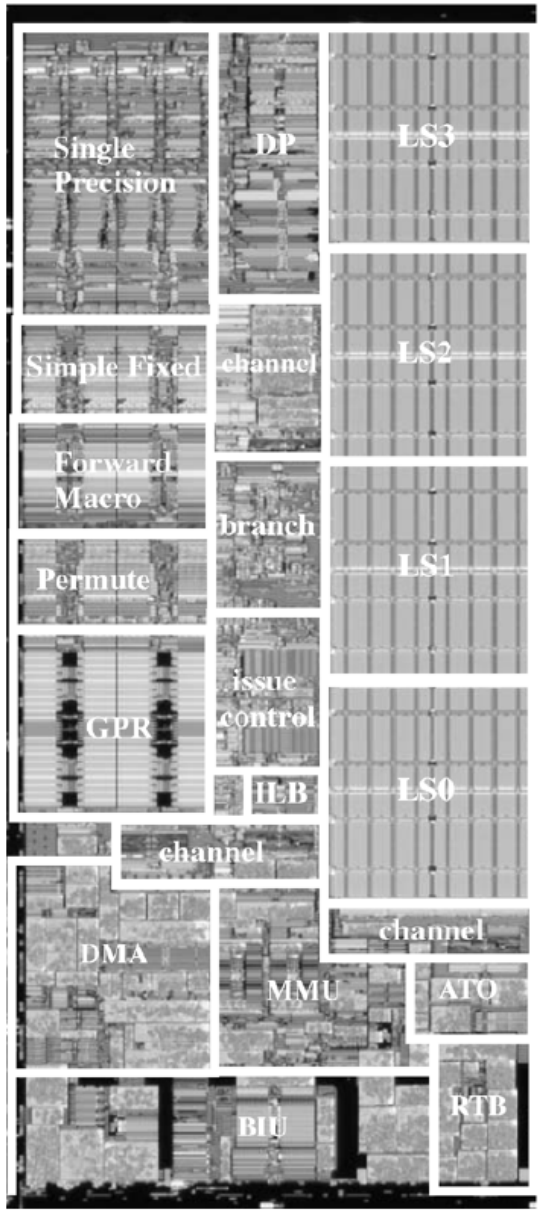


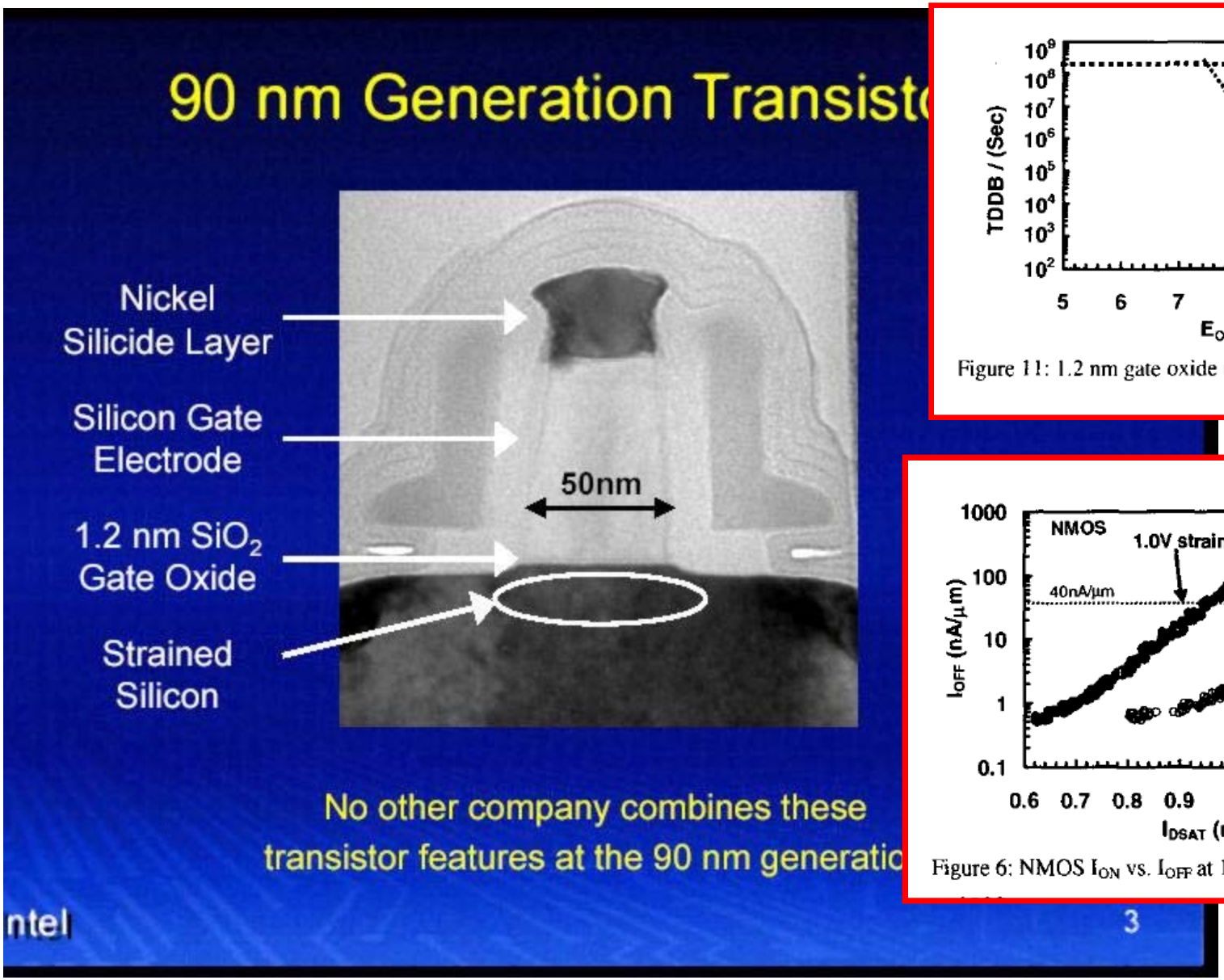
TABLE IV
VOLTAGE/FREQUENCY SCHMOO

2	2.2	2.4	2.6	2.8	3	3.2	3.4	3.6	3.8	4	4.2	4.4	4.6	4.8	5	5.2
48C 4W	49C 4W	50C 5W	50C 6W	51C 6W	52C 7W	53C 7W	54C 7W	55C 8W	56C 8W	57C 9W	58C 9W	59C 10W	60C 10W	61C 10W	63C 11W	61C
39C 2W	39C 3W	40C 3W	41C 4W	42C 4W	42C 4W	43C 5W	44C 5W	45C 5W	45C 5W	46C 6W	47C 6W	47C 7W	48C	49C		
32C 2W	33C 2W	33C 3W	35C 3W	35C 3W	36C 3W	36C 4W	37C 4W	37C 4W	38C 4W	38C 4W	39C	39C				
28C 2W	28C 2W	29C 2W	29C 2W	30C 2W	30C 3W	30C 3W	31C 3W	31C 3W	31C 3W	32C						
25C 1W	26C 1W	26C 1W	26C 2W	27C 2W	27C 2W	27C										

Failed

Freq (GHz)

Classic Int. Electron Device Meeting (IEDM) Paper: How we designed a single transistor



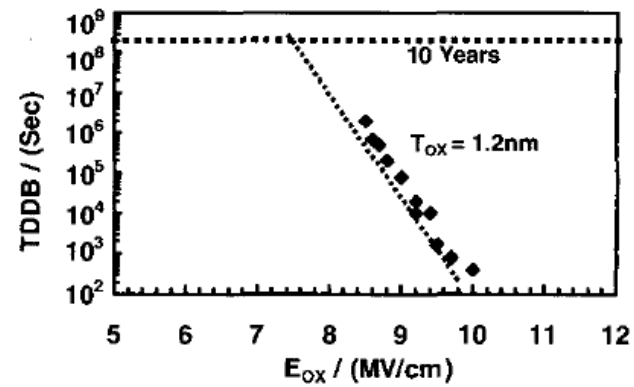


Figure 11: 1.2 nm gate oxide time to fail vs. electric field.

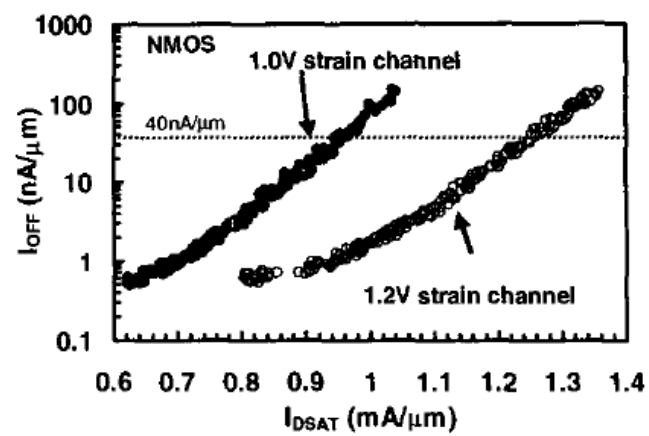
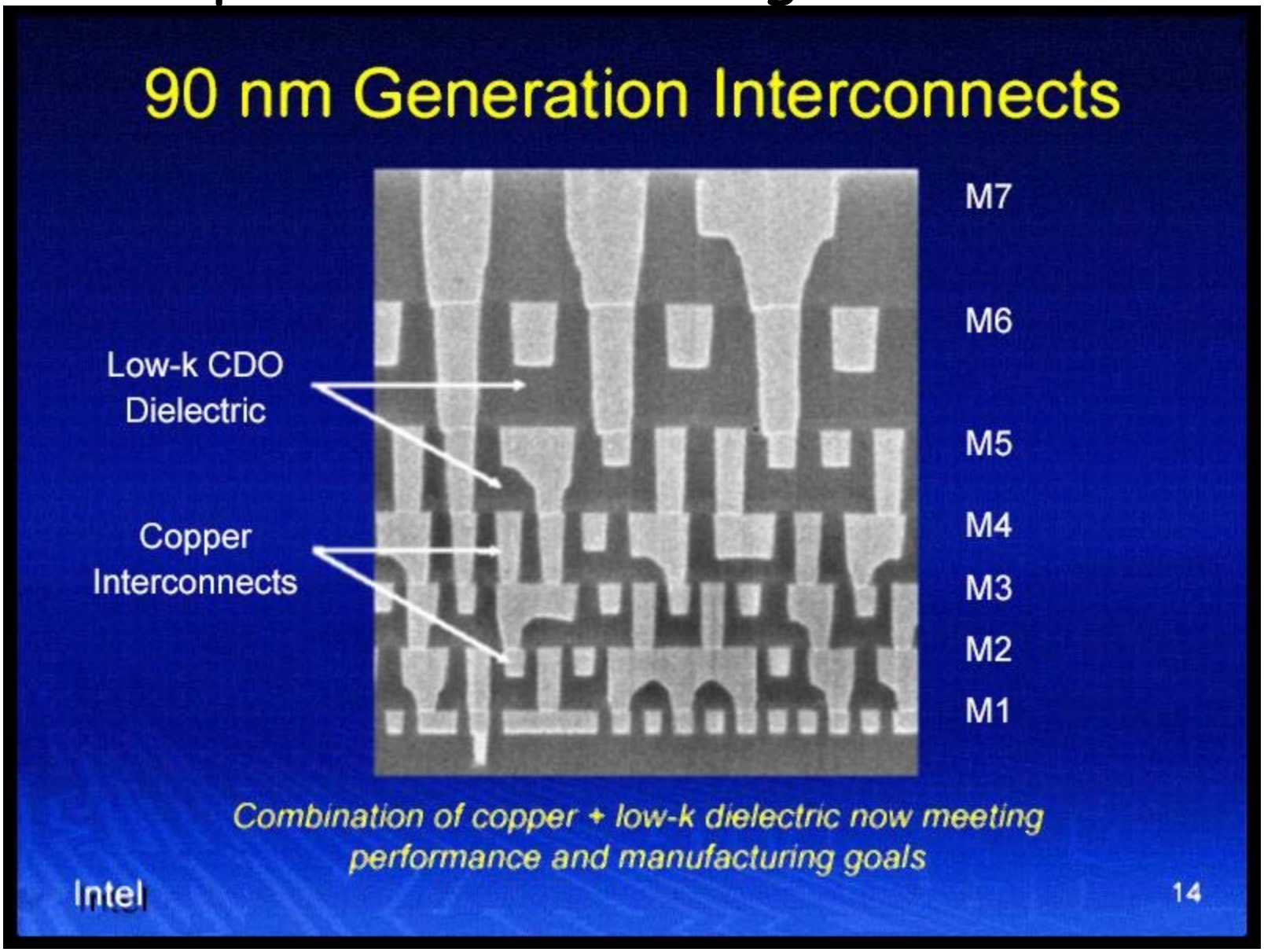
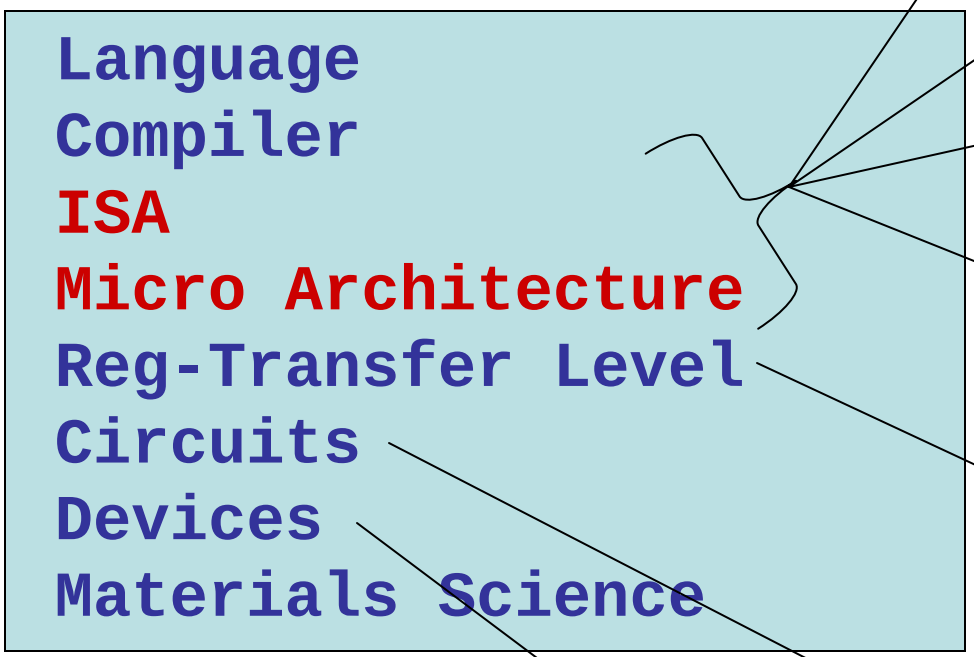


Figure 6: NMOS I_{ON} vs. I_{OFF} at 1.0V and 1.2V.

Classic Int. Electron Device Meeting (IEDM) Paper: "How we designed a *wire*"



The focus of this class



International Symposium on Computer Architecture (ISCA)

High Performance Computer Architecture (HPCA)

Architectural Support for Programming Languages and OS (ASPLOS)

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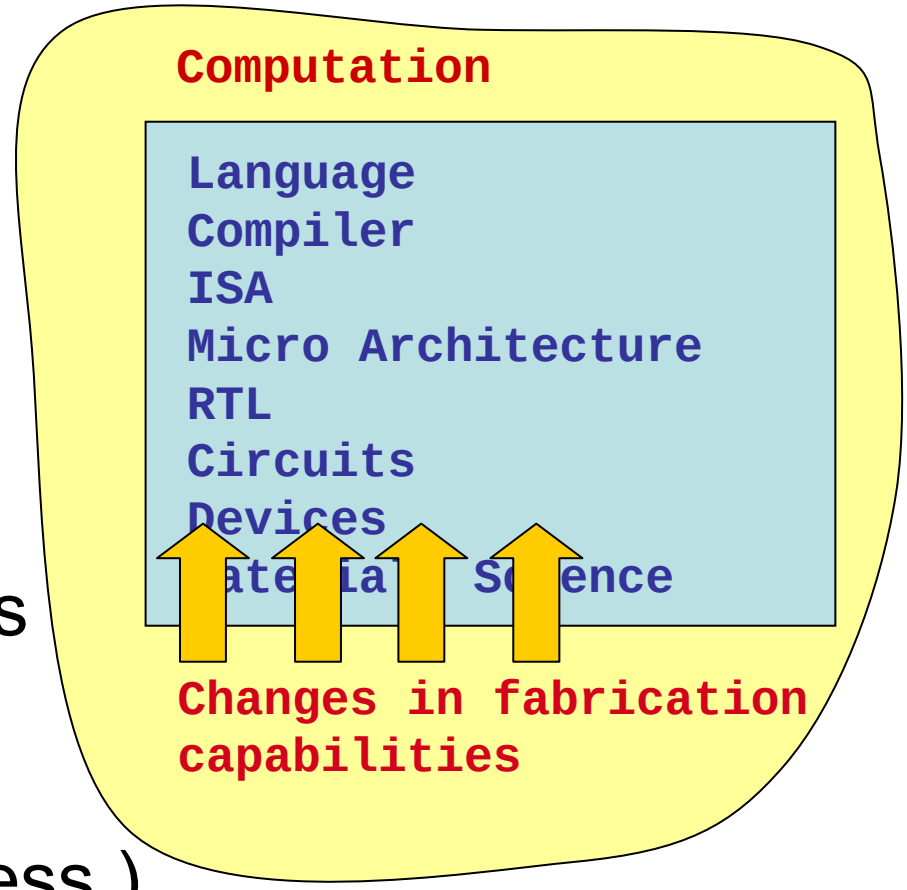
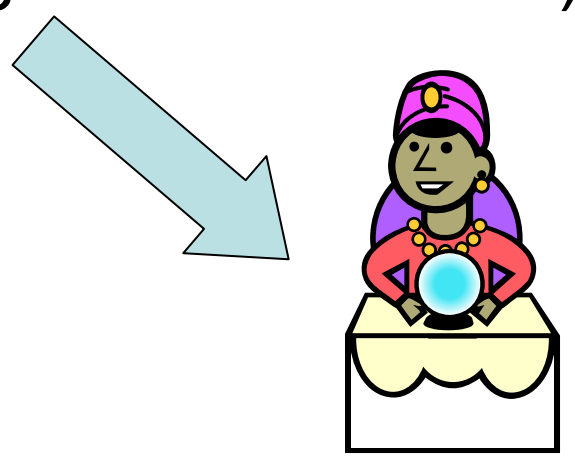
International Solid State Circuit Conference (ISSCC)

International Electron Devices Meeting (IEDM)

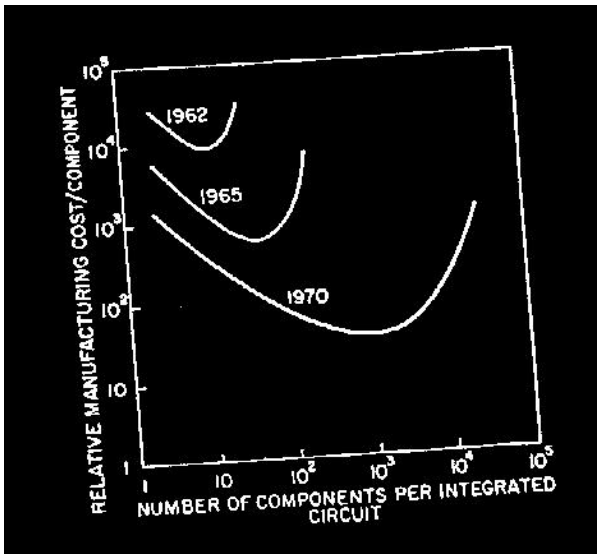
Tech Trends

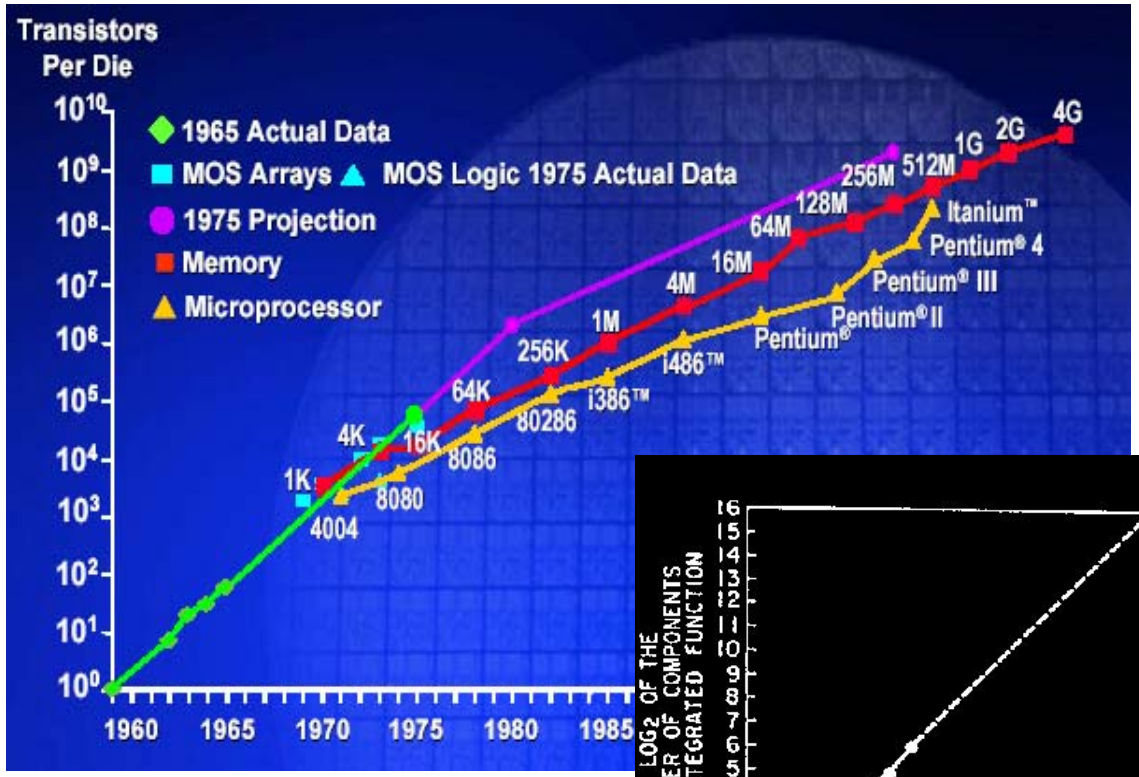
Since technology change is such a big influence in architecture, and because it takes 3-6 years to create a totally new design, we try to predict & exploit it (with varying degrees of success.)

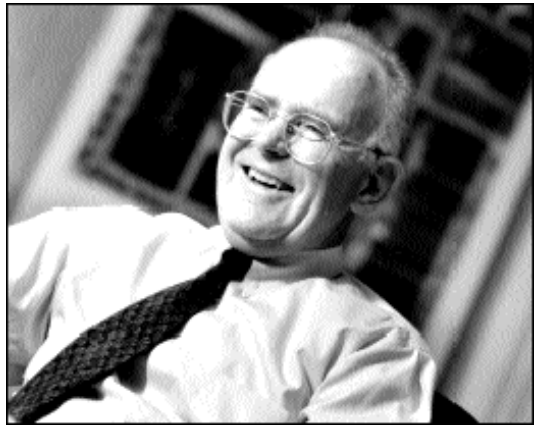


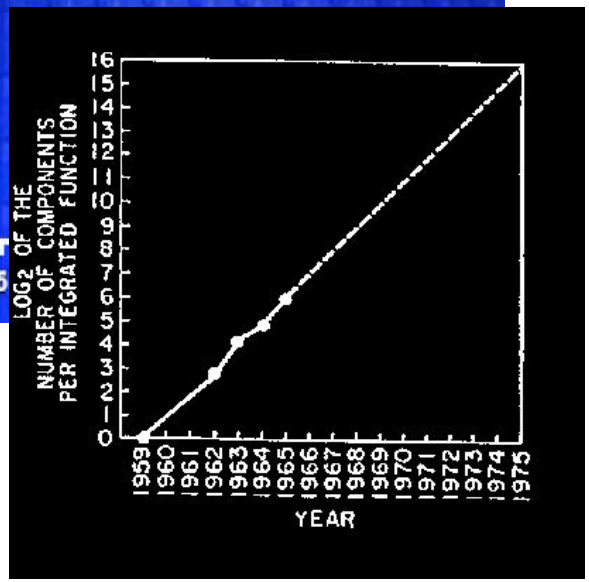


Moore's Law: 2X transistors / "year"









"Cramming More Components onto Integrated Circuits"

- Gordon Moore, Electronics, 1965

on transistors / cost-effective integrated circuit double every N months (12 ≤ N ≤ 24)

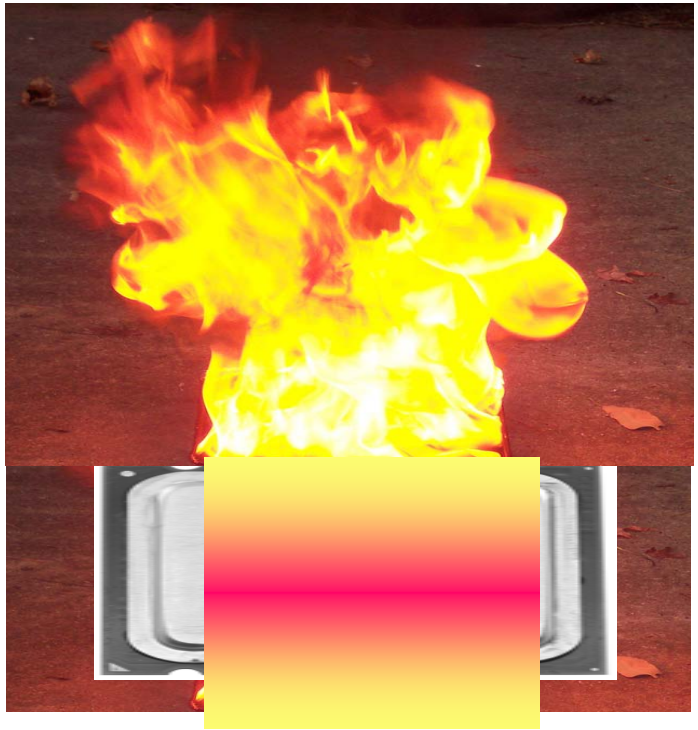
Adapted from Patterson, CSE 252 Sp06 Lecture 2 © 2006 UC Berkeley.

One Important Change: Power

Santa Clara, we have a problem

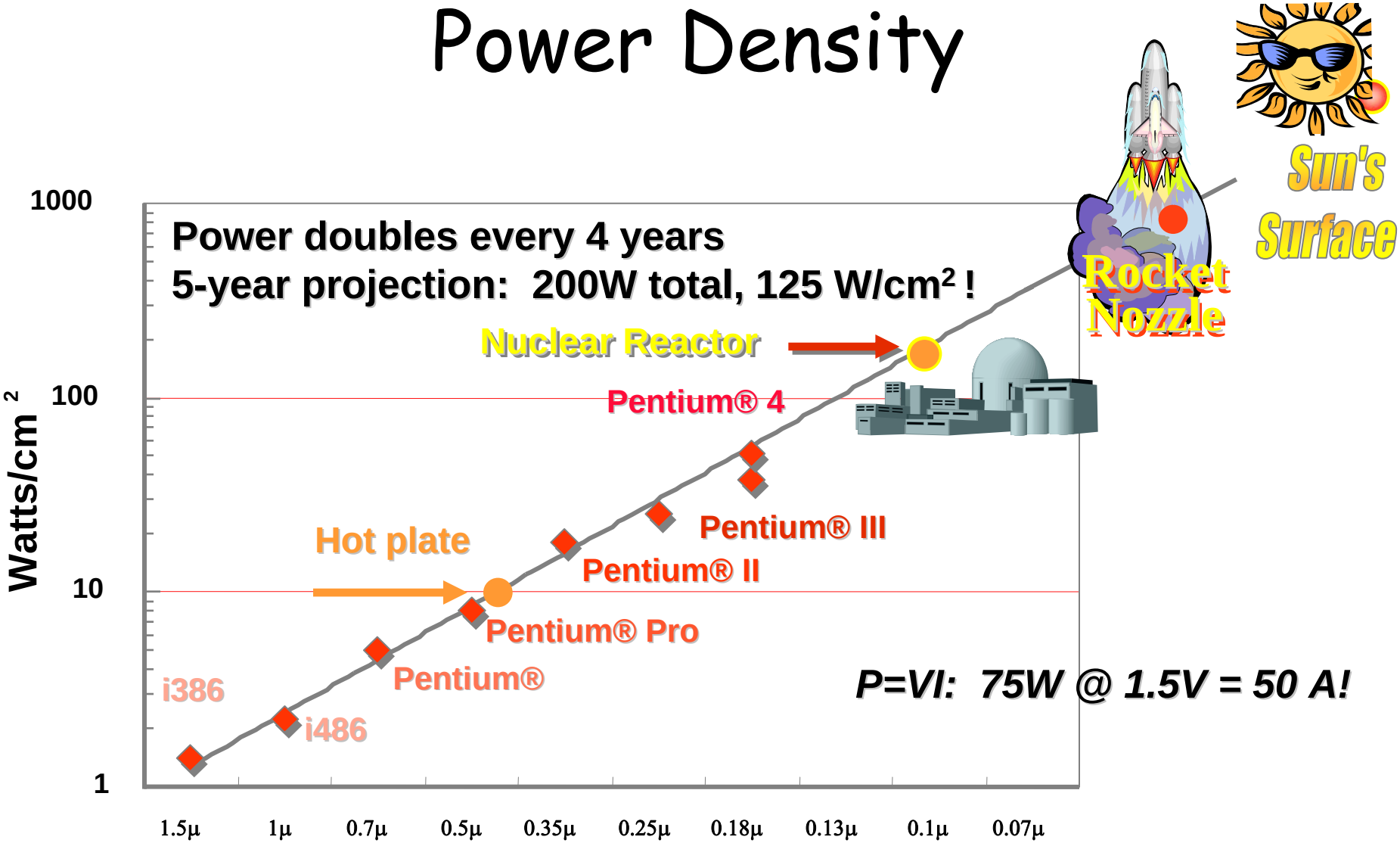
More pipeline stages,
less efficient, more power.

Just can't remove
> 100 watts
without great expense on
a desktop.



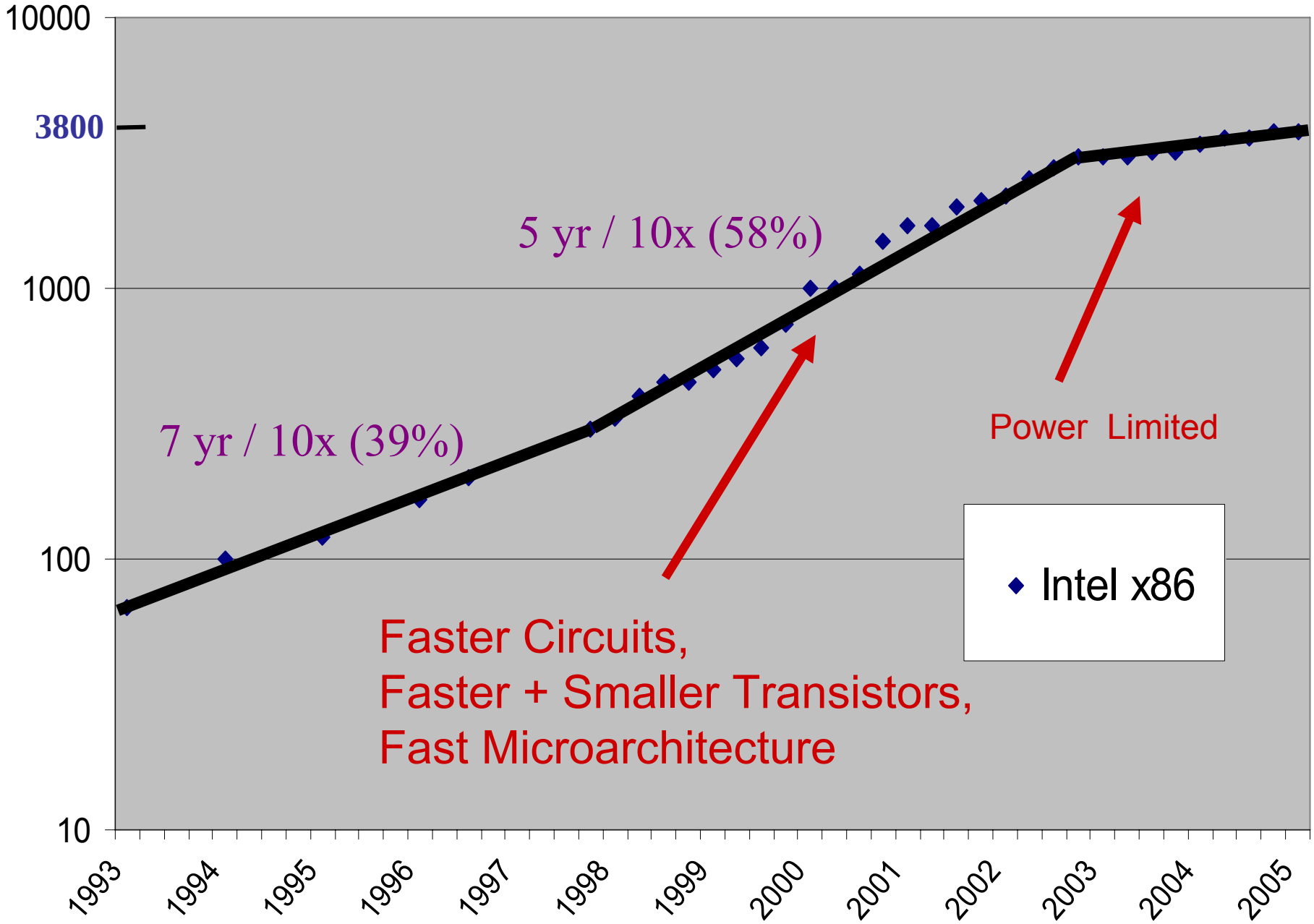
<u>All</u> computing is now
<u>Low Power Computing</u>!

Power Density



From "New Microarchitecture Challenges in the Coming Generations of CMOS Process Technologies" – Fred Pollack, Intel Corp. Micro32 conference key note - 1999.

Change: microprocessor frequency versus time



Intel

P3: **12 stages**

P4 (b4 paper): **20 stages**

P4/prescott: **31 stages**

~~**P5/Tejas:**~~ **>> 31 stages**

Intel

P3: **12 stages**

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Intel

P3: **12 stages**

~~**P4 (b4 paper):**~~ **20 stages**

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~~**P5/Tejas:**~~ **>> 31 stages**

Back to the future

P3:

12 stages

P4 (b4 paper):

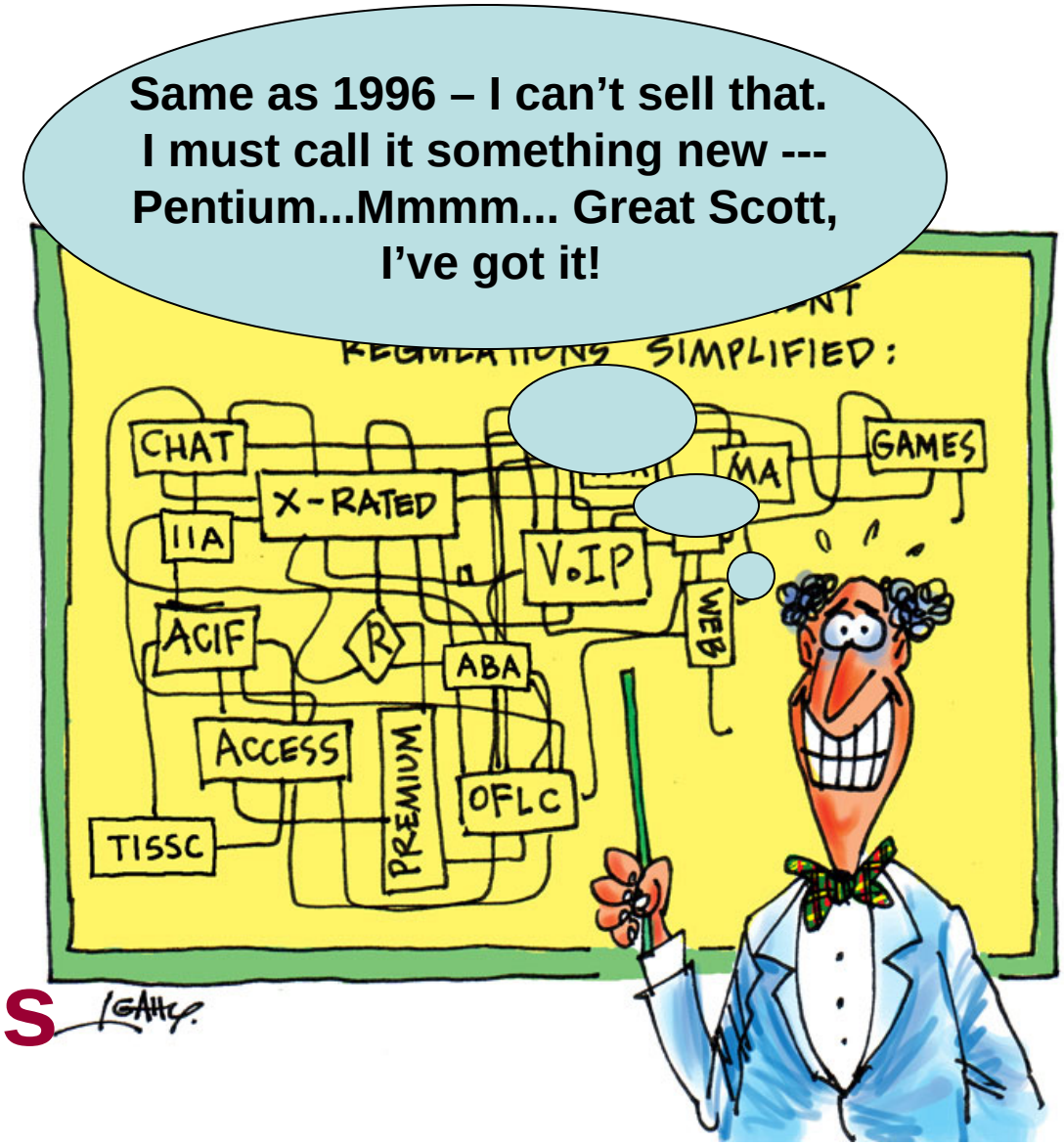
~~20 stages~~

P4/prescott:

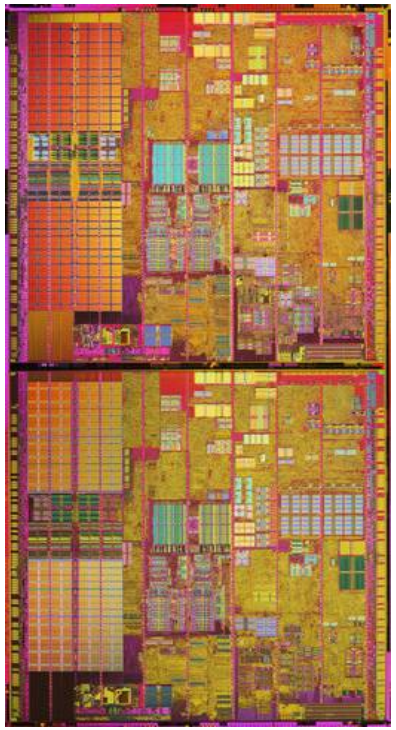
~~31 stages~~

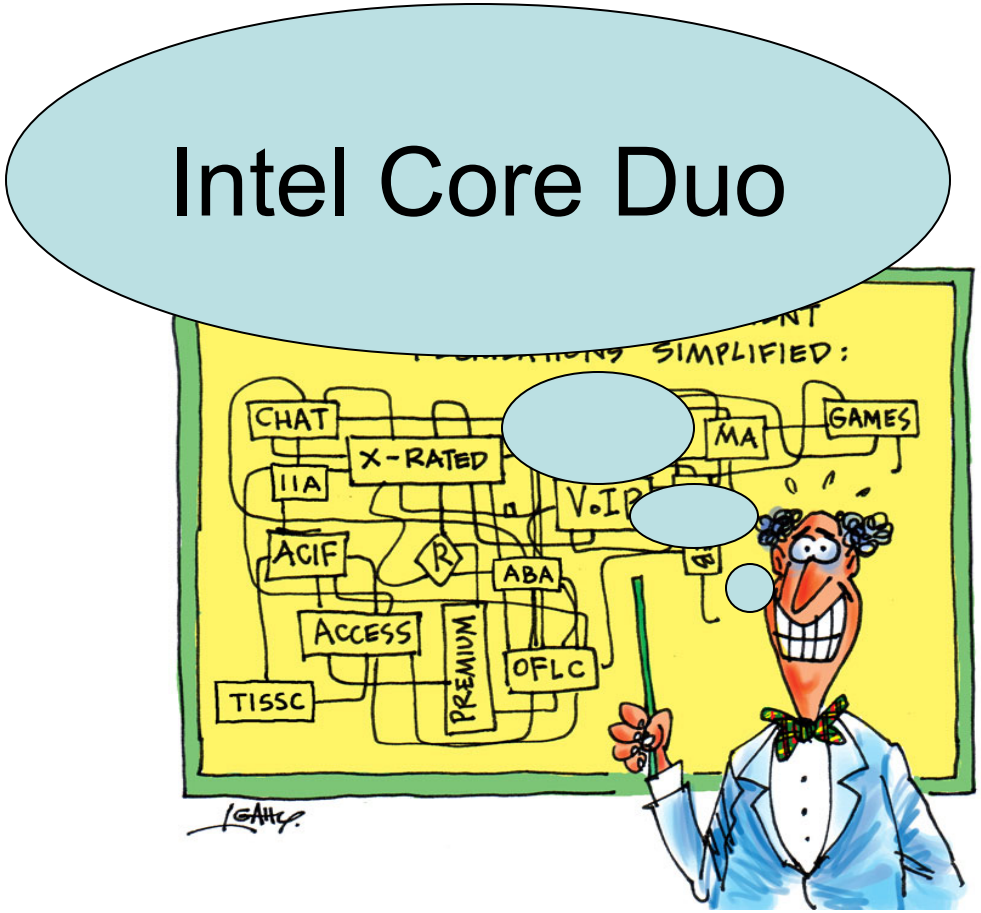
P5/Tejas:

~~>> 31 stages~~



And forward to multi-core





Future outlook

Old Trend: Frequency

New Trend: Parallel processing

→ Intel is pushing multi-core instead of higher clocks (will we ever hit 10 GHz?)

→ good time to know something about architecture

→ your application may be feasible only if you can use the architecture efficiently

Abstractions protect us from change
-- but must also change as the world changes

Changes in application space

Virtual Homicide (Quake)

Photographic memory

Telepathic

Mathematical Genius

Etc…

Language
Compiler
ISA
Micro Architecture
Register-Transfer Level
Circuits
Devices
Materials Science

Physics

And on that note: PC's are not the only important class of computer – in fact they are in the minority (~2%)!

Administrative Details

****

Course Work and Grading

- Let's Review the Course Website ...

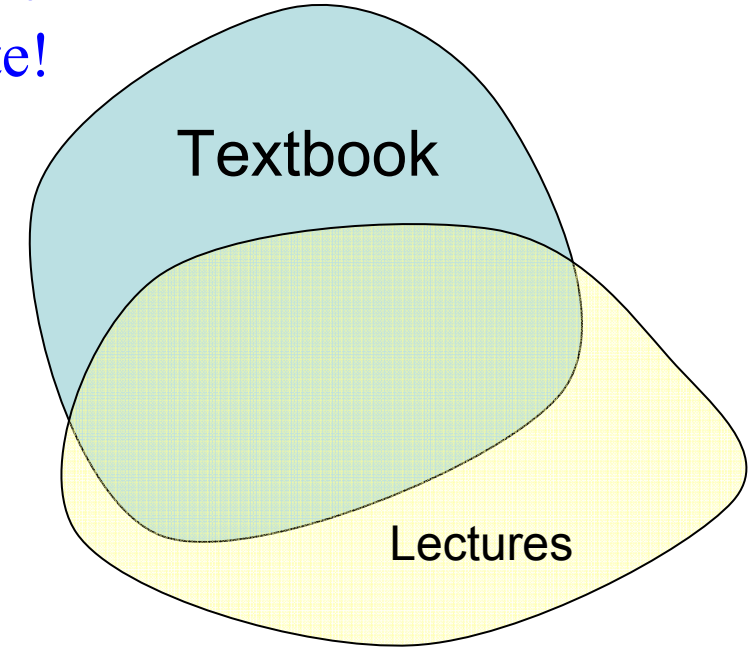
Textbook

Patterson & Hennessy, fourth edition of "Computer Organization, the Hardware/Software Interface"

- Decent book. We'll read most of it.
  - 4rd Edition, came out this year, look for errata
- Patterson is professor at Berkeley;
  - lead RISC project (foundation of SPARC processor)
  - lead RAID (redundant array of inexpensive disks) project
- Hennessy is professor at Stanford
  - now President of Stanford
  - co-founded of MIPS Computer Systems
- Note: same authors wrote the graduate textbook, "Computer Architecture, A Quantitative Approach".

Text vs. Lectures in CSE 141

Assigned readings for each lecture posted on website!



- Lectures will include material not in the text…text will include material not in the lectures.

- Resource limitations prevent us from addressing material from the prerequisites in office hours…but we are happy to refer you to the book or your classmates.

How to find out your deliverables

- Check the website. Generally, we won't necessarily announce readings or assignment due dates in lecture.

  http://www-cse.ucsd.edu/classes/sp10/cse141/

- You will have assigned reading for every lecture except when you have an exam.

Please watch the website for course updates, reading assignments and homework assignments!

Course Staff

Instructor: Michael Taylor

Lectures: Tu/Th

TA: Matt Devuyst

Discussion sec: Wed

Question Triage: Who to ask which Question

Me:

"In lecture, …"

"I'm designing my own supercomputer, and…"

Matt:

"On problem 5, …"

Arash:

"In the Altera environment, … "

Me+Matt:

"In a 2-way set associative cache…"

"In the book, …"

Me+Arash:

"In my 141L Implementation, …"

.. and of course, talk with your classmates!!

Am I Qualified to Teach You?

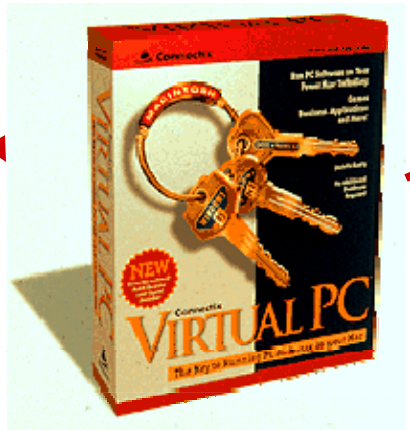
- PhD, MIT, EE & CS
  - ten years at MIT studying processor design
  - 2 years consulting for chip companies
  - various research publications

Architectures designed: 4
Machines Implemented: 3
Millions of units of software shipped: > 1
Million-gate chips designed: 1
Supercomputers designed: 1

About Me

PowerMush 3

PowerMush IV



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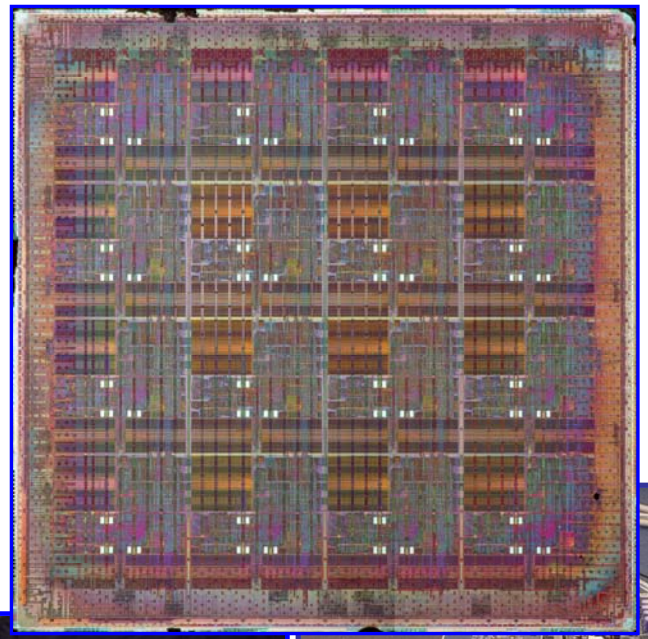
UCSD

About Me



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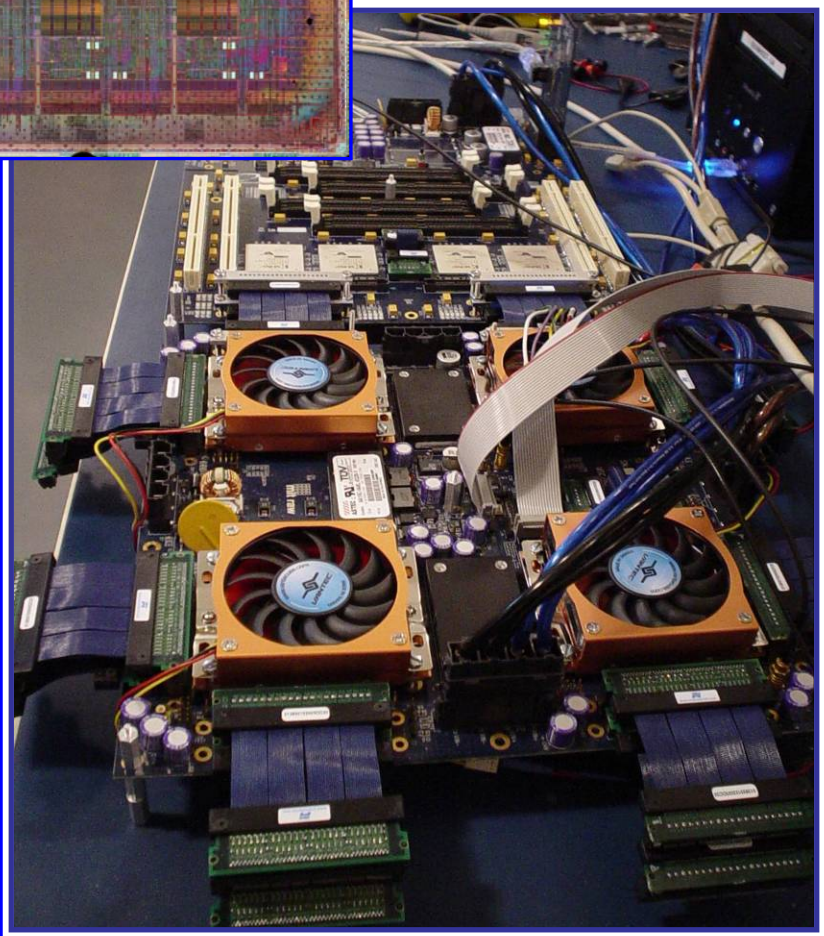
~120 million transistors