

6.17 Reduce the number of states for the FSM in Figure 6.91 by using an implication table.

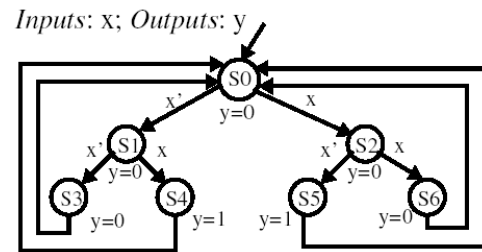


Figure 6.91: Sequence detector for bit patterns “01” and “10”

S1	S4,S2 S3,S1				
S2	S6,S2 S5,S1	S6,S4 S5,S3			
S3	S0,S2 S0,S1	S0,S4 S0,S3	S0,S6 S0,S5		
S4					
S5					S0,S0 S0,S0
S6	S0,S2 S0,S1	S0,S4 S0,S3	S0,S6 S0,S5	S0,S0 S0,S0	
	S0	S1	S2	S3	S4

First Pass

S1	~~S4,S2 S3,S1~~				
S2	~~S6,S2 S5,S1~~	~~S6,S4 S5,S3~~			
S3	~~S0,S2 S0,S1~~	~~S0,S4 S0,S3~~	~~S0,S6 S0,S5~~		
S4					
S5					S0,S0 S0,S0
S6	~~S0,S2 S0,S1~~	~~S0,S4 S0,S3~~	~~S0,S6 S0,S5~~	S0,S0 S0,S0	
	S0	S1	S2	S3	S4

Second and Final Pass

Inputs: x ; Outputs: y

