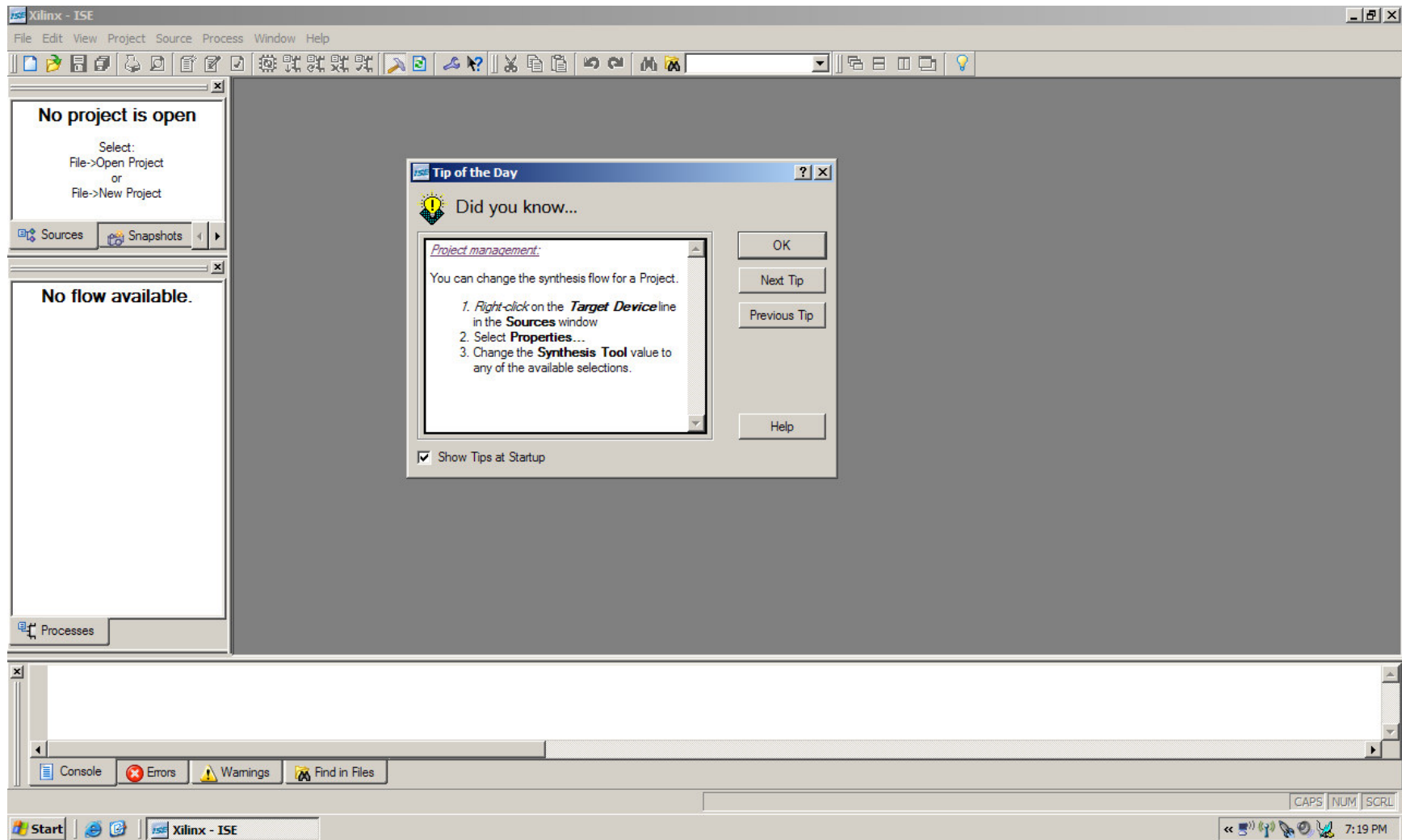
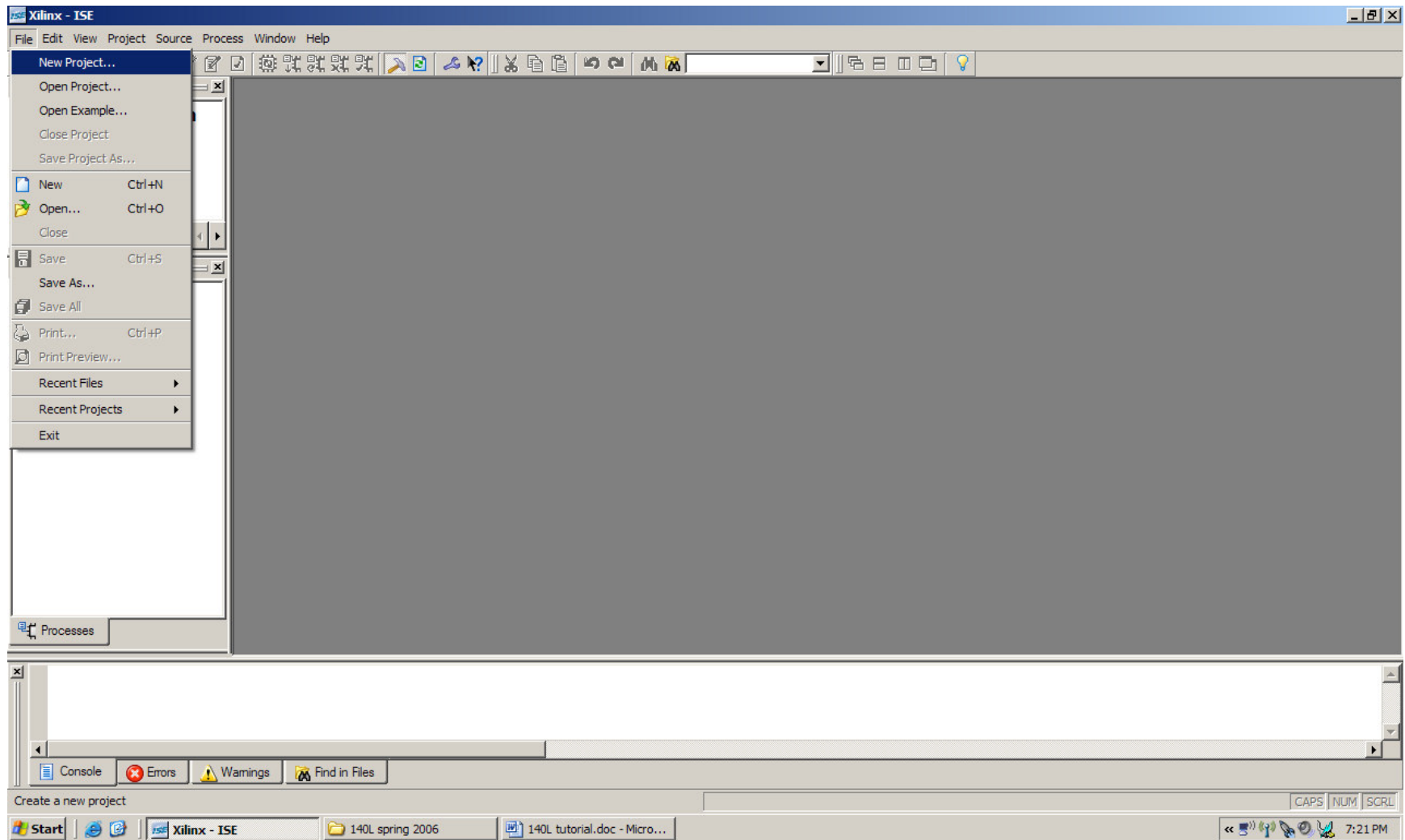
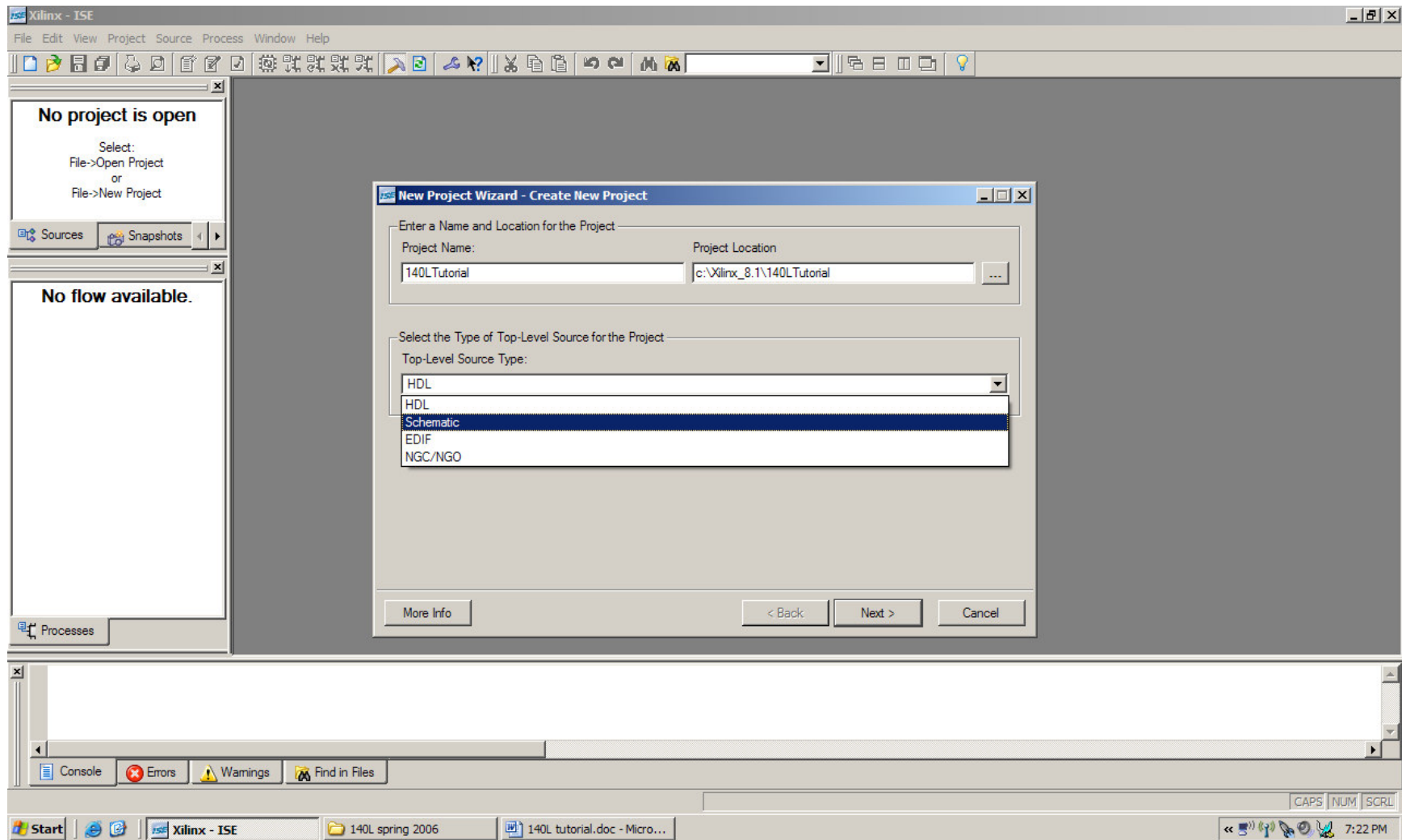




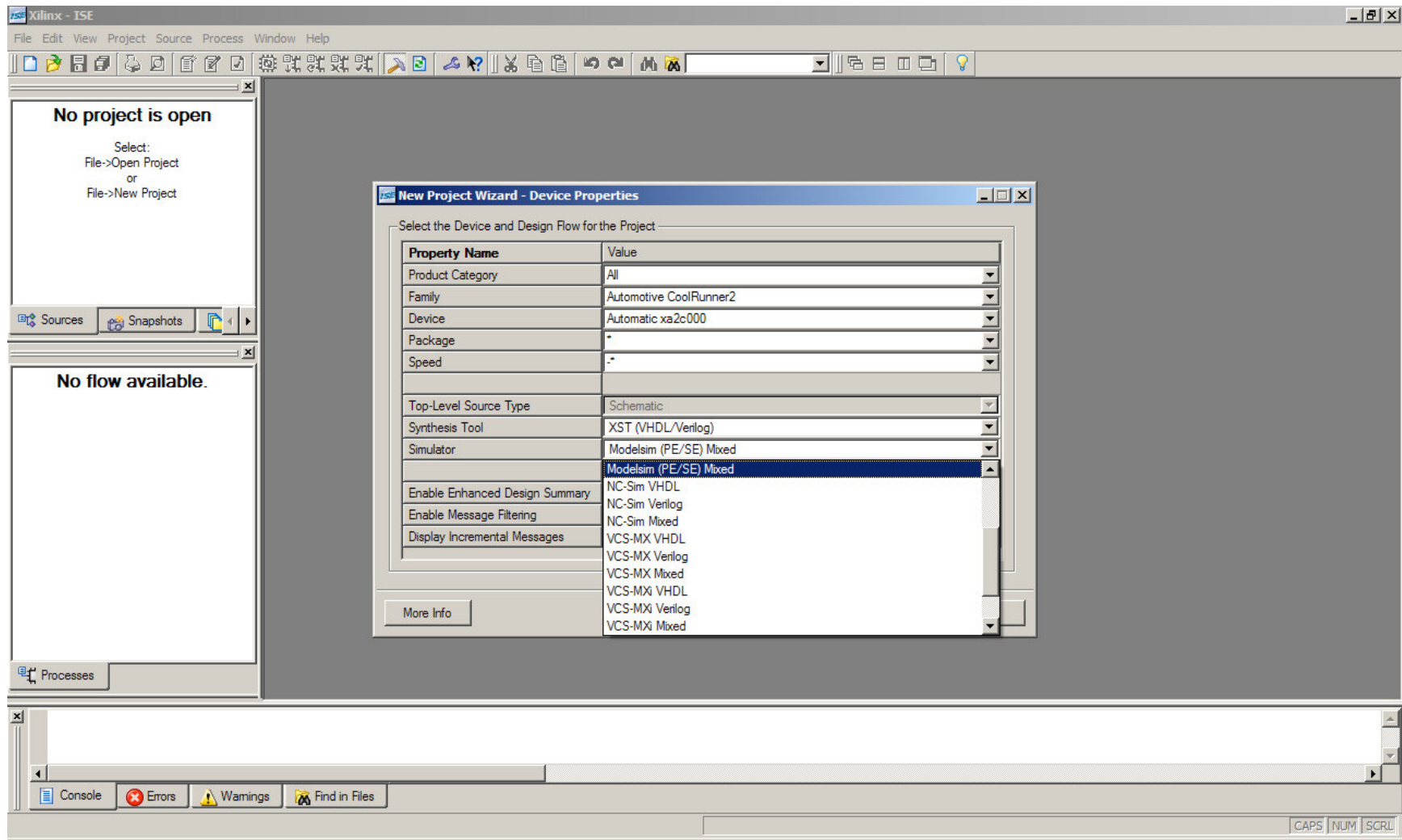
After opening the Programs> Xilinx ISE 8.1i > Project Navigator, you will come to this screen as start-up.



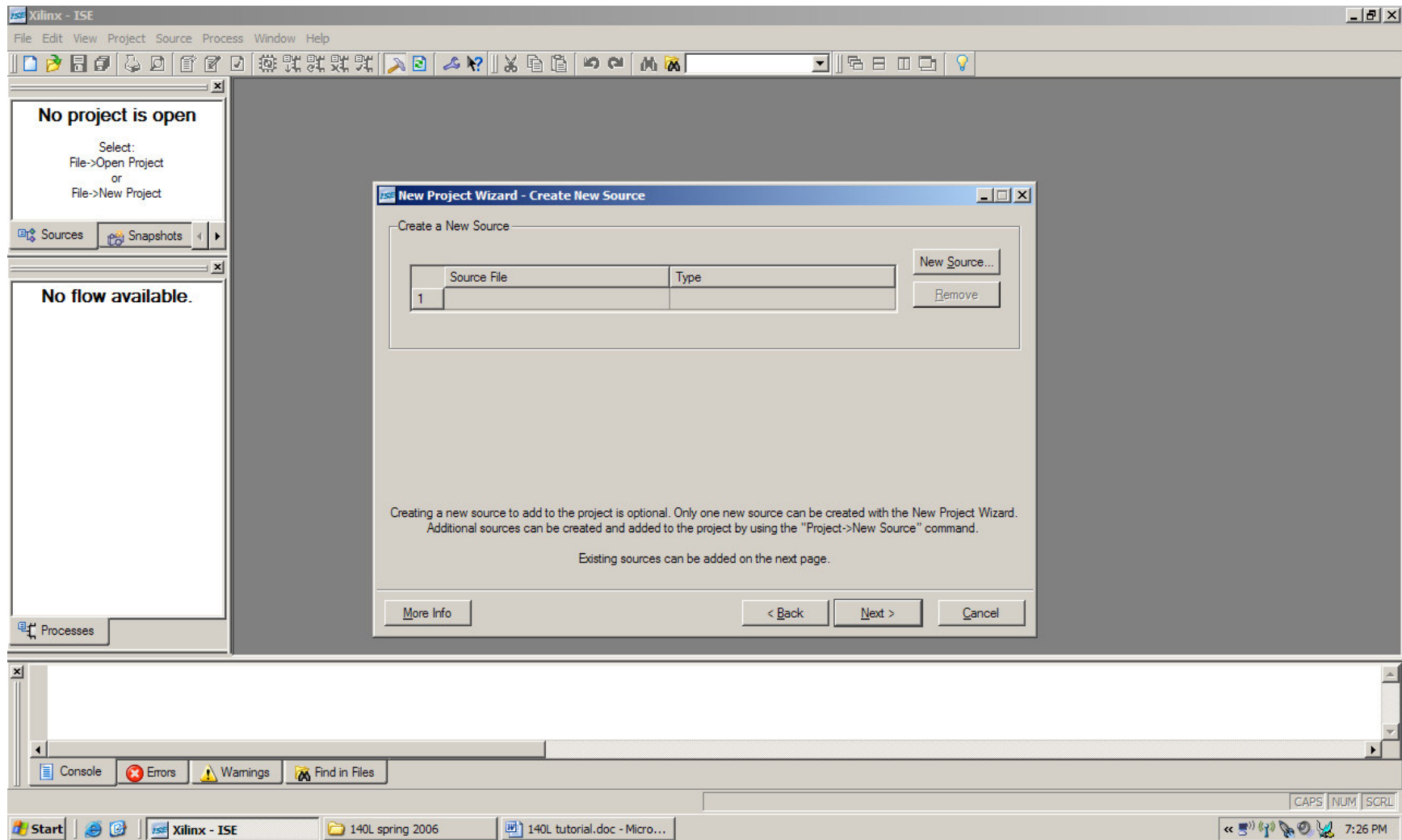
Start with a new project.



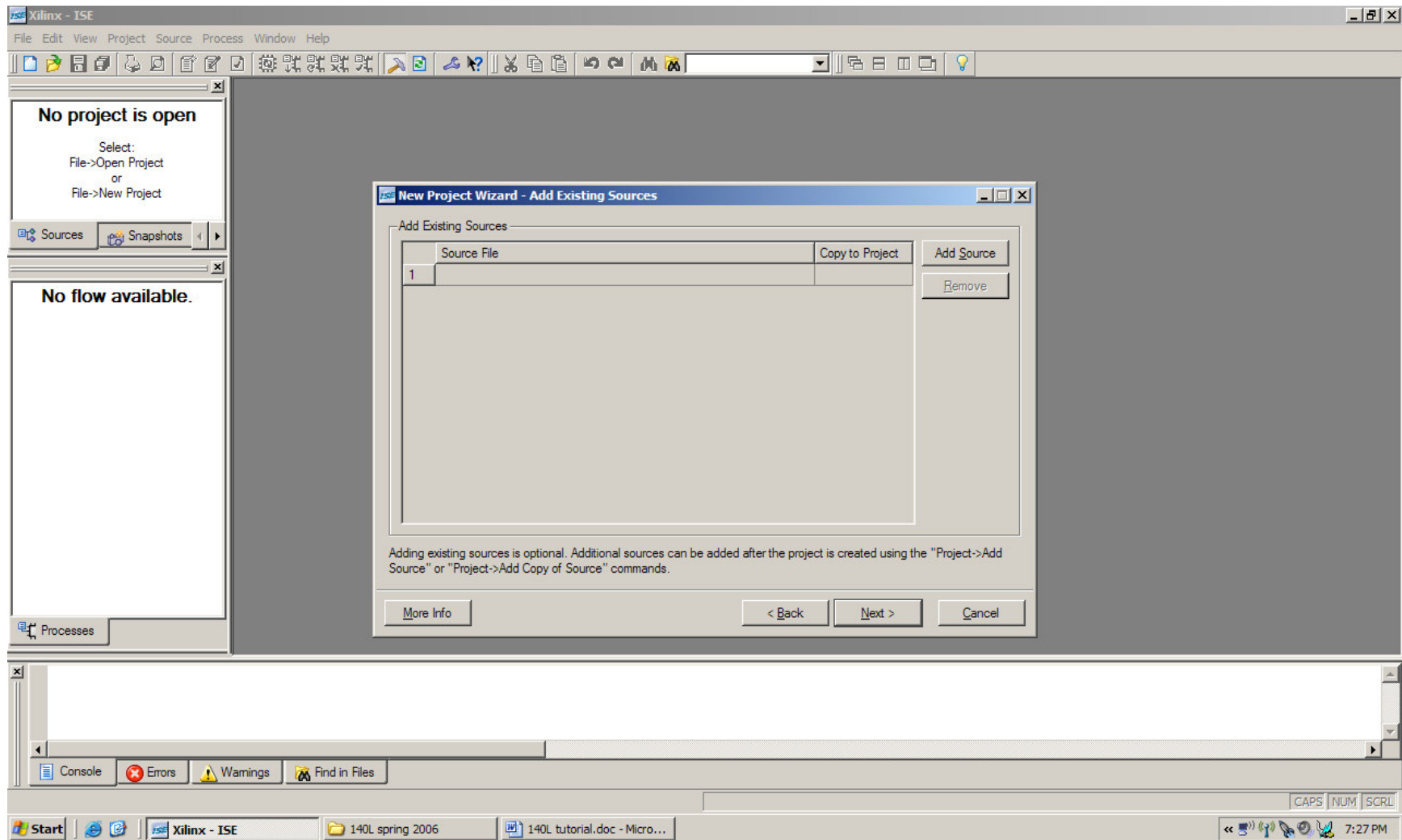
Enter a project name and be sure to select “Schematic” as the Top-Level Source Type and click Next.



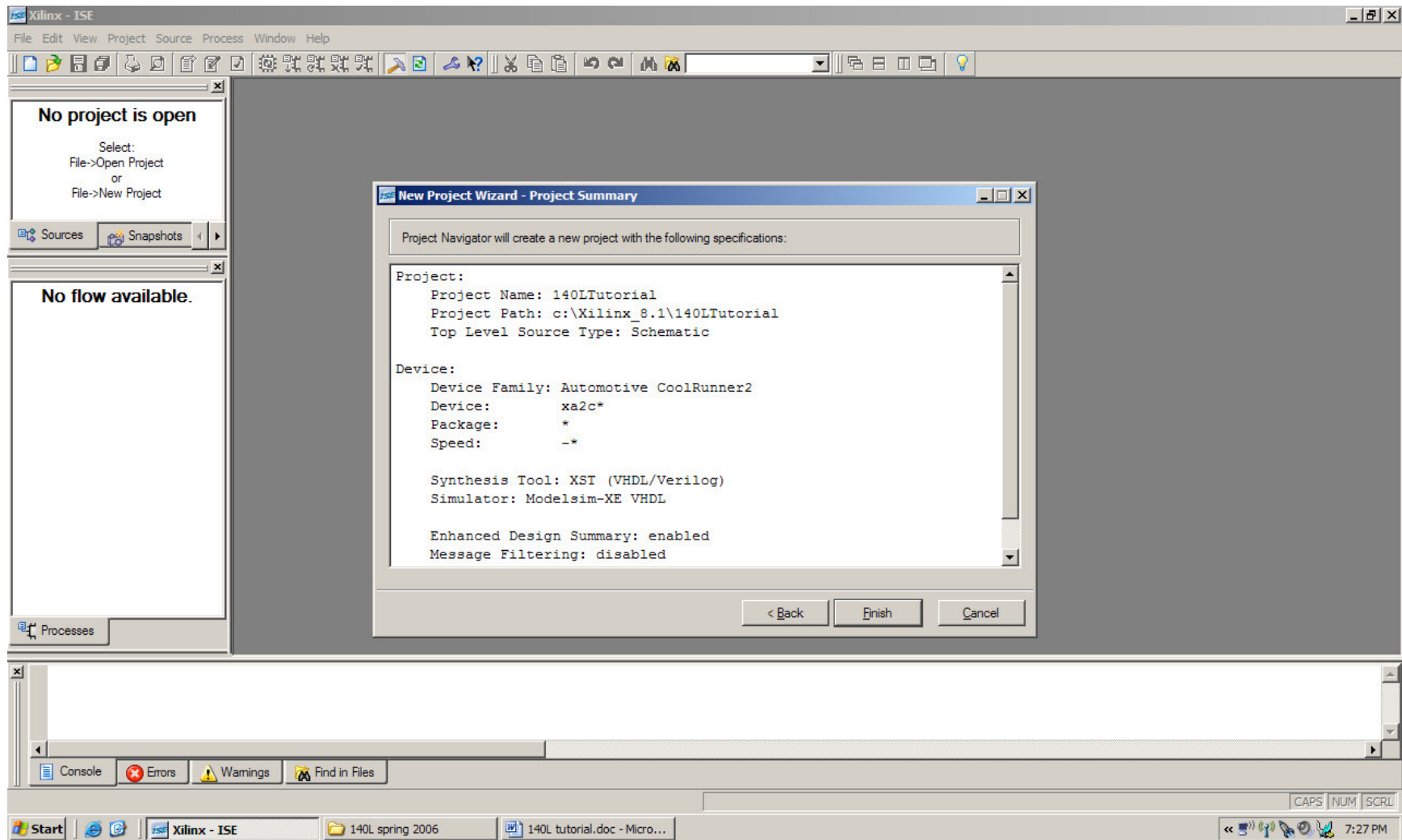
Make sure your Simulator is the **ModelSim (PE/SE) Mixed** otherwise your simulation will not work. Leave everything else as default for now. You may change these setting later also. Click Next to continue.



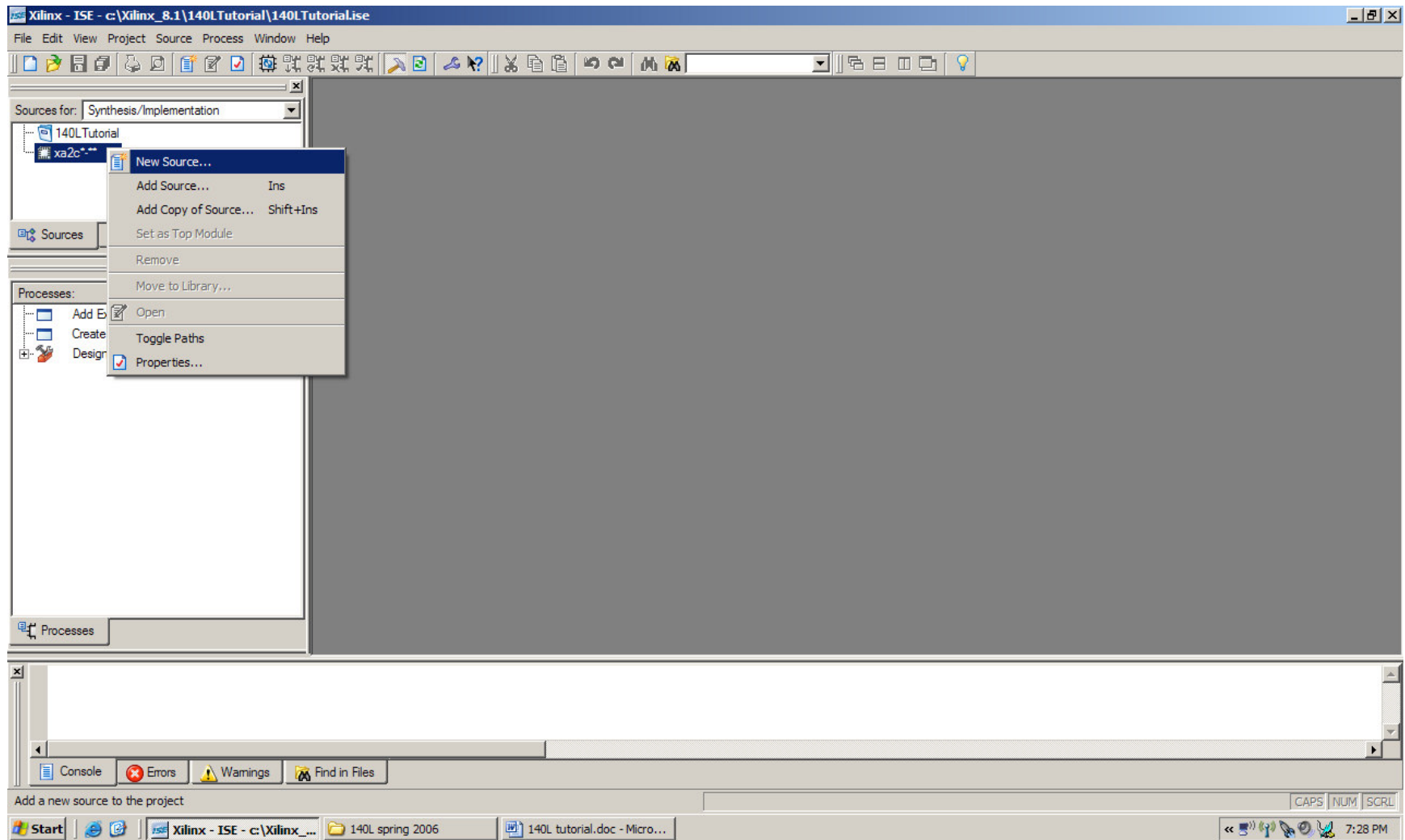
You don't need to create any new files at this time because you can add files later. Click Next to continue.



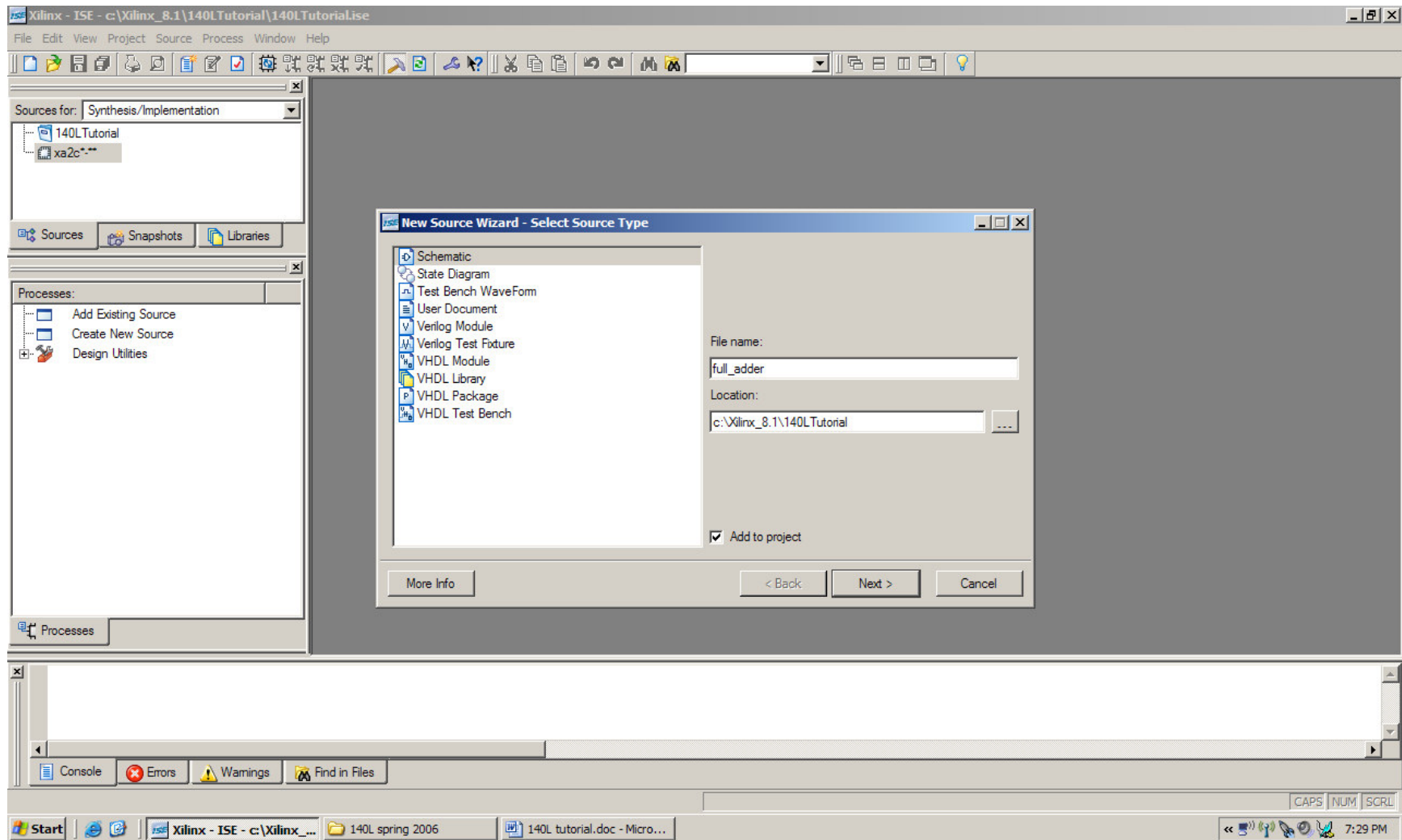
You don't need to add existing files either. So click Next to continue.



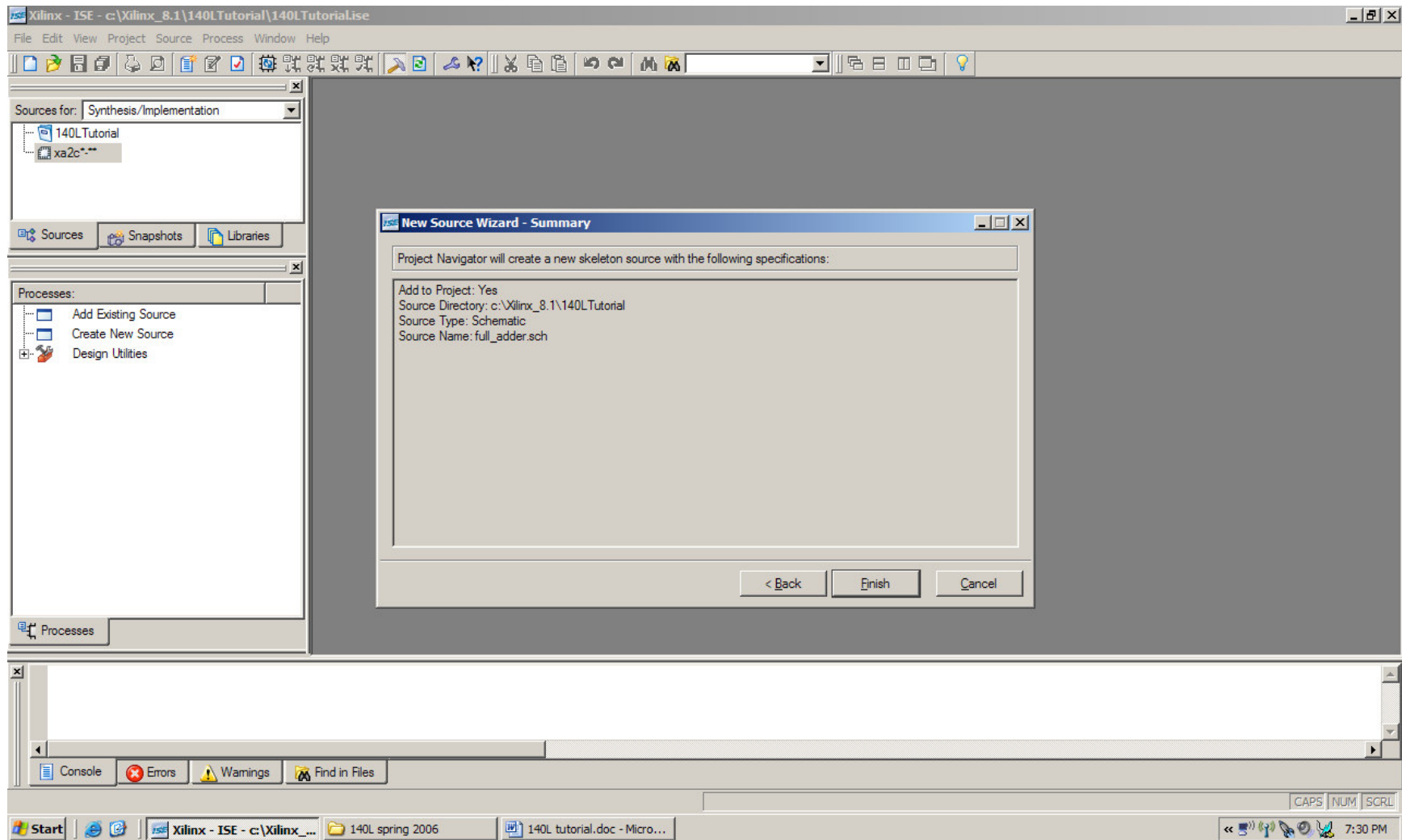
This is a quick summary of what you are creating for the project. Click Finish.



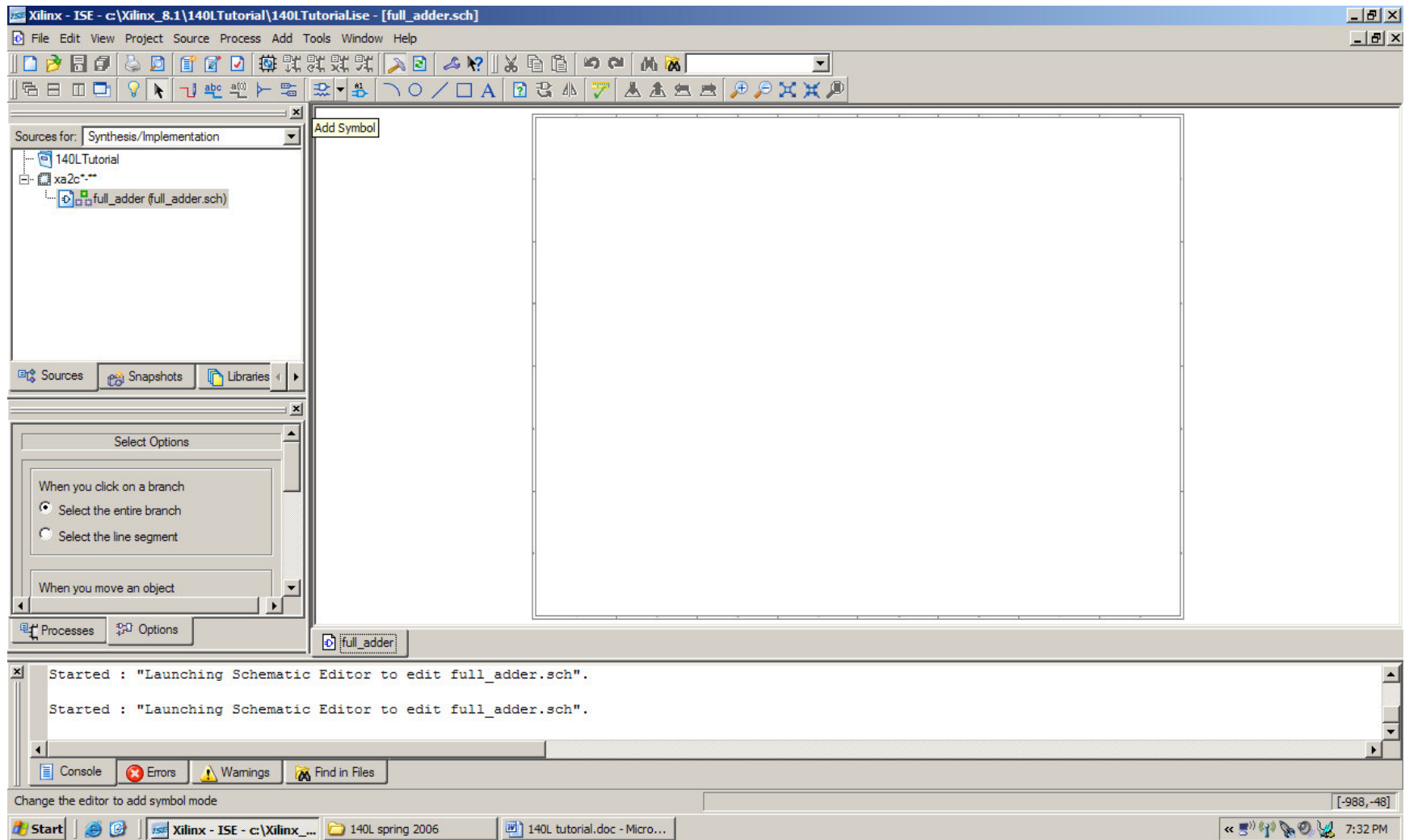
Now, you can add a new Source. Let's build a simple full-adder.



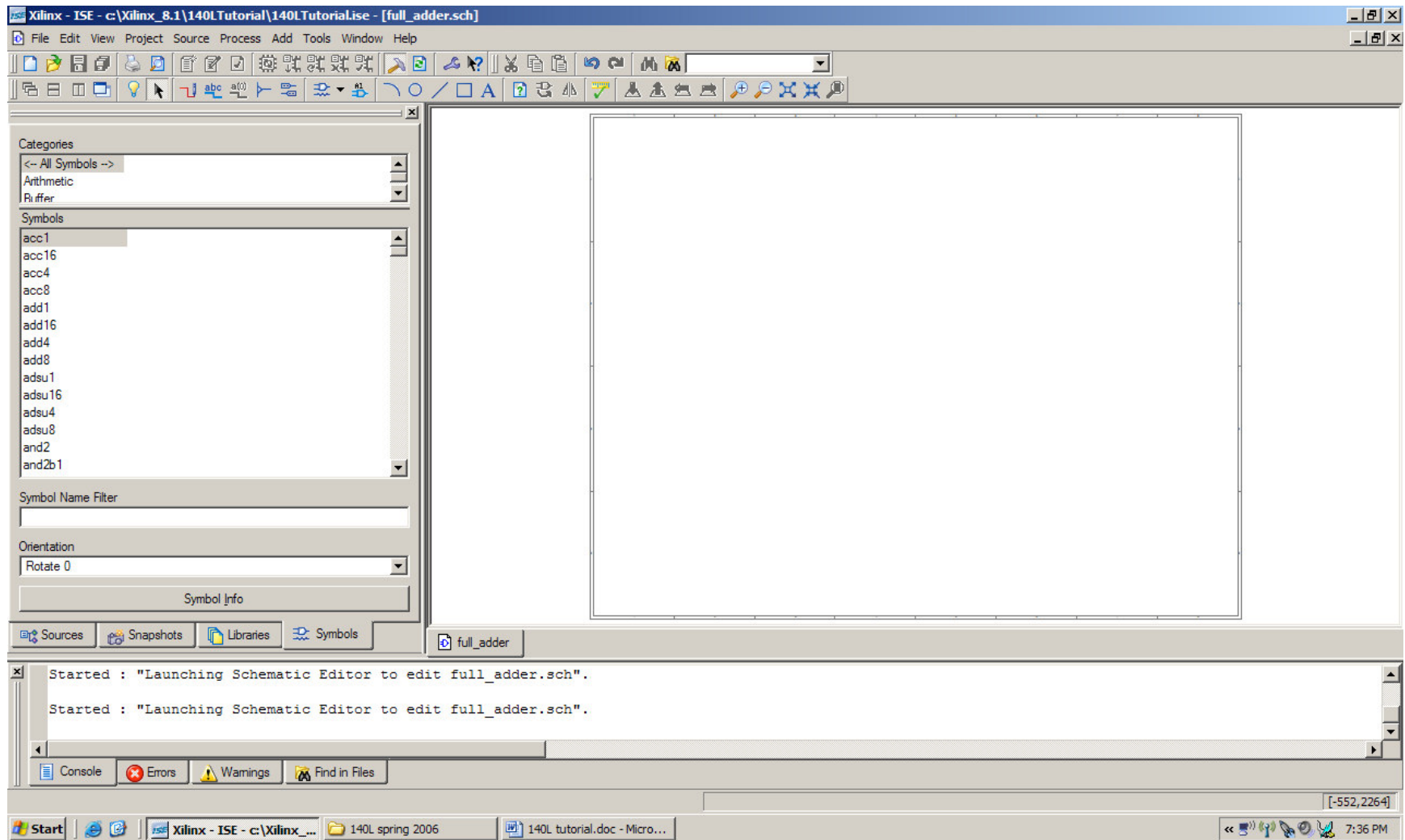
Be sure to select “Schematic” from the left-window list. Enter a file name called “full_adder” and click Next.



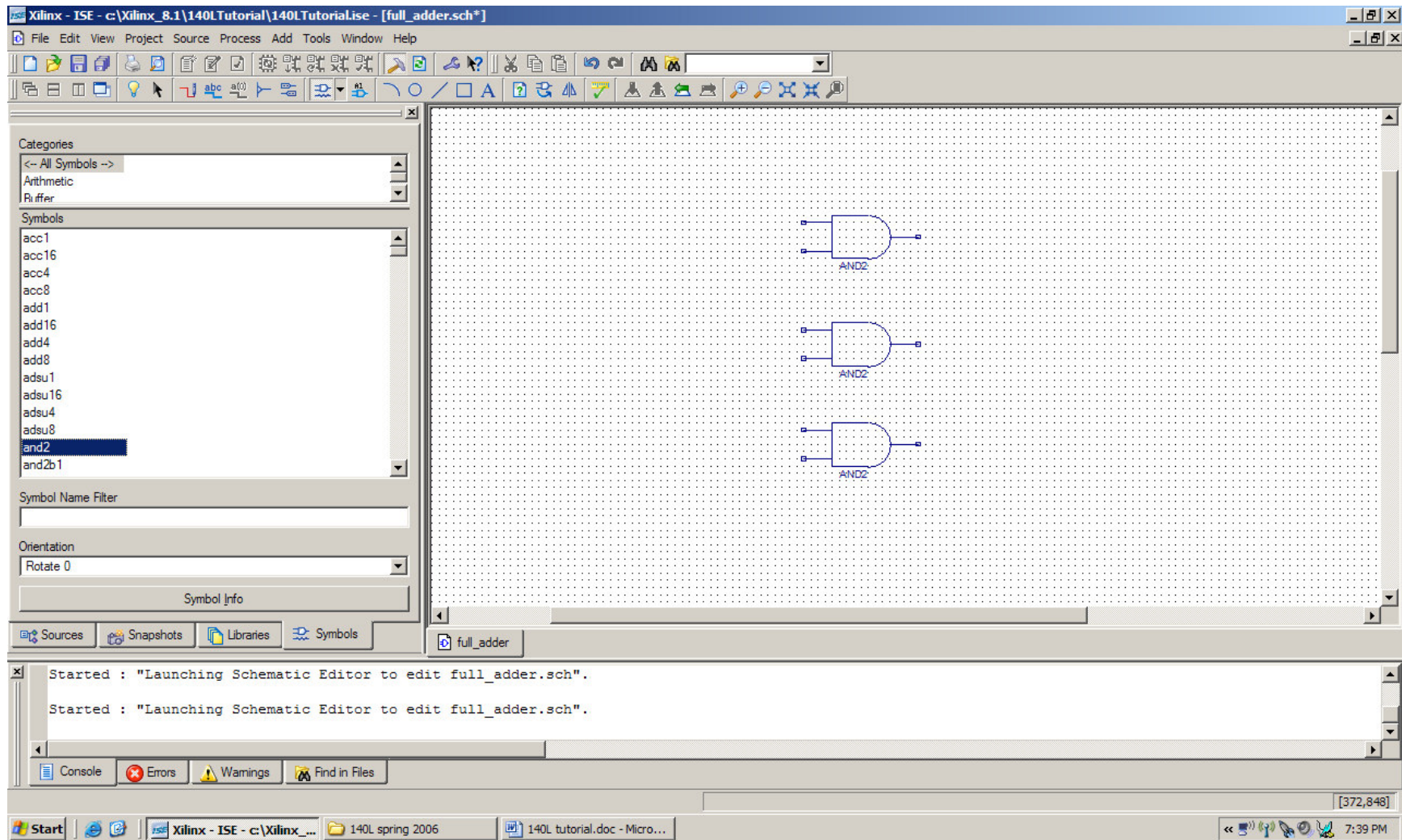
A quick summary is displayed. Click Finish.



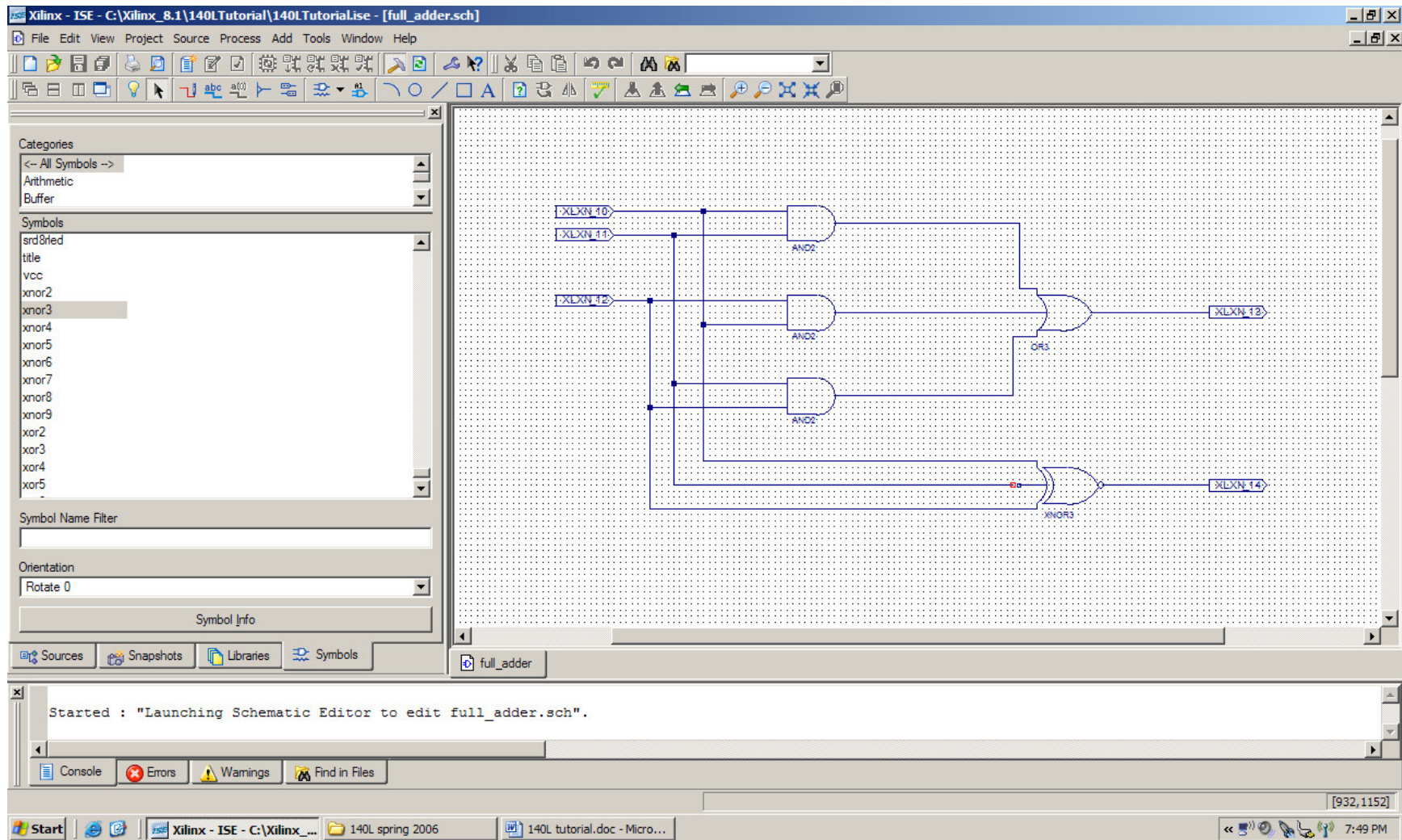
A screen with a blank schematic will appear. Now mouse over the tool bar with a “and-gate” looking symbol. The “Add Symbol” tag will appear. Click on this button.



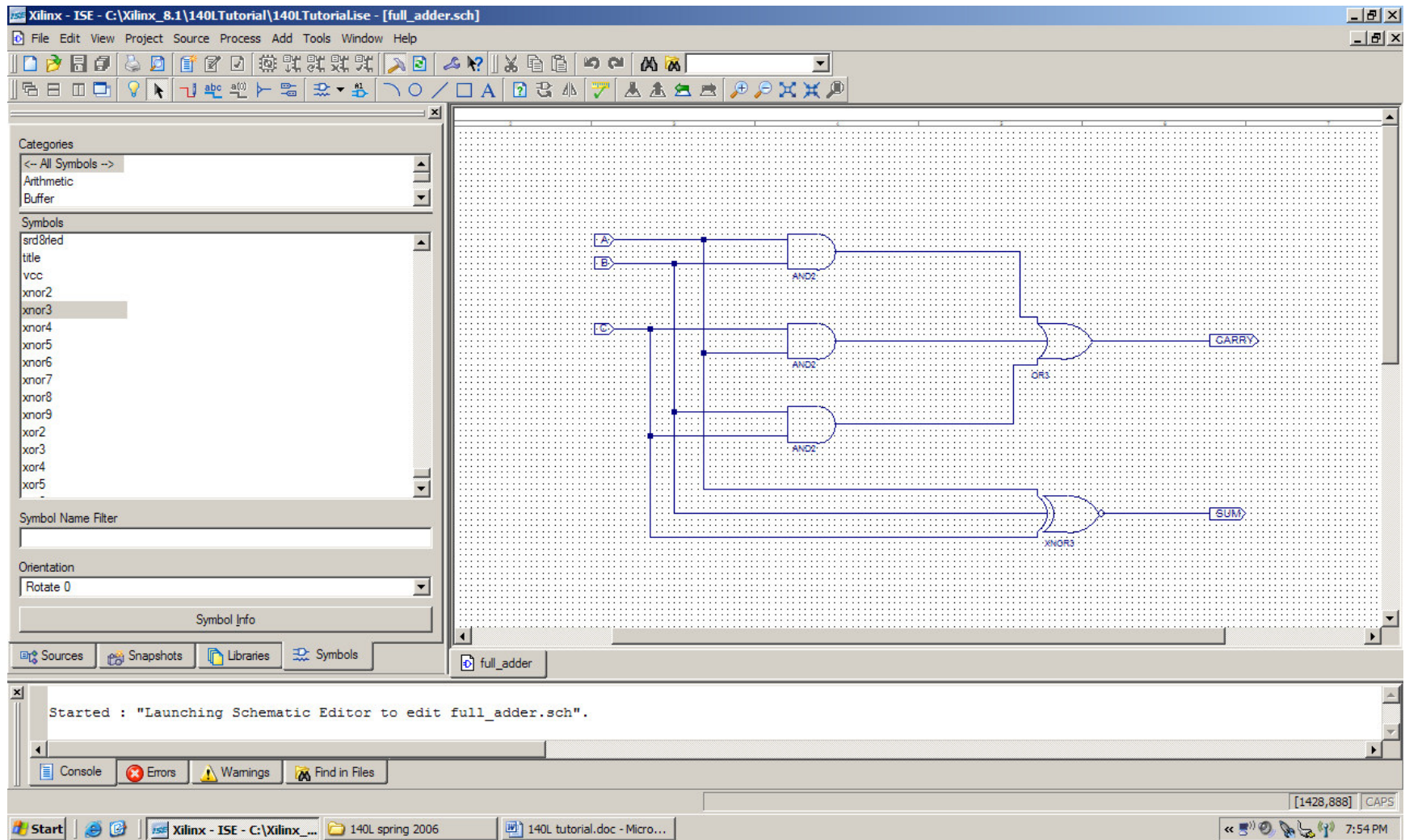
After closing down the left-bottom window and widen the left-panel a bit, you will see the Symbol list better. This is a list of logic gates which is available for the device “xa2c*.***” which we originally selected by default when we started the project.



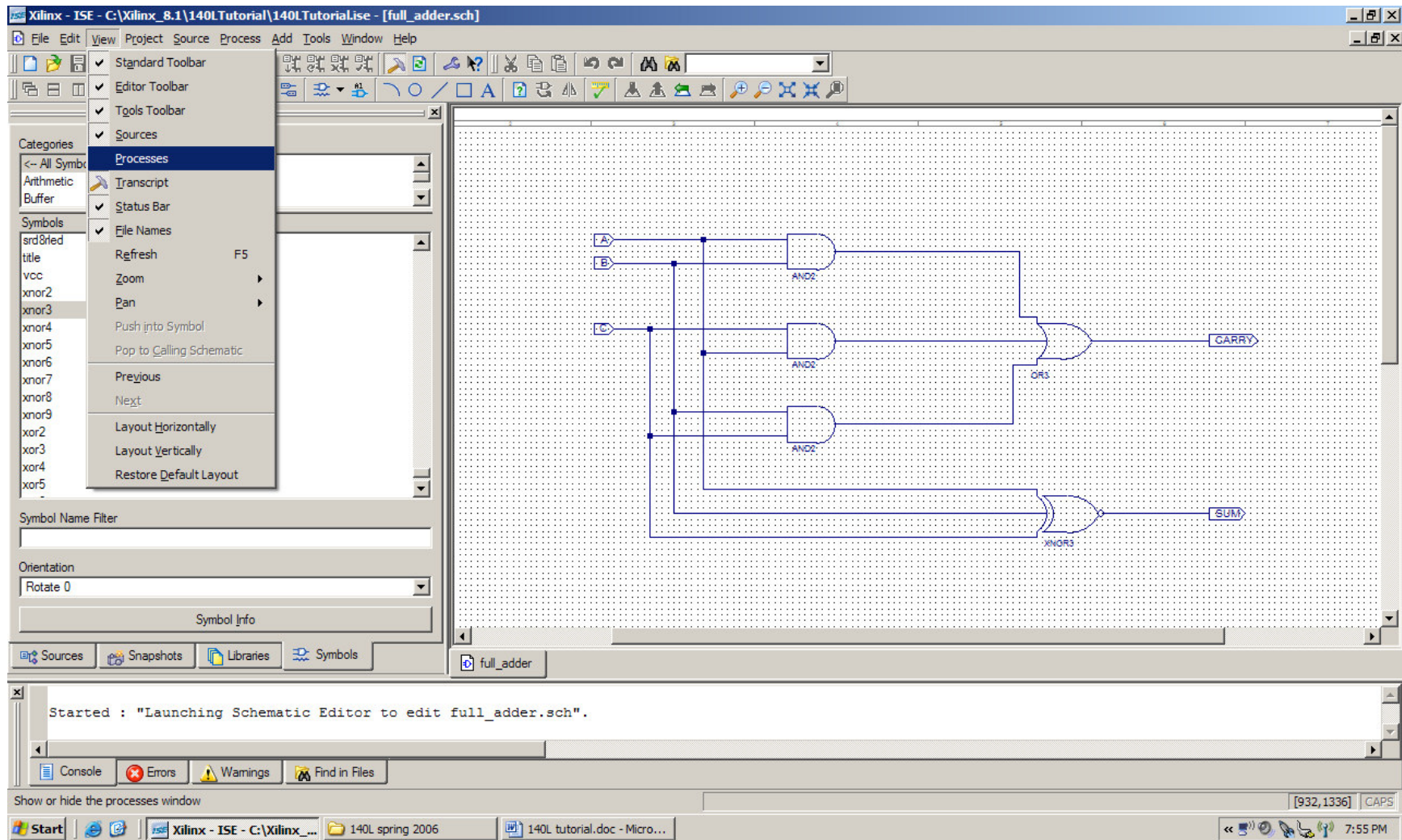
Let's select the and2 gate (2-input and-gate) and put three of them on the schematic area. You can zoom in and out of this schematic editor with the zoom button.



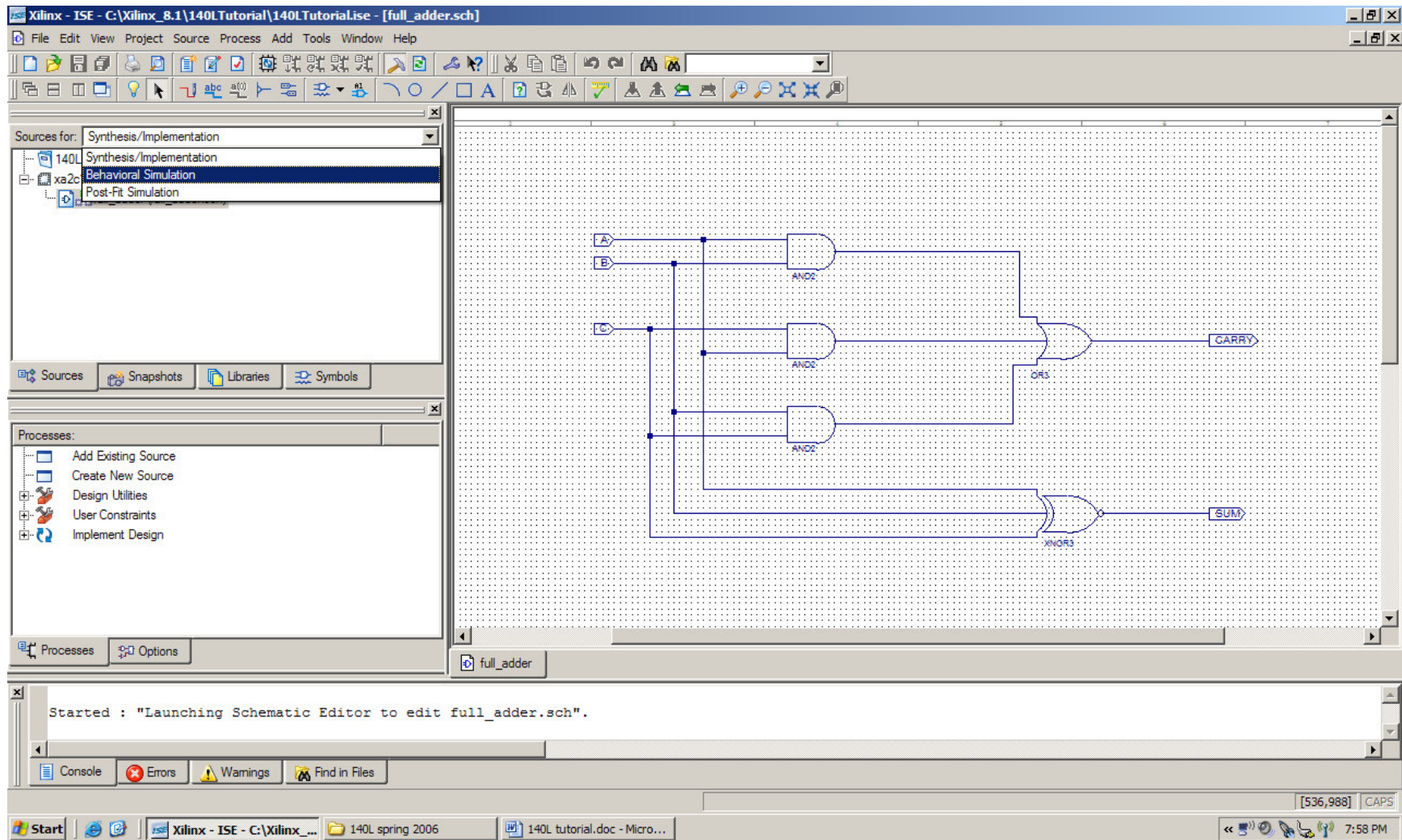
Now we added the or3 gate and xor3 gate. Then, use the “Add Wire” button to add wires to the input of the xor3 gate. And use the “Add I/O Marker” to add inputs and outputs. To connect wire, you can click once at the begin point and double-click on the end point. Do a little experiment here to see different way to connect wires. Notice when wire did not connect to the input of a logic gate (in this case xor3). You can also right click on the I/O port to rename.



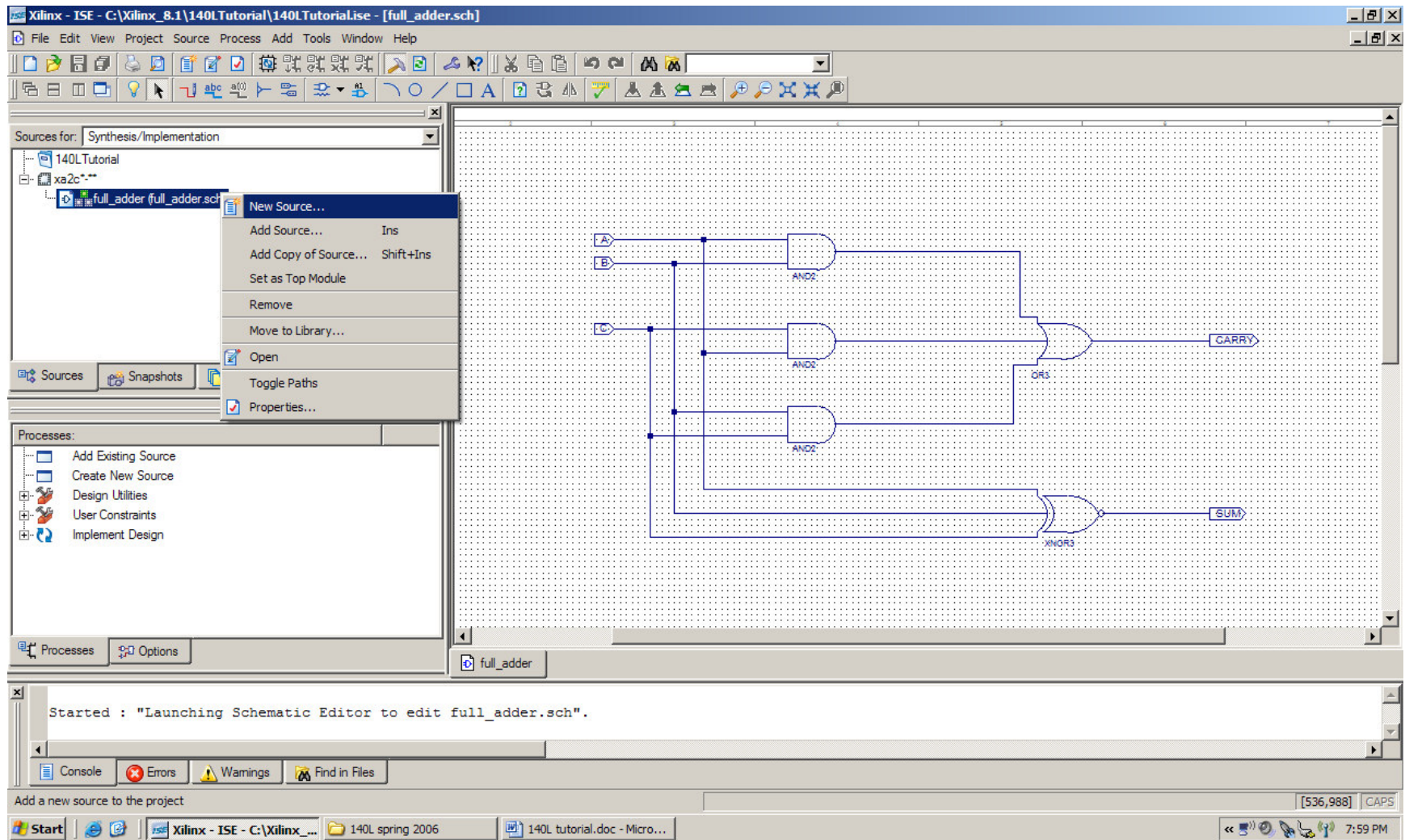
After connecting the wire to the xor3 and renaming the port, this is our final layout of the circuit. You should now save your work.



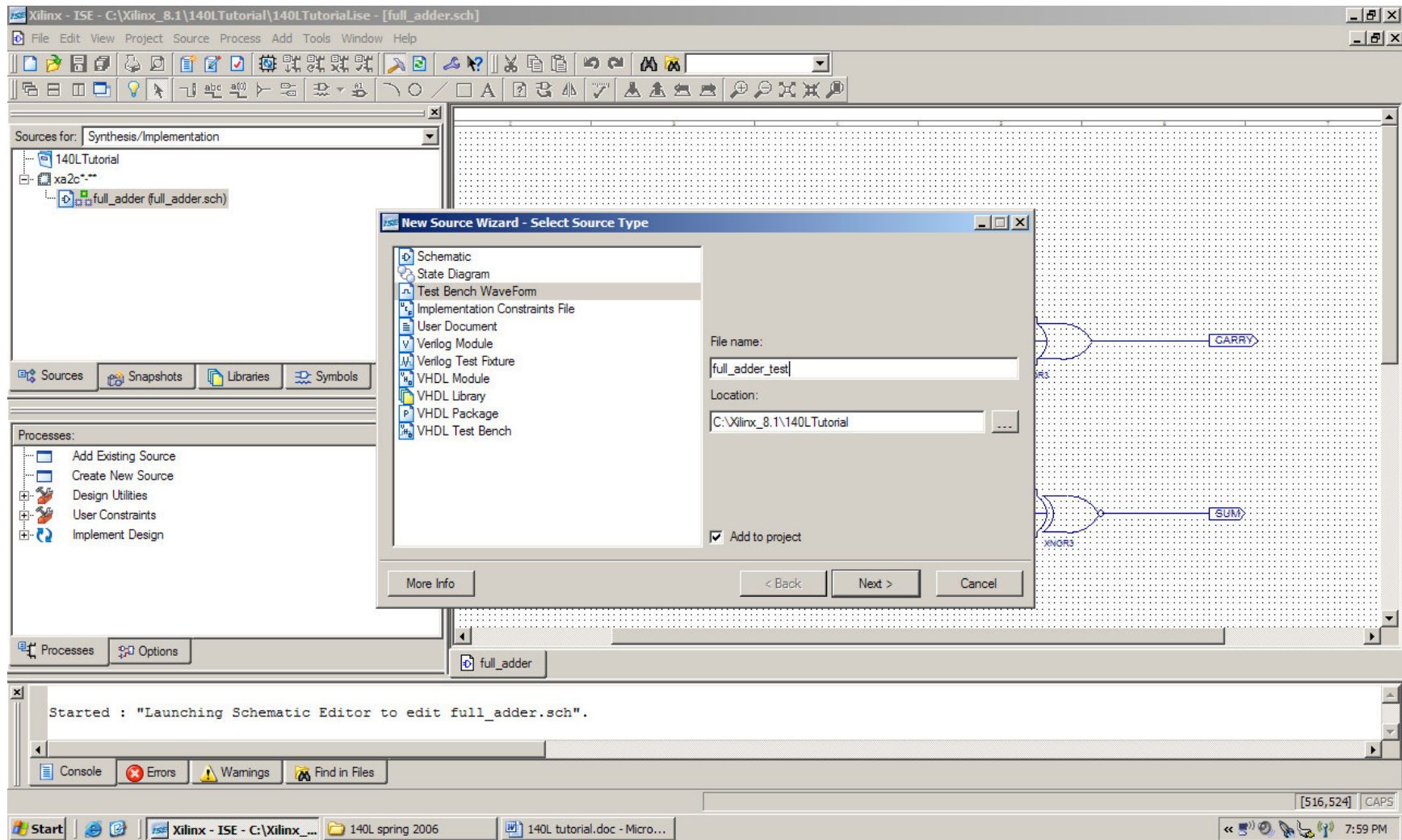
Because we have close down the Processes window earlier to make room for the Symbols listing, let's bring it back by Menu>View>Processes. There are two windows on the left pane. For upper window, click on the "Sources" tab, and for lower window, click on the "Process tab". You will get the following window.



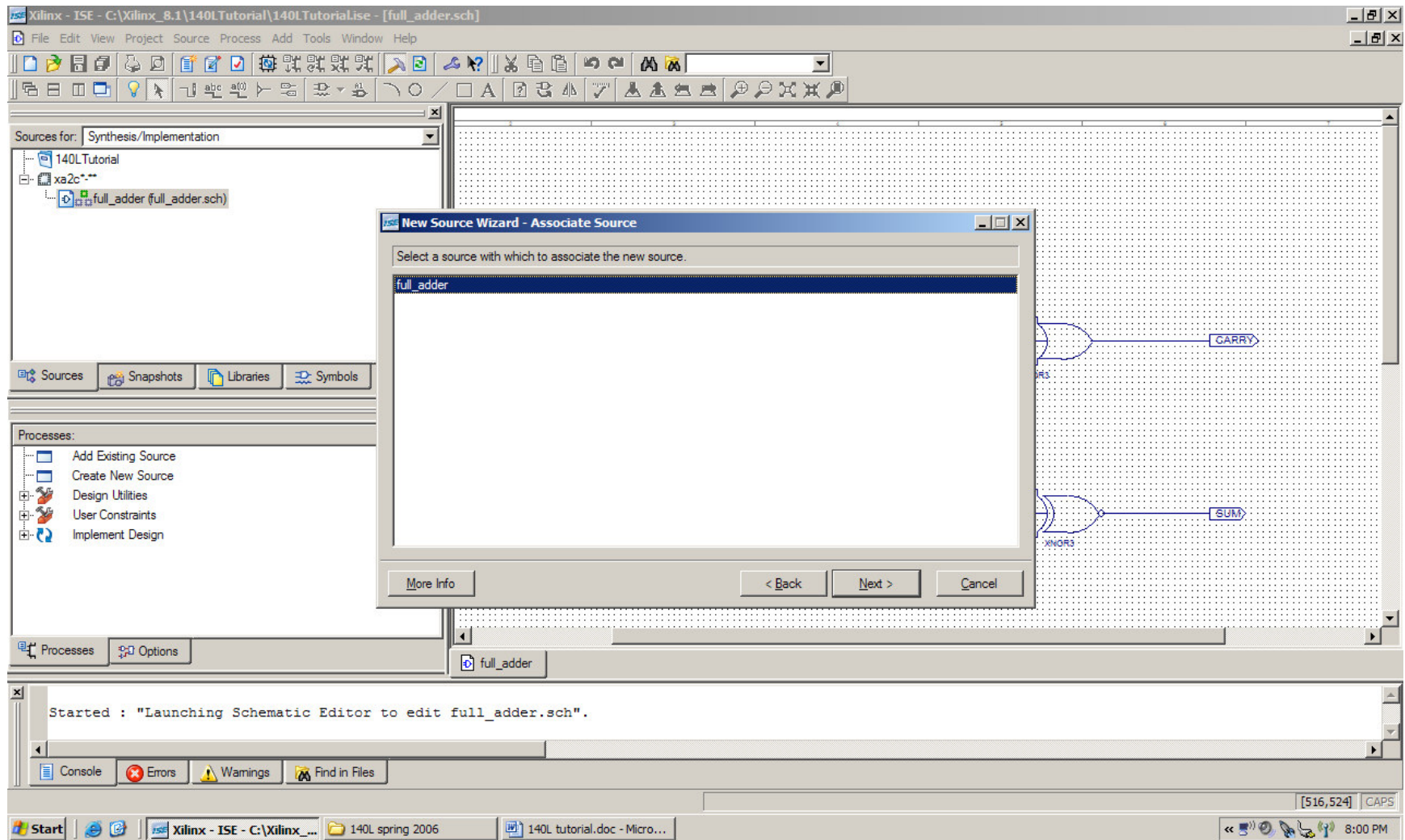
On the upper left window, select the “Behavioral Simulation” drop-down so we can get ready to create a simulation file.



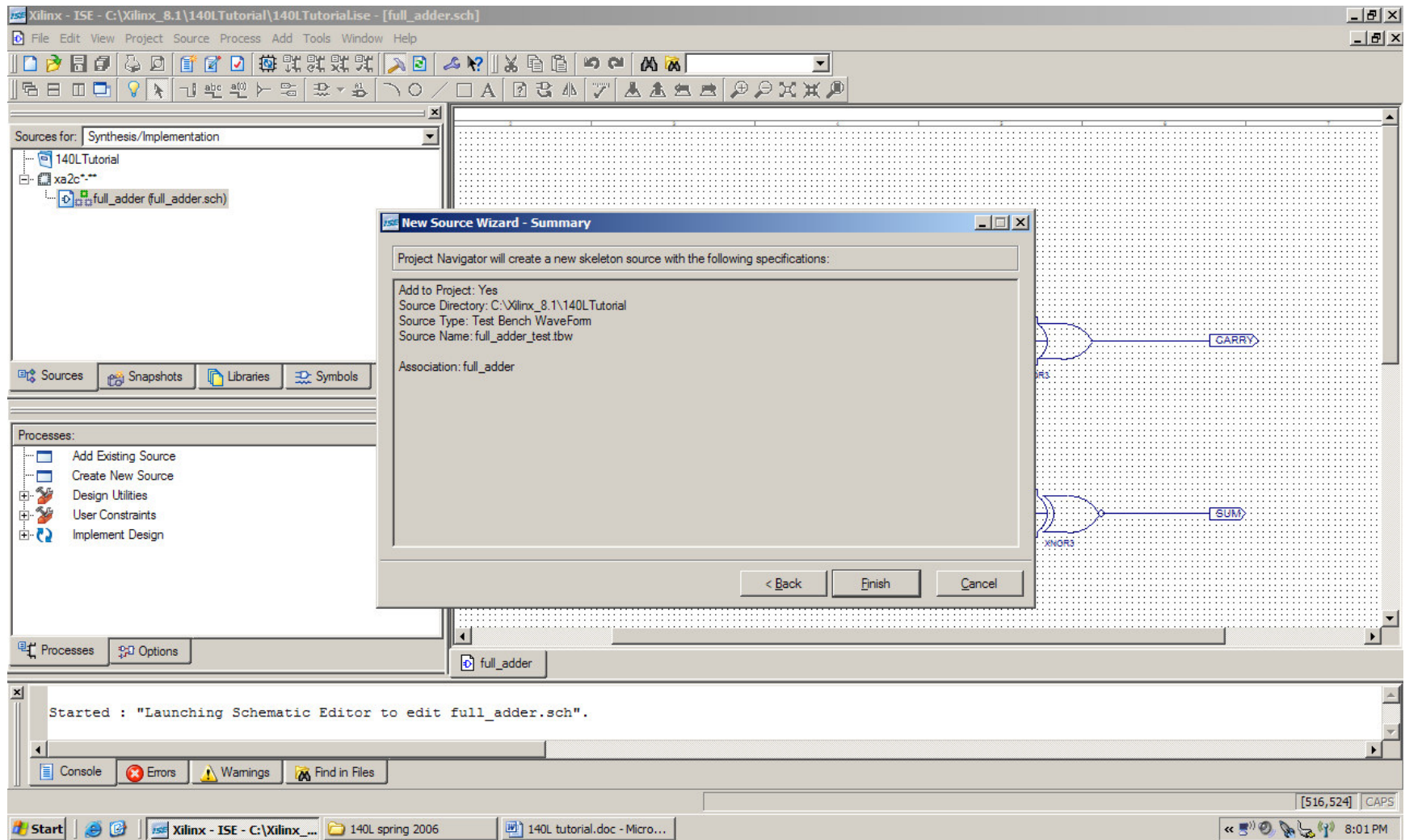
Right click on the full_adder.sch file and select “New Source”.



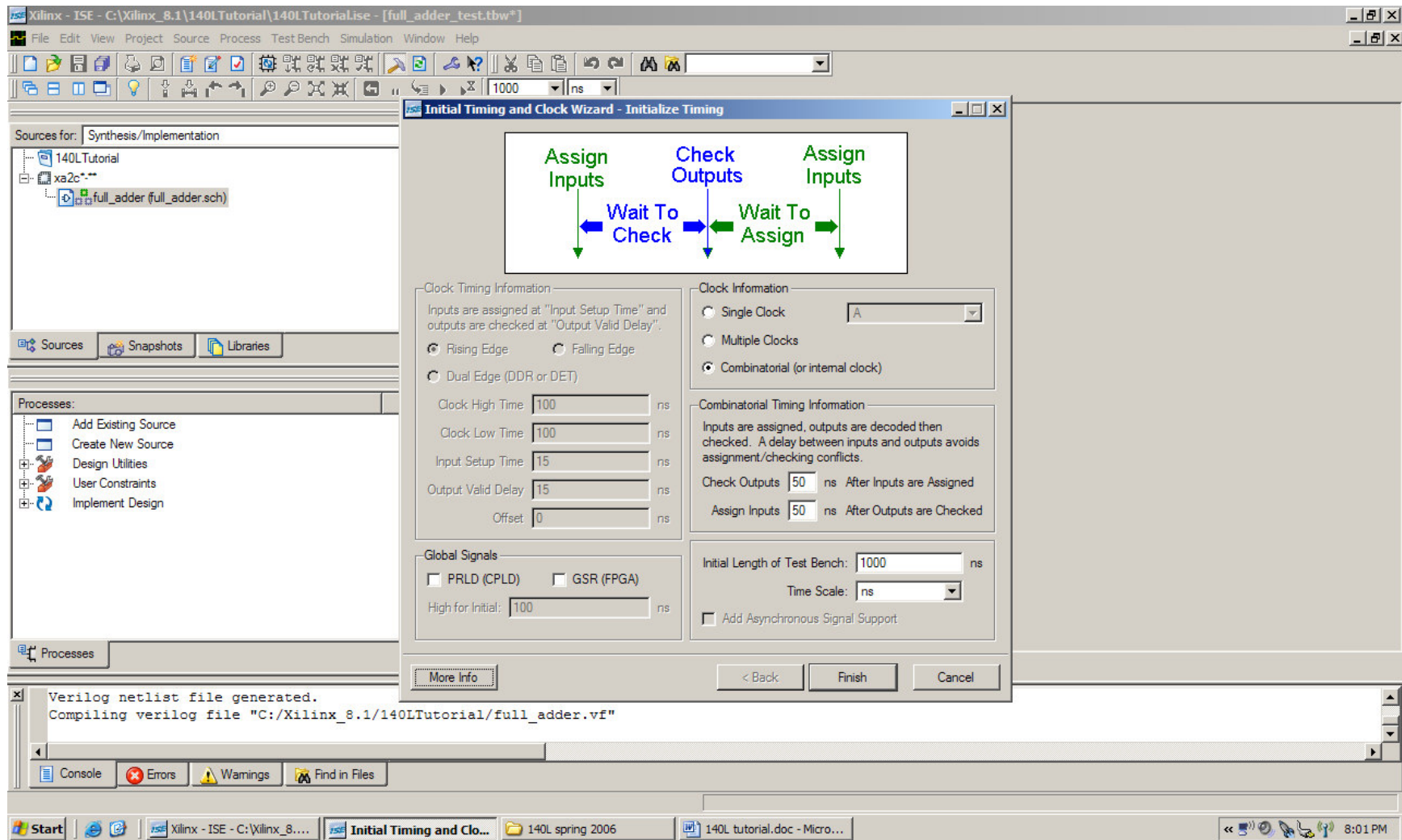
A new window opens. Select the “Test Bench WaveForm” and type in “full_adder_test” in the File name and click Next.



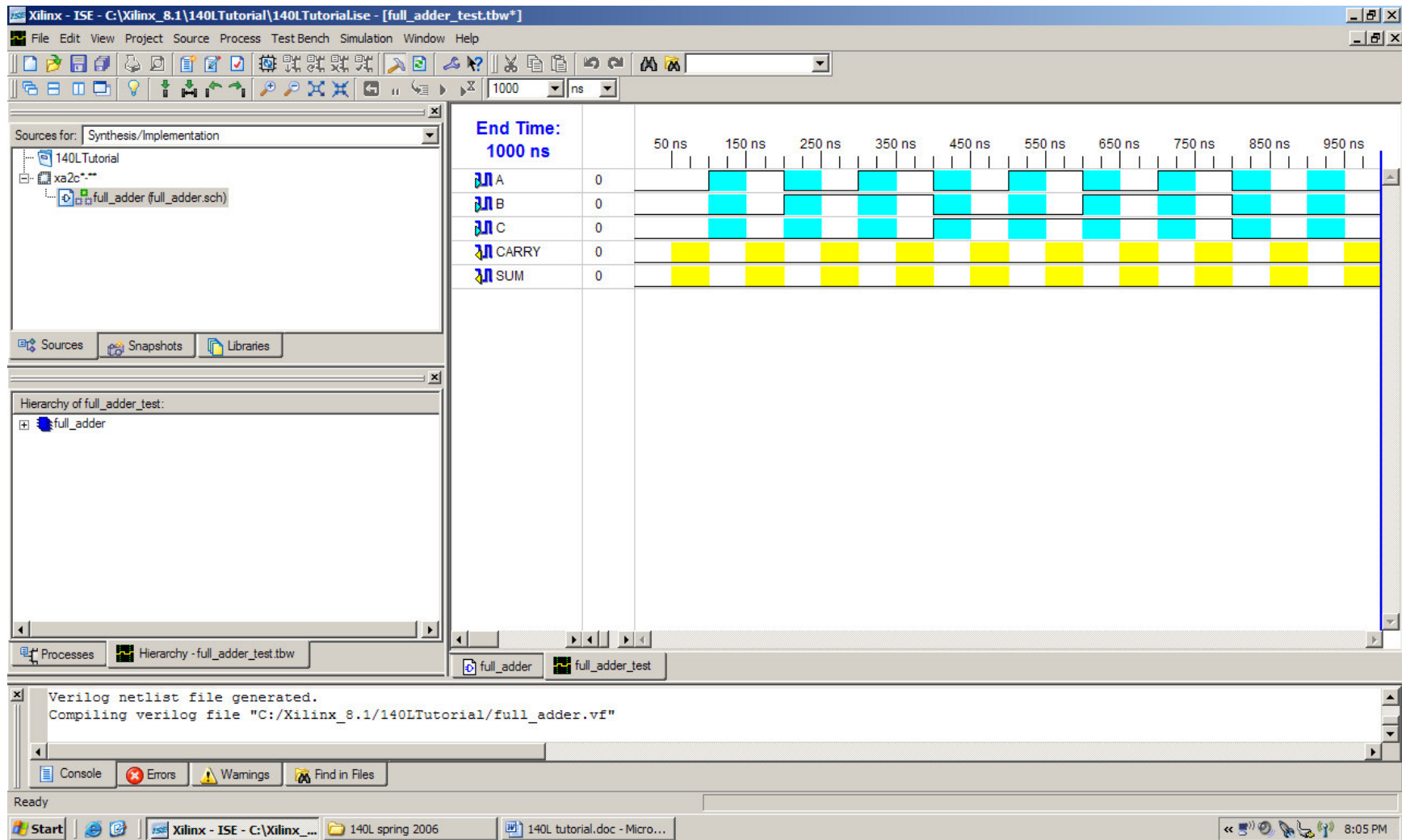
Since we want to create the test for full_adder, simply click on full_adder and then Next button.



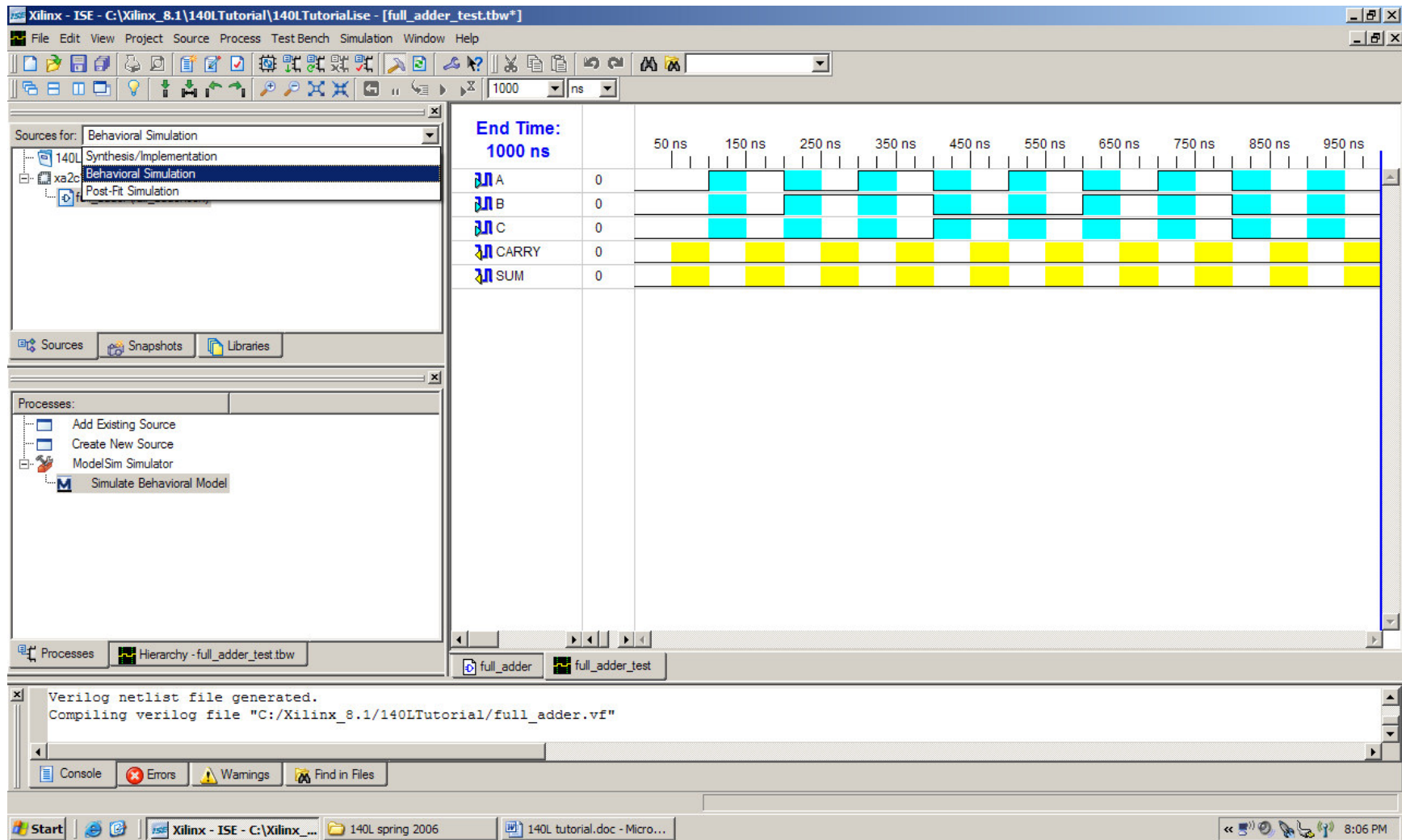
A quick summary screen display. Click Finish.



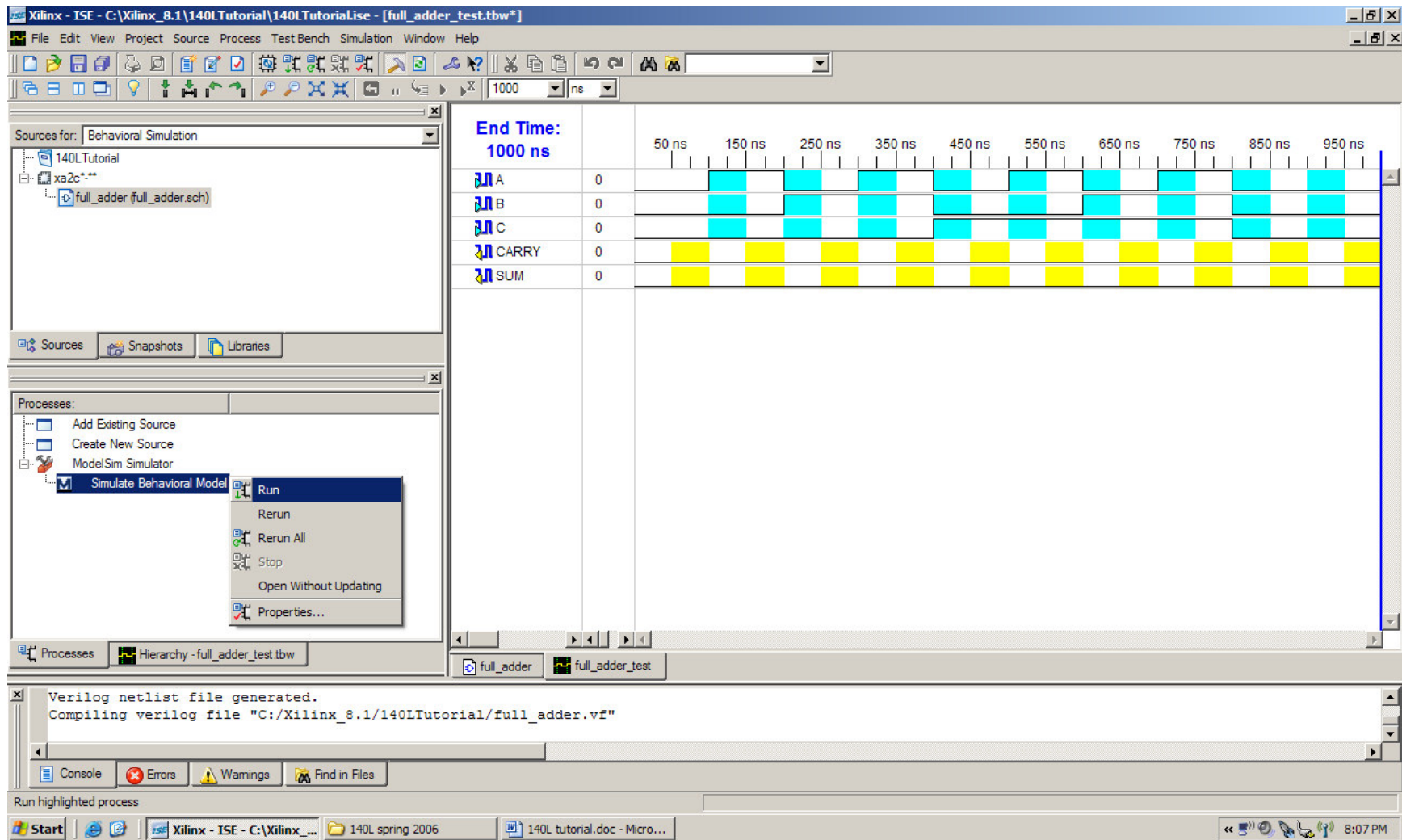
A new window opens to give you some setting on how long you like to simulate. In Clock Information, make sure to select “Combinatorial (or internal clock)” and click Finish.



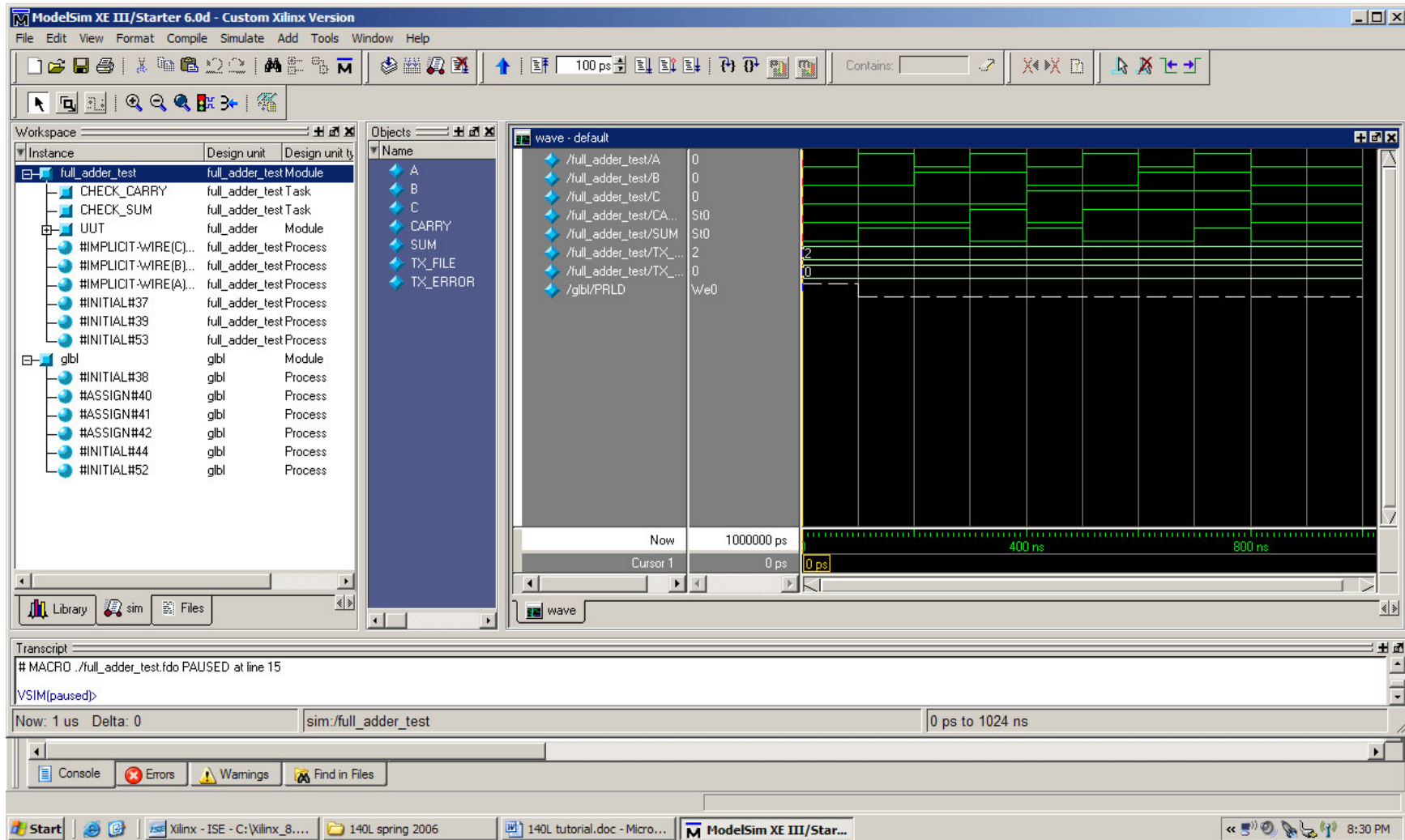
A window of all inputs and outputs are displayed. Go ahead and click on the light-green area of the timing chart to toggle the value. Toggle the A, B, and C so that it counts from 000 to 001 to 010 to 011, all the way to 111 and back to 000 as shown above. Once you have done this, you are ready to run the simulation. Save your simulation (Ctrl-s) and save often.



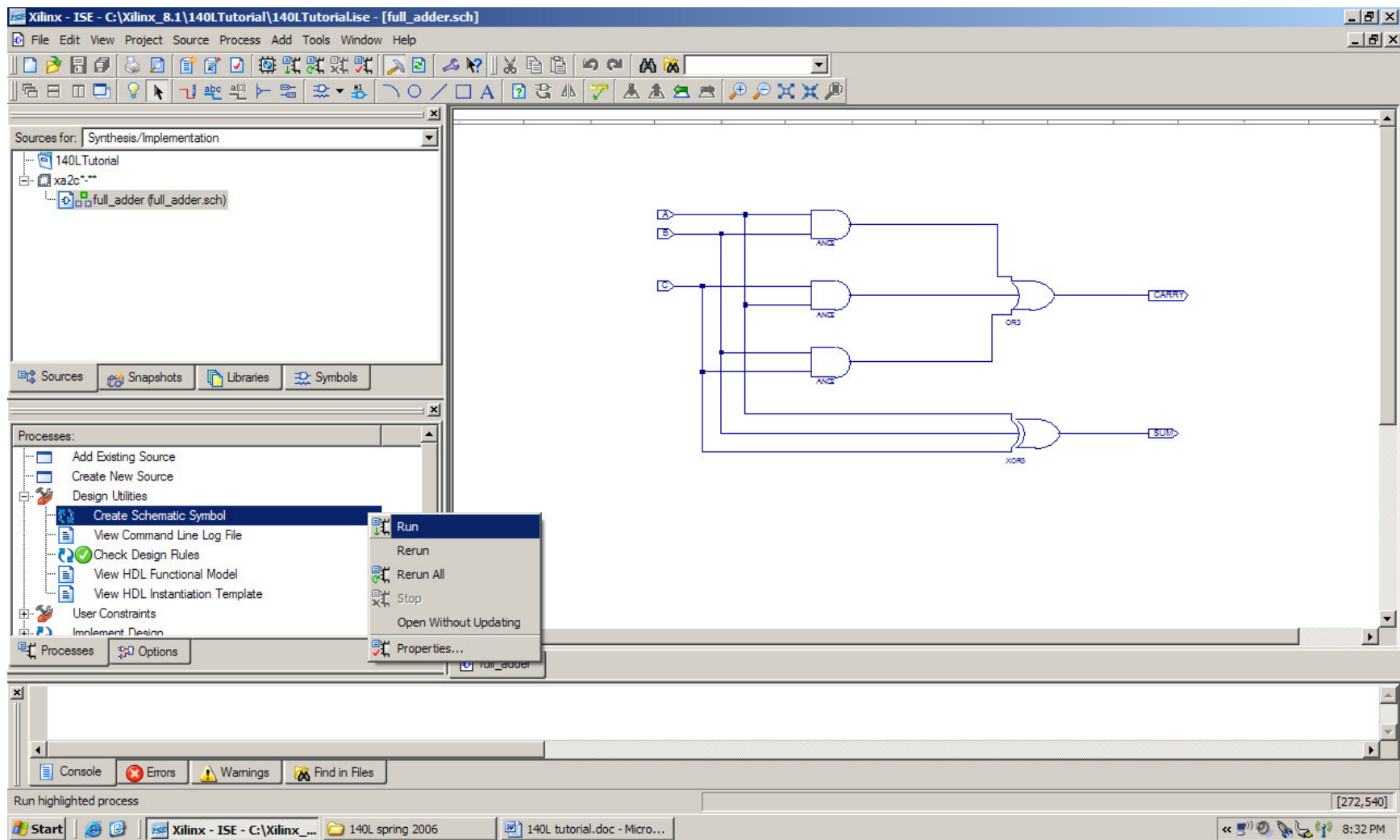
On the upper left window, make sure the “Behavioral Simulation” is selected and bottom left window, the “Processes” tab is showing.



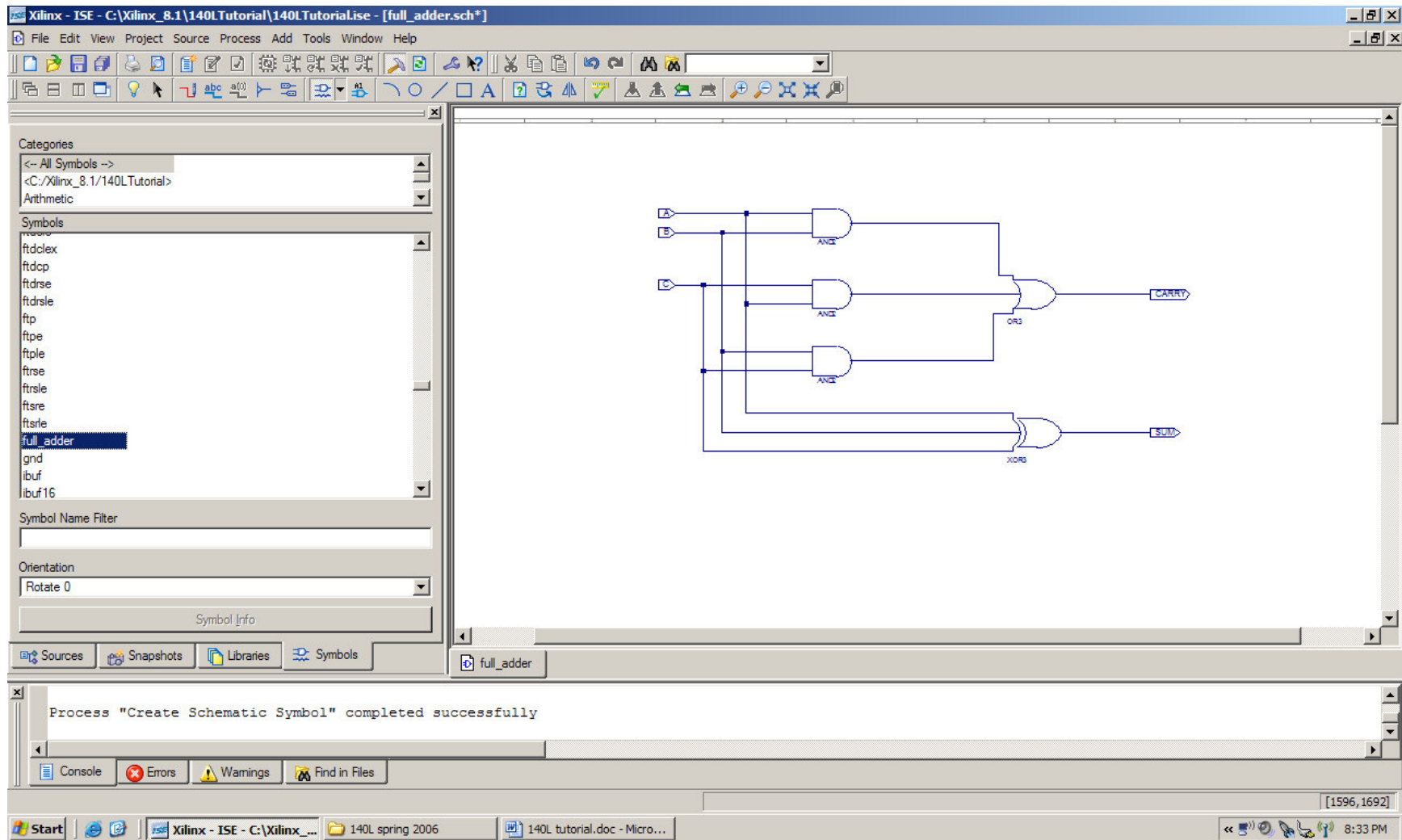
Right click on the Simulate Behavioral Model and select Run. The ModelSim window will open.



You did not see any error in the Transcript window (lower window) and see only green-color simulation in the timing chart window, your simulation is successfully ran. Try zoom-out and scroll all the way to the left in the timing chart window. You will see the above waveform. Congratulations, you now learn enough skill to do your first lab. The next two pages will show you how to create your own library (full_adder) so you can re-use them many times.



Make sure you select the “Synthesis/Implementation” drop down on the upper-left of the window. And select the “Create Schematic Symbol” under the “Processes” tab and click Run. This will create a new symbol in the symbol-list (see next page).



By expanding Symbols window, you now see the “full_adder” as one of the symbols in the list. You can now use this full_adder symbol to build larger circuits (4-bit adder for example).

By the way, there is a very subtle mistake in this tutorial. Notice that the above schematic shows XOR3 and previous screens showed before simulations showed XNOR3 (x-nor). I have made the quick correction once I realized the simulation result wasn't correct. If your team have caught this earlier in the tutorial, kudos to you!