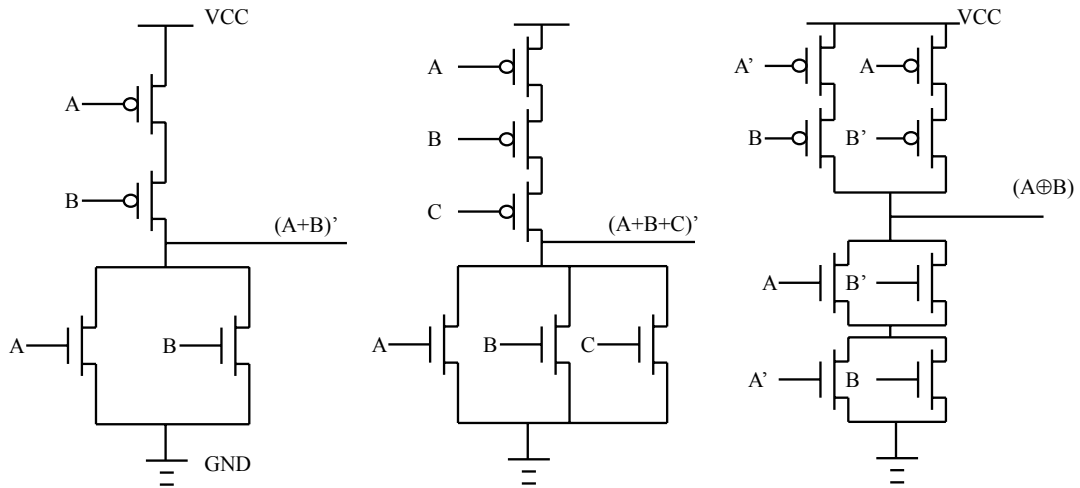


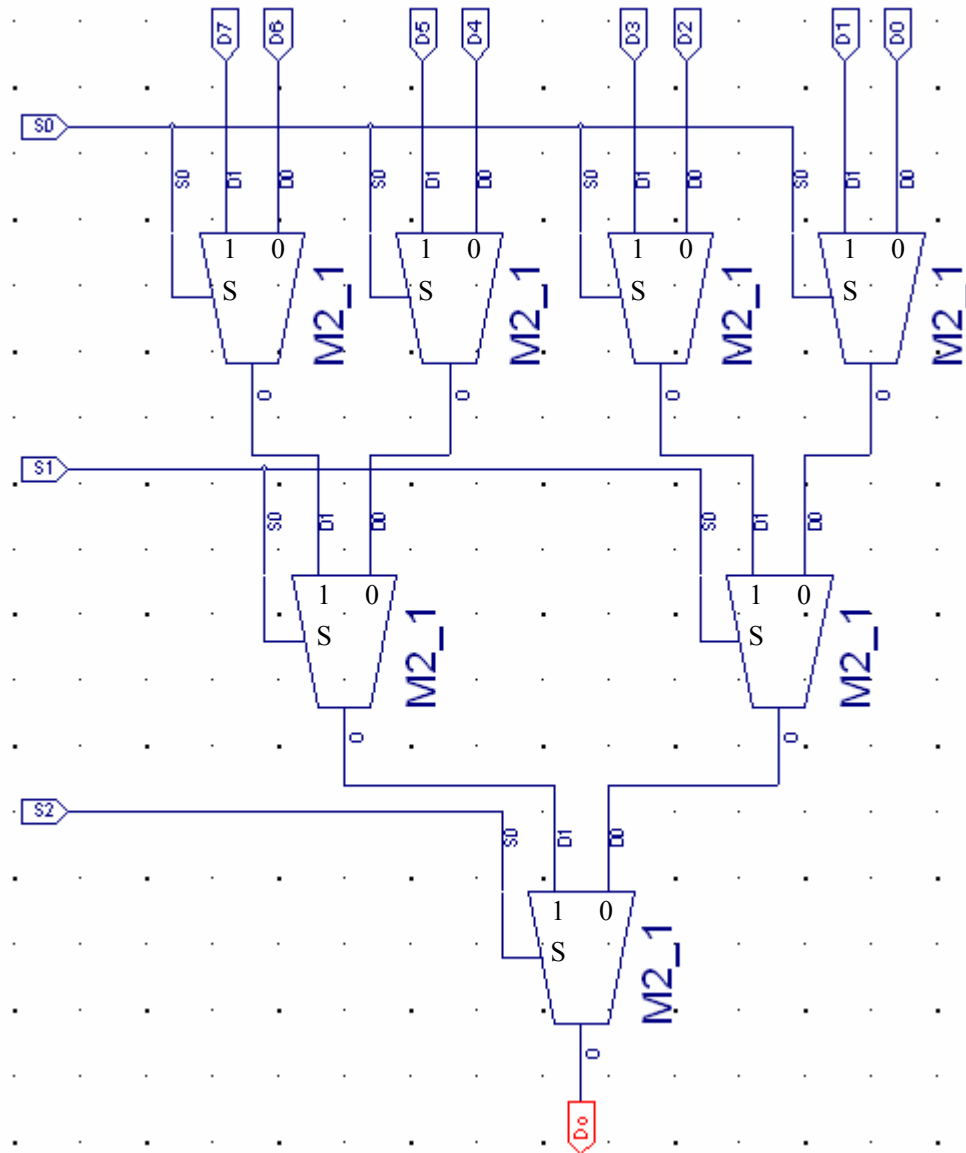
Solution

1. Use CMOS complementary logic to design a 2-input NOR gate, a 3-input NOR gate, a 2-input XOR gate. Draw the circuit.



2. Design an 8-input multiplexer with a tree of 2-input multiplexers.

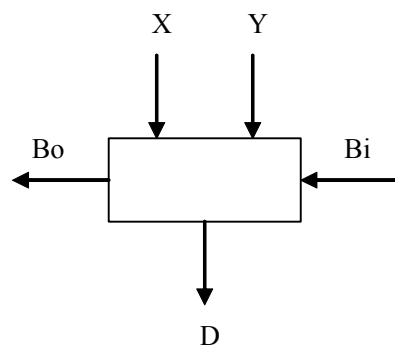
Draw the schematic diagram.



3. Design a Full-Subtractor with a minimal network of AND, OR, NOT gates.

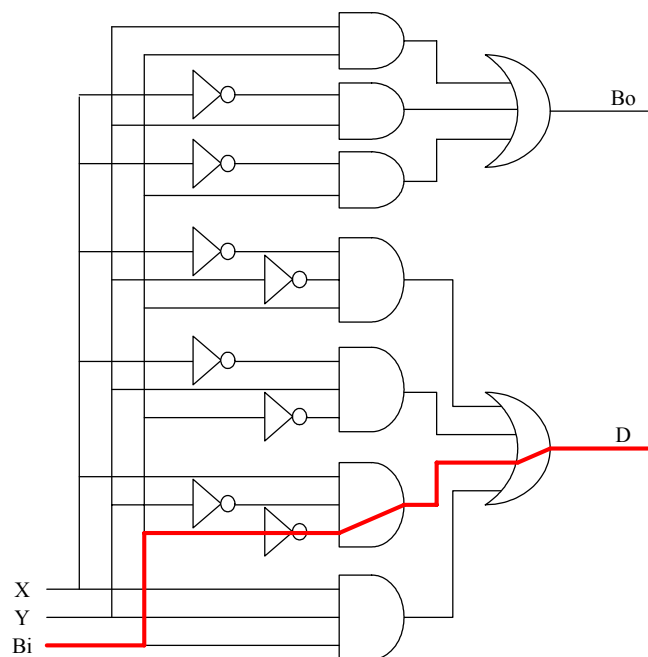
- a) Show the schematic diagram.
- b) Assume that each gate of the Full-Subtractor takes one unit delay.
 - i. What is the worst delay from inputs to outputs?
 - ii. Write and explain the input patterns that demonstrate the worst delay in timing analysis.

$X - Y - B_i$

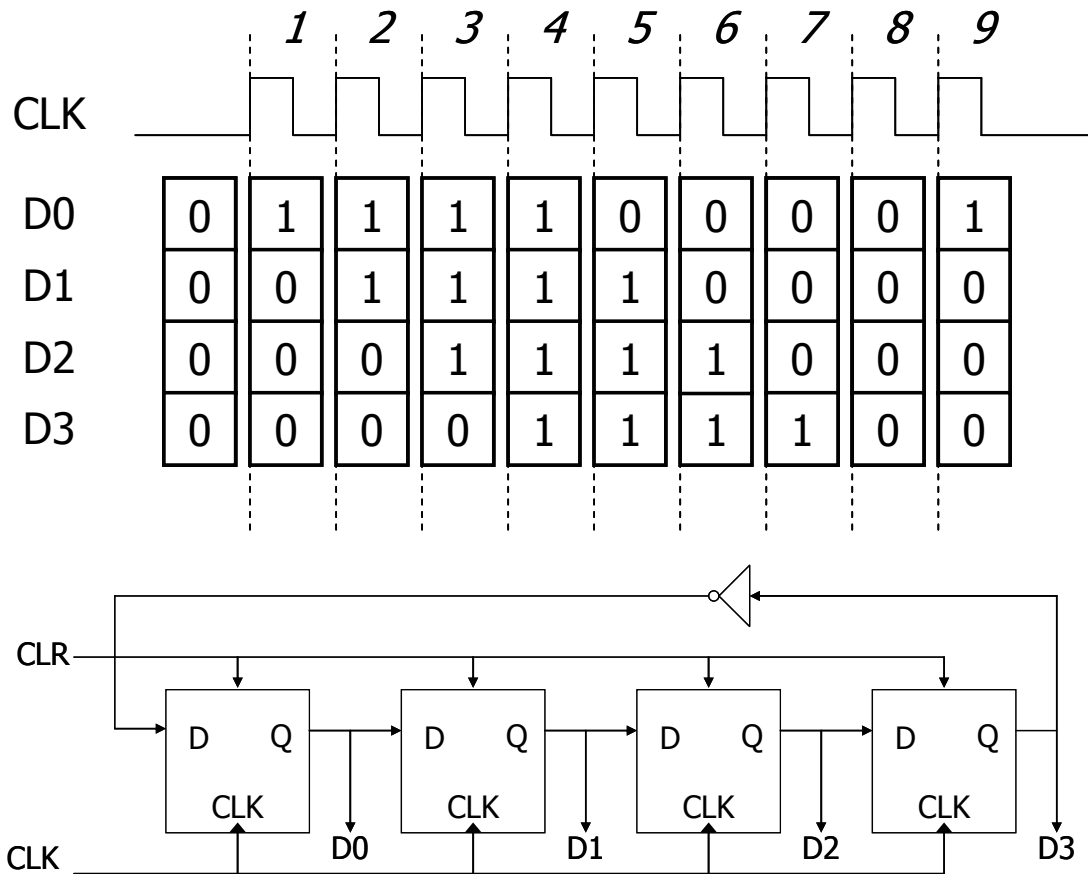


X	Y	B _i	D	B _o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

The worst delay is 3 units from B_i to D. To demonstrate the worst delay, X and Y can be set to '1' and '0' respectively. When B_i changes from '1' to '0', this switching will be propagated to D along the red path. And we can observe a '0' to '1' change at D output.



4. Design a 4-bit Johnson Counter with FDCE Flip-Flops. Draw the schematic diagram. Write the sequence of the counting cycle.



5. Given a Mealy machine described by the following state table.

Transform the Mealy machine to a Moore machine. Write the state table.

PS	x=a	x=b
A	C, 1	A, 0
B	D, 1	E, 1
C	A, 0	B, 0
D	B, 0	E, 0
E	A, 1	D, 1
	NS, z	

Only A and E have incoming edges with different output values, so A is split to A0 and A1, E is split to E0 and E1.

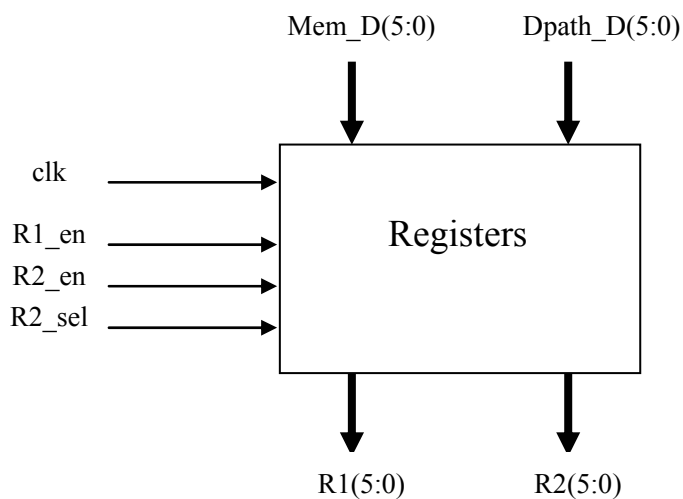
PS	x=a	x=b	Output
A0	C	A0	0
A1	C	A0	1
B	D	E1	0
C	A0	B	1
D	B	E0	1
E0	A1	D	0
E1	A1	D	1
	NS, z		

6. Assume a computer system has a simple instruction set described as follow:

Command	2-bit Instruction	6-bit Data	Description
Move1	00	$A_5A_4 \dots A_0$	Put $A_5A_4 \dots A_0$ value into register R1
Move2	01	$B_5B_4 \dots B_0$	Put $B_5B_4 \dots B_0$ value into register R2
Add	10	XXXXXX	Add contents in R1 and R2. Present the result at R2
Mask	11	XXXXXX	Mask (AND-ing) R1 and R2. Present the result in R2

The registers block has four 6-bit data ports and some control inputs.

The function of the registers block described as follow:



R1_en	R2_en	R2_sel	clk	Mem_D(5:0)	Dpath_D(5:0)	R1(5:0)	R2(5:0)
1	X	X	↑	M(5:0)	D(5:0)	M(5:0)	No Change
0	1	0	↑	M(5:0)	D(5:0)	No Change	M(5:0)
0	1	1	↑	M(5:0)	D(5:0)	No Change	D(5:0)
0	0	X	↑	M(5:0)	D(5:0)	No Change	No Change

Mem_D(5:0) is connected to a memory block which holds instructions. Dpath_D(5:0) is connected to the outputs of adder/mask. The output ports R1(5:0) and R2(5:0) are connected to the inputs of add and mask.

Please write the truth table of control logic, with instruction bits as inputs and R1_en, R1_en, R2_sel as outputs.

Assume that Inst(7) and Inst(6) are the most two significant bits in each instruction.

Inst(7)	Inst(6)	R1_en	R2_en	R2_sel
0	0	1	0	0
0	1	0	1	0
1	0	0	1	1
1	1	0	1	1