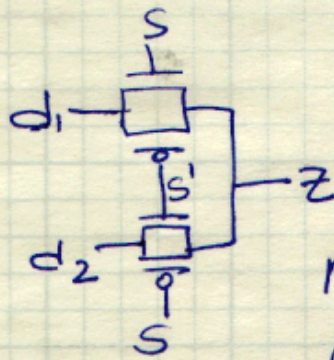
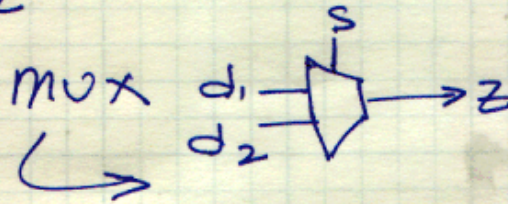


②

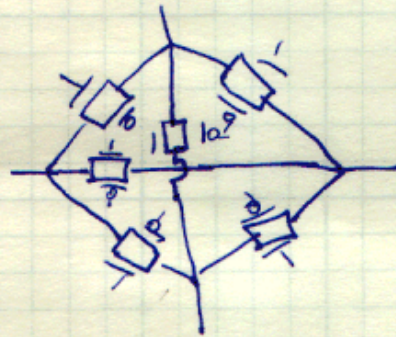


$$S=1 \Rightarrow Z=d_1$$

$$S=0 \Rightarrow Z=d_2$$



Reconfigurable Interconnect



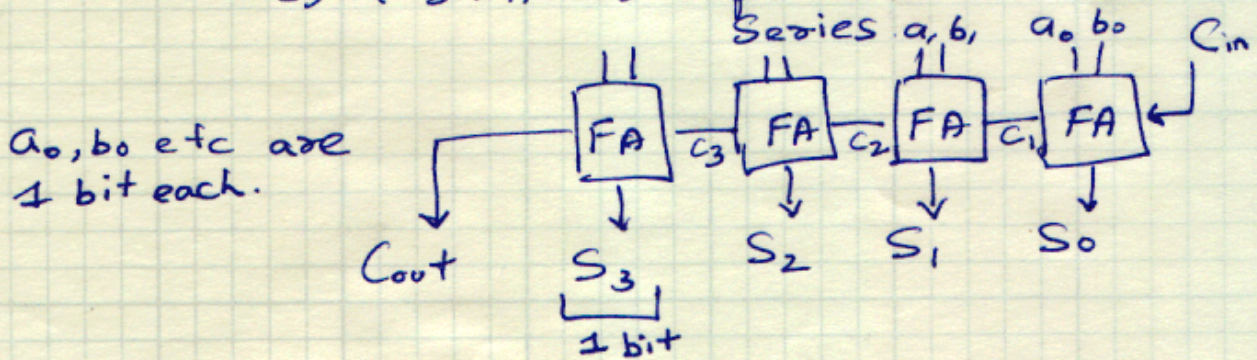
Lab - 1

Adder

a) Full Adder : $a + b + C_{in} = 2C_{out} + S$

↑ ↑ ↑
inputs

b) 4 bit Adder : put 4 F. Adders in Series



longest delay = $C_{in} \rightarrow C_1 \rightarrow C_2 \rightarrow C_3 \rightarrow C_{out}$

Function (no delay) Simulation : verify functionality

Post layout (delay) : verify clock cycles