

CSE 140L Hardware Lab Four, Spring 2002

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System Design using Datapath and Control Subsystems

Due date: June 3, 2002

Objective

In this lab, we will build a simple system using datapath and control subsystems. We use buses and standard modules as basic building blocks for the design. For this project, we use FPGA Family:XC4000E, Part: 4003EPC84 and Speed: 1.

The Project

Design a simple system that can perform addition, shift, comparison, and masking. The system reads a 7-bit value as input (3-bit instruction set & 4-bit data). There are three 4-bit registers R1, R2, and R3. Registers R1 and R2 store the data. Register R3 presents the result of the calculations. There is also a 1-bit flag for overflow and comparison.

We list the specification of the instructions.

- 1 Init: 000 XXXX - Initialize all registers, i.e. $R1=R2=R3=(0,0,0,0)$.
- 2 Move1: 001 aaaa - Put aaaa value into register R1.
- 3 Move2: 010 bbbb - Put bbbb value into register R2.
- 4 Store: 011 XXXX - Take the previous result in R3 & store into register R2.
- 5 Add: 100 XXXX - Add contents in R1 and R2. Present the result at R3 and output overflow flag.
- 6 Shift: 101 aaXX - Take the content in R2. Do left shift by aa bits and store the result in R3.
- 7 Comp: 110 XXXX - Compare the contents of R1 and R2. The flag bit is true if R1 is greater or equal to R2. Otherwise, it is false.
- 8 Mask: 111 XXXX - Mask (AND-ing) R1 and R2. Present the result in R3.

Note that register R1 holds its content except for instructions 1, 2. Register R2 holds except for instructions 1, 3, 4. Register R3 holds except for instructions 1, 5, 6, 8.

Report

Title page:

Names of students and due date.

Title of the lab and objective.

A brief description of each person's contribution.

Content:

- 1: Schematic diagram of the design.
2. ABEL code of the control subsystem.
3. Layout of the design.
4. Functional simulation of instructions. Demonstrate the content of the input and output of each operation. Use two different patterns for each instruction.
5. A discussion of the verification. Show the reason why we are confident that the system can function properly. Or list the processes needed for the proof. Use less than 30 words.
6. A discussion of the performance. Predict the clock frequency range of the system. Illustrate the worst delay path with timing simulation.

Grading

90% will be based on the completeness and correctness of the report. 10% will be based on the neatness, organization, and following instruction of the report format.