

CSE 243 (Section Id: 402517)
VLSI Computer-Aided Design
Synthesis Methodologies in VLSI Design & Test

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Course Contents

Synthesis Fundamentals Levels of Abstraction. Synthesis Definition. Languages. Essential Issues in Synthesis.

Circuits and Models Microelectronics. Semiconductor Technologies. Microelectronic Design Styles. Computer-Aided Synthesis and Optimization. Physical Design. Simulation. Verification. Test.

Architectural Models Design Styles. Combinatorial Logic. Finite State Machine with a Data-path. System Architecture.

Architectural Synthesis Design Representation. Behavioral Transformations. Partitioning. Time-Constrained Scheduling. Resource-Constrained Scheduling. Scheduling Pipelined Circuits. Allocation Tasks. Functional Unit Binding. Storage Unit Binding. Interconnection Binding. Decomposition Approaches.

Logic-Level Synthesis Two-level Combinational Logic Optimization. Logic Optimization Principles. Exact Logic Minimization. Heuristic Logic Minimization. Symbolic Minimization and Encoding Problems. Sequential Logic Optimization. State Minimization. State Encoding. State Extraction.

Hardware/Software Codesign Models. Architectures. System Partitioning. Specification Refinement. Cosimulation.

Test Fault Modeling. Fault Detection and Redundancy. Fault Equivalence and Fault Location. Fault Dominance. Single Stuck-Fault Model. Multiple Stuck-Fault Model. Automatic Test Generation for Single Stuck-Faults in Combinational Circuits. Automatic Test Generation for Single Stuck-Faults in Sequential Circuits. Functional Testing. Logic Level Diagnosis. Self-Checking Designs.