CSE 141 Summer 2020 Assignment 2

PID: _____ Name:_____

1. The following table lists the time spent in each module of a processor:

Module	Instruction Fetch	Instruction Decode	Execution	Data memory	Write back
Delay	350 ps	300 ps	250 ps	450 ps	200 ps

Please answer the following questions:

A. If the processor uses a single-cycle design and supports MIPS ISA, what's the cycle time of the processor?

B. Assume adding a pipeline register would incur 50 ps overhead, what's the cycle time of a "5-stage pipeline processor" by using each of the above module as a pipeline stage?

2. Consider the following MIPS instruction sequence:

```
LOOP: lw   $t0, 0($a0)
      lw   $a0, 0($t0)
      addi $a1, $a1, -1
      bne  $a1, $zero, LOOP
      add  $v0, $a0, $zero
      addi $sp, $sp, 8
```

   A. Assume the value in `$a1` was 2 before executing this code sequence. Please list the dynamic instructions that will be executed.

B. Assume the value in `$a1` was 2 before executing this code sequence. Also assume that you have a 5-stage MIPS pipeline processor that stalls for every hazard with a revised register file that accepts writes in the first half of a cycle and reads in the second half of a cycle. Please draw the pipeline diagram until the program reaches "`addi $sp, $sp, 8`".

C. Assume the value in `$a1` was 2 before executing this code sequence. Now, assume that you have a 5-stage MIPS pipeline processor that supports full data forwarding and always predict not-taken. The processor also uses a revised register file that accepts writes in the first half of a cycle and reads in the second half of a cycle. Please draw the pipeline diagram until the program reaches "`addi $sp, $sp, 8`". When you draw the pipeline diagram, you also need to include those instructions that were flushed.

D. With the processor in B, but assume the value in `$a1` was 10000 before executing this code sequence. How many cycles it takes for the program to reach "`addi $sp, $sp, 8`"? What's the average CPI?

E. Again, assume the value in `$a1` was 2 before executing this code sequence. Now, assume that you have a "7-stage MIPS pipeline processor" – which take 2 stages in both fetching instructions and data accesses. Therefore, the resulting pipeline processor will have the following stages – IF1, IF2, ID, EX, MEM1, MEM2, and WB. If the processor supports full data forwarding and always predict not-taken. The processor also uses a revised register file that accepts writes in the first half of a cycle and reads in the second half of a cycle. Please draw the pipeline diagram until the program reaches "`addi $sp, $sp, 8`". When you draw the pipeline diagram, you also need to include those instructions that were flushed.

F. With the processor in E, but assume the value in `$a1` was 10000 before executing this code sequence. How many cycles it takes for the program to reach "`addi $sp, $sp, 8`"? What's the average CPI?

3. Consider the following dynamic MIPS instructions:

```
1:  lw    $t0, 0($a0)
2:  add   $t0, $t0, $t0
3:  sw    $t0, 0($a0)
4:  addi  $a0, $a0, 4
5:  bne   $a0, $a1, LOOP
6:  lw    $t0, 0($a0)
7:  add   $t0, $t0, $t0
8:  sw    $t0, 0($a0)
9:  addi  $a0, $a0, 4
10: bne   $a0, $a1, LOOP
```

   A. Please identify the data dependencies in these instructions. You may list these data dependencies using the format like:
   Inst. 2 depends on Inst. 1 for $t1

   B. Please list the data dependencies that leads to data hazards in a 5-stage MIPS pipelined processor supporting full forwarding