CSE248: ALGORITHMIC AND OPTIMIZATION FOUNDATIONS FOR VLSI CAD

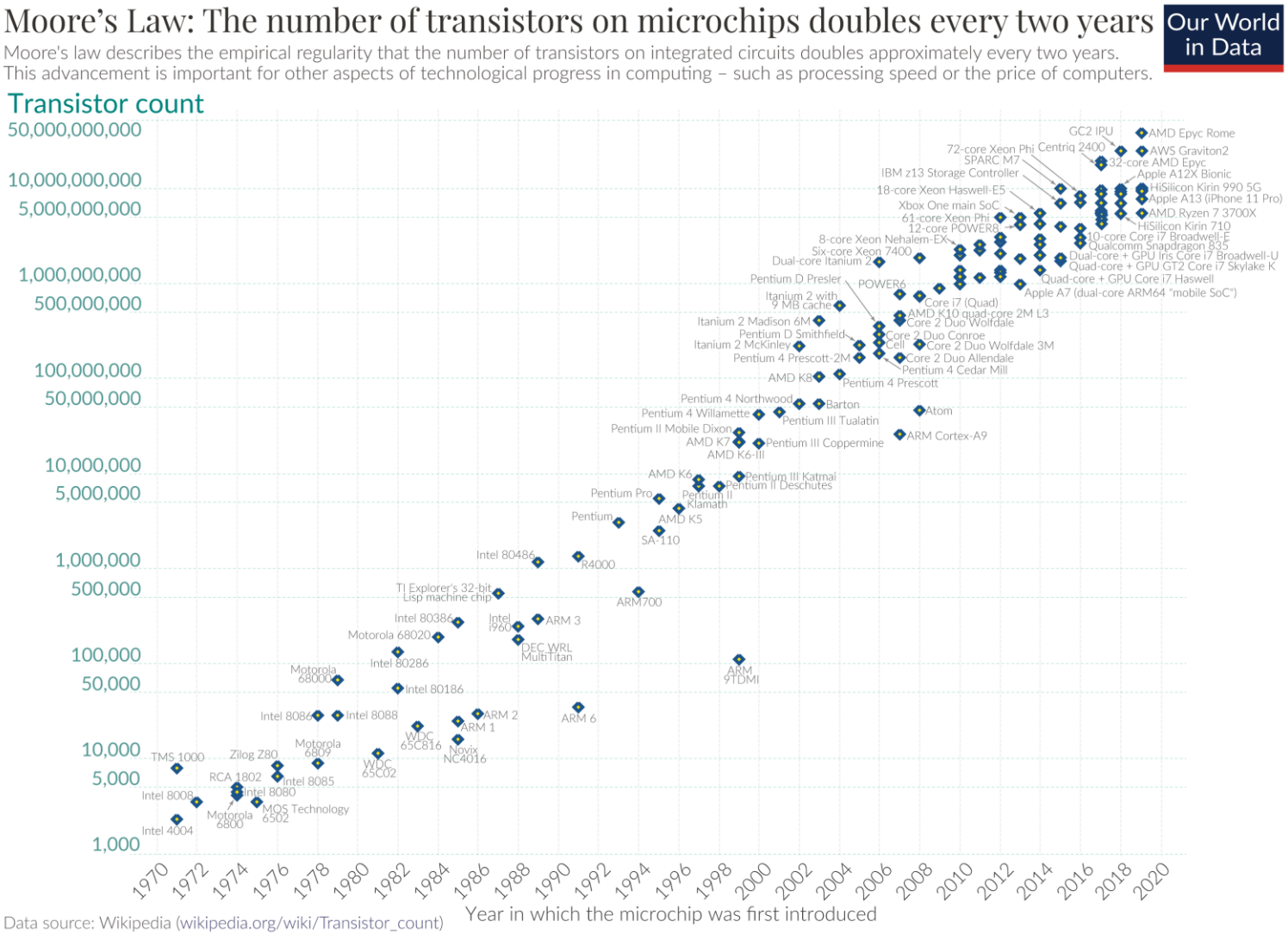
Lecture 2: Moore's Law

Fall 2023

Chung-Kuan Cheng

Moore's Law

Moore's law is the observation that the number of transistors in an integrated circuit (IC) doubles about every two years. (Wikipedia)



Moore's Law: Market

The market is the key to the growth due to heavy investment costs: equipment, non-recurring engineering (NRE) expenses.

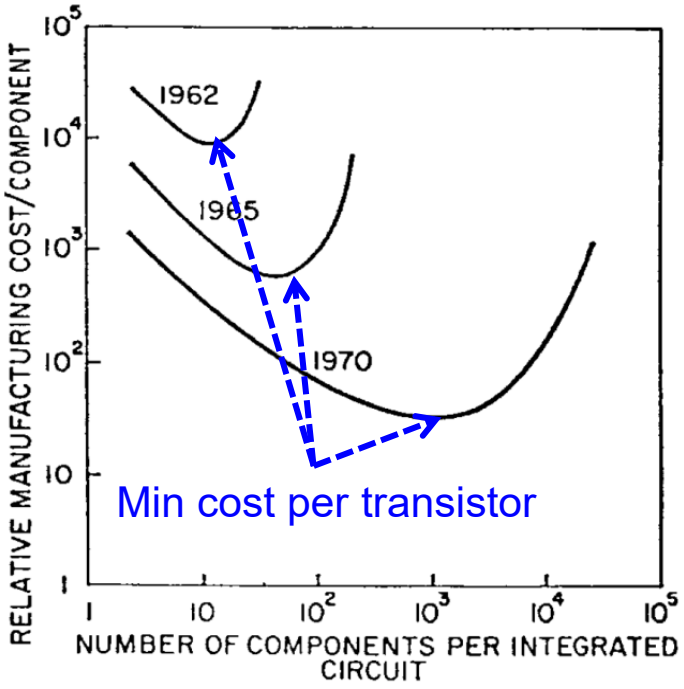
Investment: Product: Market

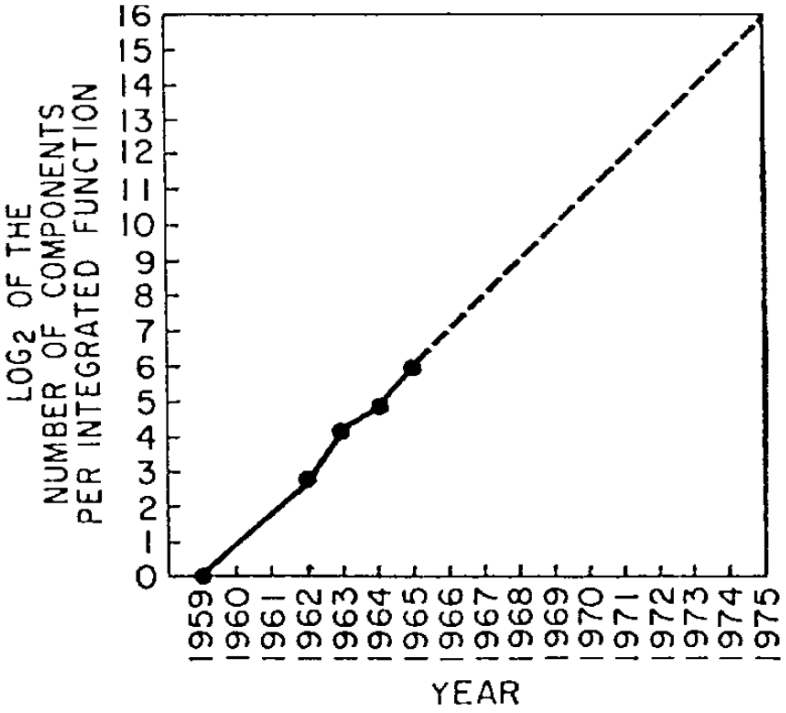
Annual semiconductor sales (1987–2018)

Year	Revenue (nominal)	Revenue (inflation)	Ref
2022	$601,694,000,000		[13]
2021	$594,952,000,000		[13]
2020	$466,237,000,000		[14]
2019	$422,237,000,000		[14]
2018	$481,090,000,000	$560,660,000,000	[1]
2017	$420,390,000,000	$501,890,000,000	[1]
2016	$345,850,000,000	$421,710,000,000	[1]
2015	$335,170,000,000	$413,800,000,000	[15]
2014	$335,840,000,000	$415,150,000,000	[15]
2013	$305,580,000,000	$383,900,000,000	[15]
2012	$291,560,000,000	$371,640,000,000	[15]
2011	$299,520,000,000	$389,640,000,000	[15]
2010	$298,320,000,000	$400,340,000,000	[15]
2009	$226,310,000,000	$308,700,000,000	[15]
2008	$280,000,000,000	$381,000,000,000	
2007	$255,600,000,000	$360,700,000,000	[16]
2006	$247,700,000,000	$359,600,000,000	[16]
2005	$227,000,000,000	$340,000,000,000	[15]
2004	$213,000,000,000	$330,000,000,000	[15]
2000	$204,000,000,000	$347,000,000,000	[15]
1995	$144,000,000,000	$277,000,000,000	[15]
1992	$60,000,000,000	$125,000,000,000	[15]
1990	$51,000,000,000	$114,000,000,000	[15]
1987	$33,000,000,000	$85,000,000,000	[15]

Source:Wikipedia

"Moore's Law" = Scaling of Cost and Value





- **Scaling focus: "PPAC" Power, Performance, Area, Cost**
- **Moore's Law is a law of cost reduction 1% = 1 week**

A. B. Kahng, *Ho-Am Prize Presentation*, 2019.

Moore's Law: Innovation

- Device: Bipolar, NMOS, CMOS, ReRAM,… Qbit
- Interconnect: Al, Cu, Ta, Ro, CNT
- Insulator: High K
- Gate: FinFET, nanosheet, CFET, VFET, monolithic 3D IC
- Fabrication: DUV193nm, EUV13.5nm, NIL, DAS
- Design Automation: EDA, DTCO, STCO

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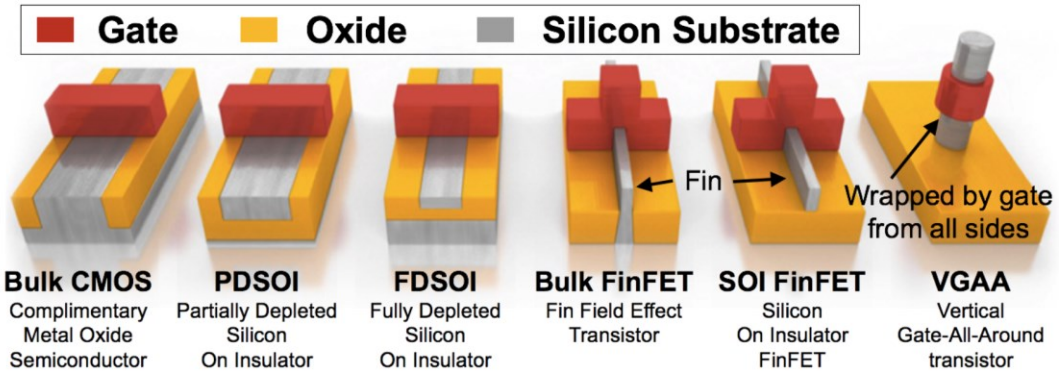
New Opportunities

Year of Production	2015	2017	2019	2021	2024	2027	2030
Technology Node (nm)	16/14	11/10	8/7	6/5	4/3	3/2.5	2/1.5
Transistor Structure							
Fully Depleted SOI (FDSOI)							
FinFET							
Lateral Gate-All-Around (LGAA)							
Vertical Gate-All-Around (VGAA)							
Monolithic 3D							

ITRS 2015 report

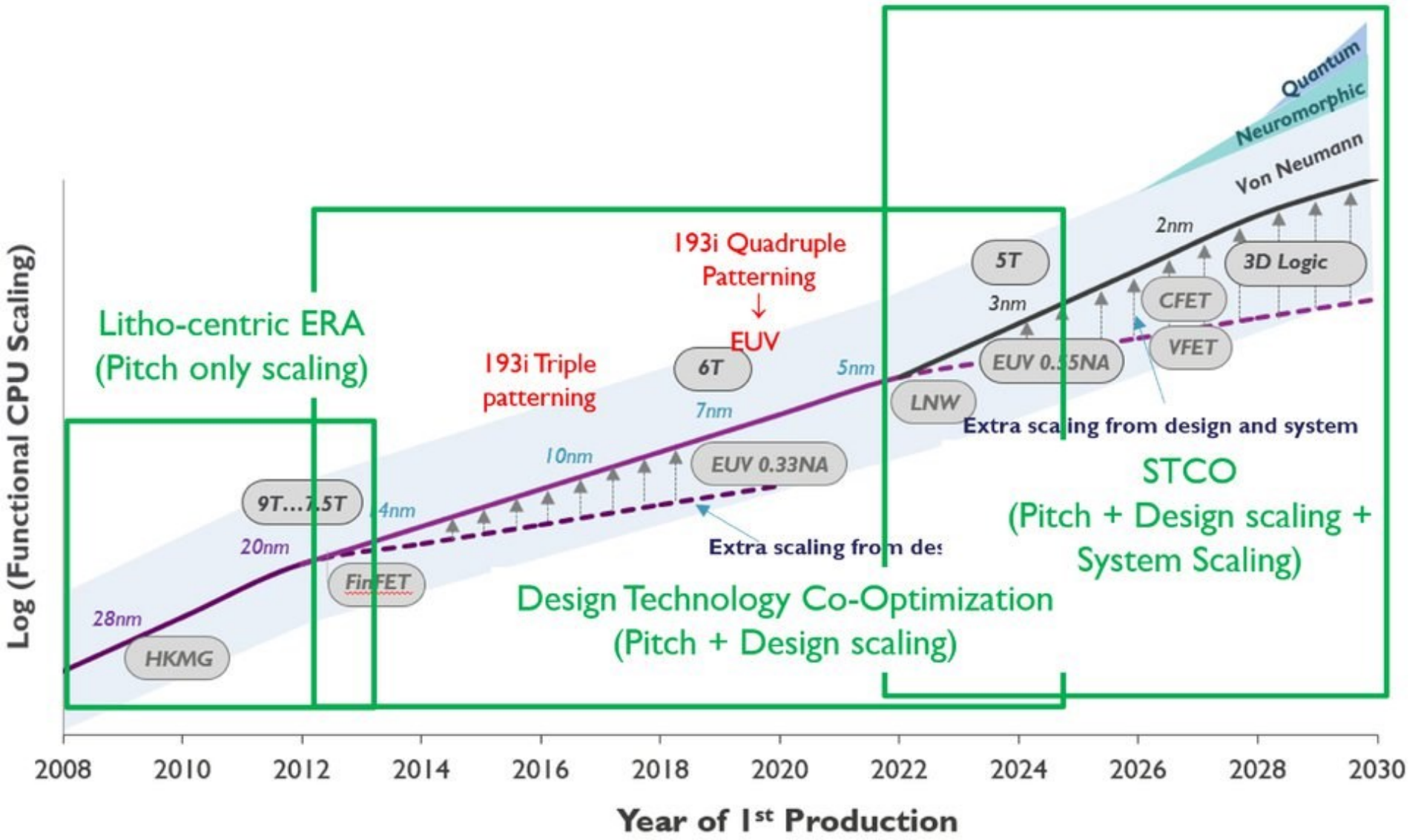


ASML report

We must prepare the future design methodology !!

ITRS Report 2015 Edition, http://www.semiconductors.org/main/2015_international_technology_roadmap_for_semiconductors_itrs/.
Many Ways to Shrink: The Right Moves to 10 Nanometer and Beyond, https://staticwww.asml.com/doclib/investor/asml_3_Investor_Day-Many_ways_to_shrink_MvdBrink1.pdf.

Now, In Deep Nanometer Technologies



[S. M. Y. Sherazi et al., "Standard-cell design architecture options below 5nm node: The ultimate scaling of FinFET and Nanoshee," keynote, Proc. SPIE, 2019]

Subjects

1. Partitioning, Floorplanning (3D)
2. Placement (3D)
3. Routing (3D)
4. Standard Cell Synthesis
5. Devices: Memtransistor