CSE248: ALGORITHMIC AND OPTIMIZATION FOUNDATIONS FOR VLSI CAD

Lecture 1: Introduction

Fall 2023

Chung-Kuan Cheng

Overall Outlines of Class

- CK Cheng, CSE 2130, tel. 858 534-6184, ckcheng+248@ucsd.edu
- Lectures: 3:30 ~ 4:50pm TTH CSE2154,
- Grading:
  - Homework: 40%
  - Project Outlines: 10%
  - Project Presentation: 25%
  - Final Report: 25%
- Goal:
  - Foundation of VLSI design automation
  - Research

Potential Project Topics

Tools at hand: GPU, Machine Learning, Deep Learning

- Partitioning
  - Min Cut with Retiming
  - Replication Cut with Retiming
- 2D/3D Floorplanning
  - Enumeration of 3D floorplans vs. number of blocks
  - 3D floorplanning
- 2D/3D Placement
  - Placement with partitioning
- Routing
  - Routing for 3D Layout
- Logic Synthesis
  - Logic synthesis using novel logic components

Motivation: IEEE IRDS Roadmap

- Moore's Law: A self-fulfilling prophecy driven by market and innovation.
- Geometric Scaling
- Design Technology Co-Optimization
- System Technology Co-Optimization
- More-than-Moore Exploration
- New Materials and Devices

References

1. IEEE IRDS Roadmap
2. Interconnect Analysis and Synthesis, Cheng, Lillis, Lin, and Chang, John Wiley & Sons, 2000.
3. Electronic Design Automation: Synthesis, Verficiation, and Test, Wang, Chang, and Cheng, Morgan Kaufmann, 2009
4. VLSI Physical Design: From Graph Partitioning to Timing Closure, Kahng, Lienig, Markov, and Hu, Springer, 2022.
5. Conference and Journal Papers