Net Separation-Oriented Printed Circuit Board Placement via Margin Maximization

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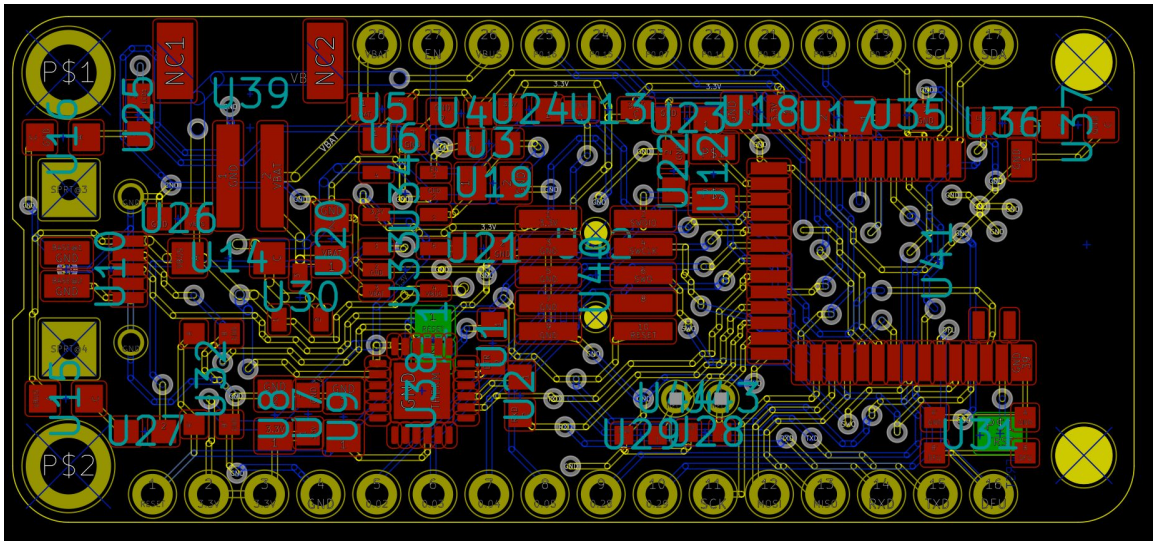
Overview

- Printed Circuit Board Placement
- NS-Place: motivation, construction, formulation
- Experiments
- Conclusion

Printed Circuit Board (PCB) Placement

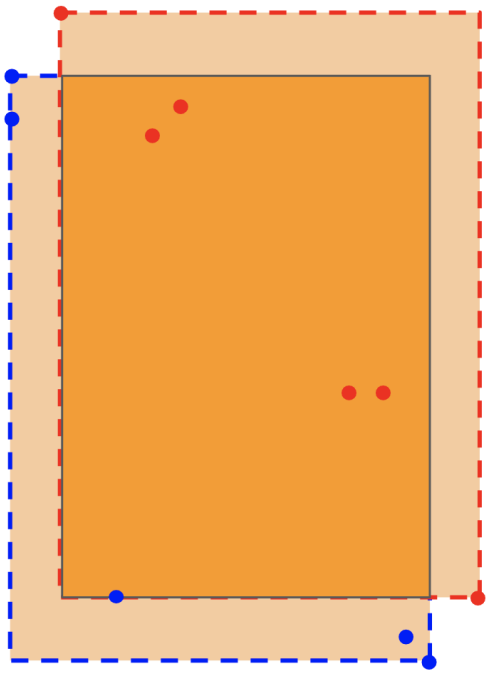


- Printed circuit board (PCB) placement as a benchmark for the packaging problem.
  - Multiple placement and routing layers
  - Arbitrary component sizes, shapes, and rotations
  - High utilization

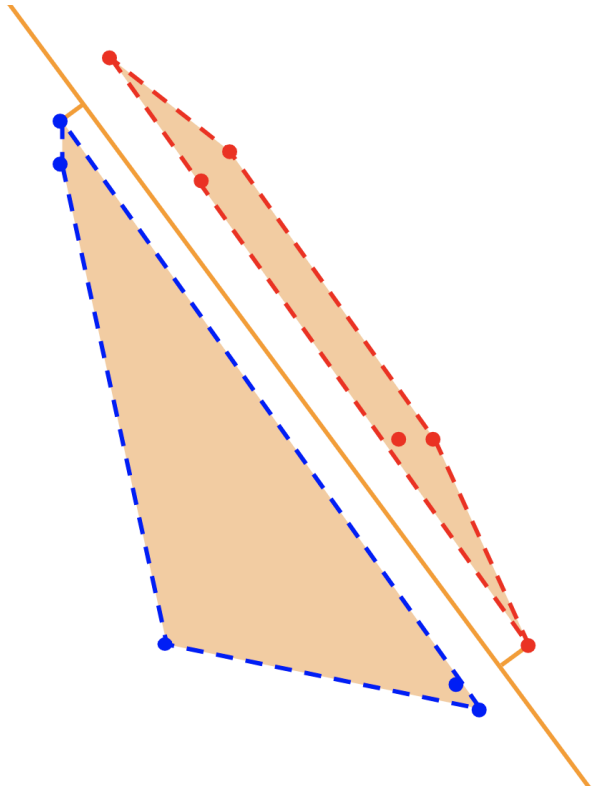
Contributions

- Existing methods for congestion are *pessimistic*.
- We propose NS-Place for PCB layout: minimizes net congestion using SVMs and an *optimistic* congestion model.
- Formulates legalization as a congestion-aware MILP
- Variable and constraint pruning via (relative position) constraint substitution

An Optimistic Model of Congestion

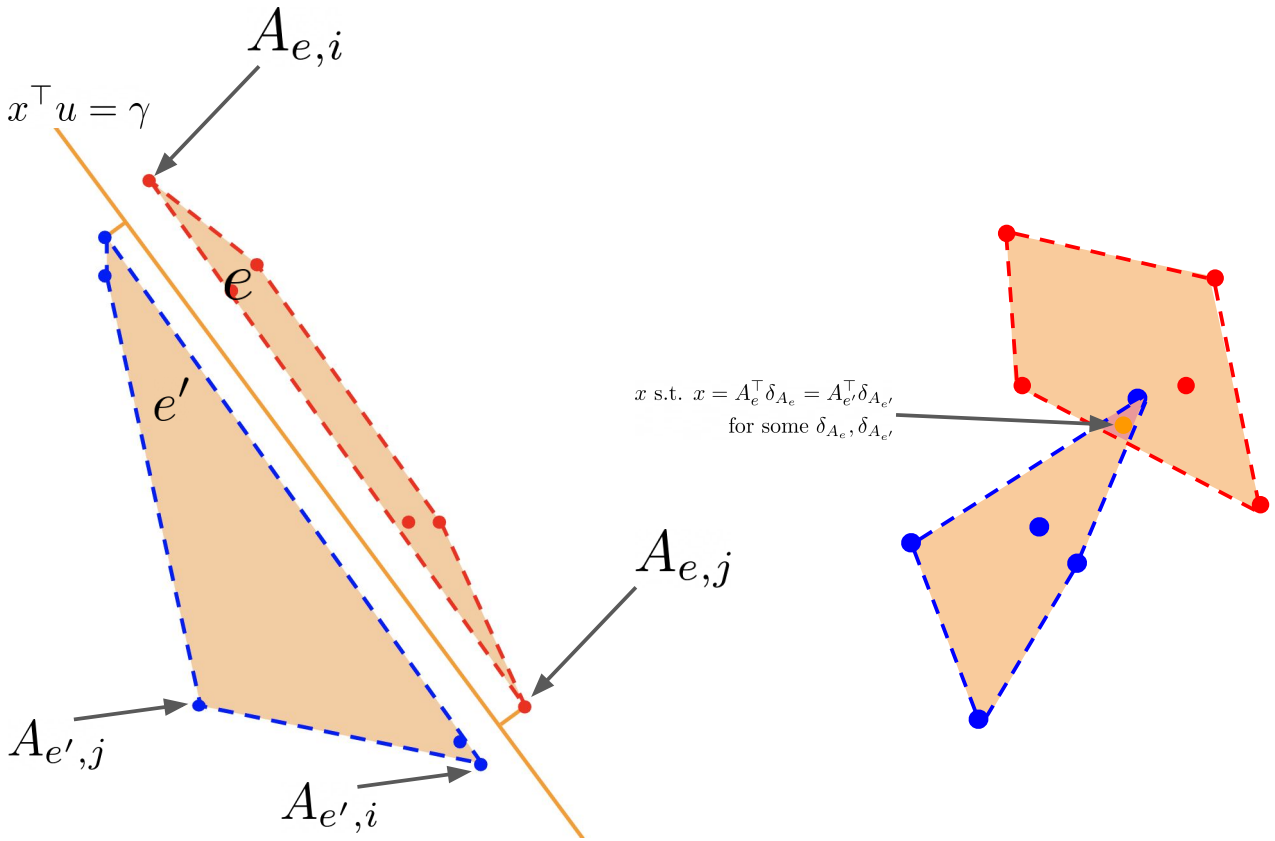


classic congestion modeling



our model

Convex Hull Construction



net	$e \in \mathcal{E}$
pin matrices	A_e
convex hull coefficients	u, γ

Formulation

$$\exists \delta_{A_e} \in \mathbb{R}^k, \delta_{A_{e'}} \in \mathbb{R}^{k'}$$
$$\text{such that } A_e^T \delta_{A_e} = A_{e'}^T \delta_{A_{e'}} \quad \mathbf{1}^T \delta_{A_e}, \mathbf{1}^T \delta_{A_{e'}} = 1,$$
$$\delta_{A_e}, \delta_{A_{e'}} \geq 0$$

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Duality & Farkas' Lemma: conditions must be satisfied if the convex hulls *do not* intersect ((5) has *no* solution):

$$A_e u \geq \alpha \mathbf{1} \quad A_{e'} u \leq \beta \mathbf{1} \quad \alpha - \beta > 0$$
$$\implies A_e u - \gamma \mathbf{1} \geq \mathbf{1}, \quad A_{e'} u - \gamma \mathbf{1} \leq -\mathbf{1}$$

Minimizing Congestion

$$
\begin{aligned}
0 &= \min_{u,\gamma} f(e, e', u, \gamma) \\
&= \min_{u,\gamma} ||(-A_e u + (\gamma + 1)\mathbf{1})_+||_2 + \\
&\qquad ||(A_{e'} u - (\gamma - 1)\mathbf{1})_+||_2
\end{aligned}
$$

Let A_e be the pin matrix corresponding to net e. We define the net-separation regularizer (over all nets) to be

$$\boxed{Ns(\cdot) = \frac{1}{|\mathcal{M}|} \sum_{e' \in \mathcal{E}} \min_{u,\gamma} f(e, e', u, \gamma)}$$

Minimizing Congestion

Our framework implies a *Bi-level* optimization problem for placement:

$$\min_{x,y} \sum_{e \in \mathcal{E}} [Wa(e; x, y) + \lambda_{\mathrm{NS}} Ns(e; x, y)] + \lambda_{\mathrm{D}} D(x, y)$$

Generally NP-Hard (especially since D is non-convex).

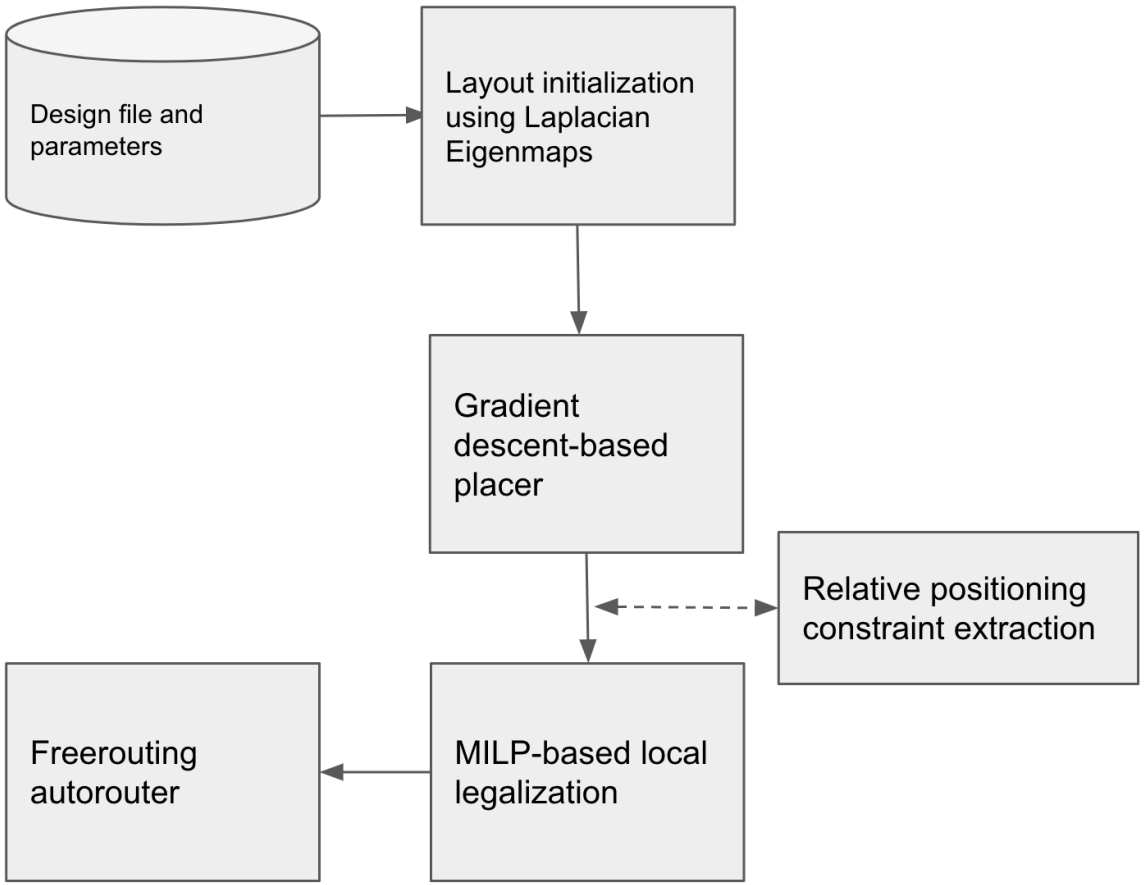
Minimizing Congestion

We can reach a local solution:

1. We can solve for μ, γ using off-the-shelf SVM solvers.

2. Update x, y with gradient descent

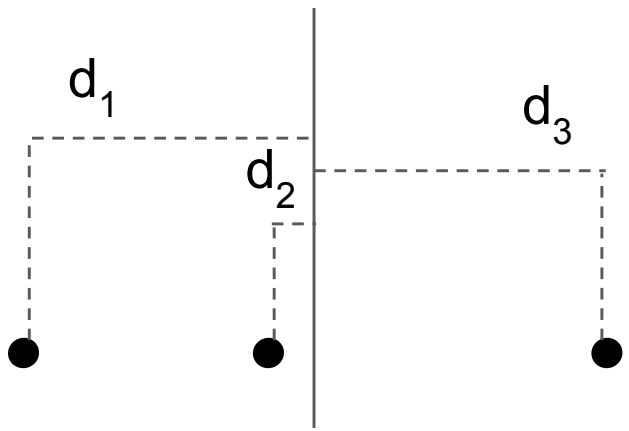
Placement Flow



Flow: Initialization

$$\begin{aligned} \min\ & x^T L x + y^T L y \\ \text{s.t.}\ & v^T x = 0, \quad v^T y = 0, \quad x, y \neq 0 \\ & x^T D x = c_1, \quad y^T D y = c_2, \quad x^T D y = c_3 \end{aligned}$$

1. Objective: minimize the squared wire length
2. Linear constraints: concentrate the layout about the origin and prevent the trivial solution
3. Quadratic constraints: spread the placement over the axes.



1-d example of constraints.

Flow: Legalizataion

$$\min_{x,y,r} \left[\sum_{i \in |\mathcal{E}|} \mathrm{hpwl}(i) + \left[\max_{i \in |\mathcal{E}|} \mathrm{hpwl}(i) - \min_{i \in |\mathcal{E}|} \mathrm{hpwl}(i) \right] \right]$$

$$\mathrm{hpwl}_x(i) = (U_x^{(i)} - L_x^{(i)})$$

Flow: Legalizataion

$$\min_{x,y,r} \left[\sum_{i \in |\mathcal{E}|} \text{hpwl}(i) + \left[\max_{i \in |\mathcal{E}|} \text{hpwl}(i) - \min_{i \in |\mathcal{E}|} \text{hpwl}(i) \right] \right]$$

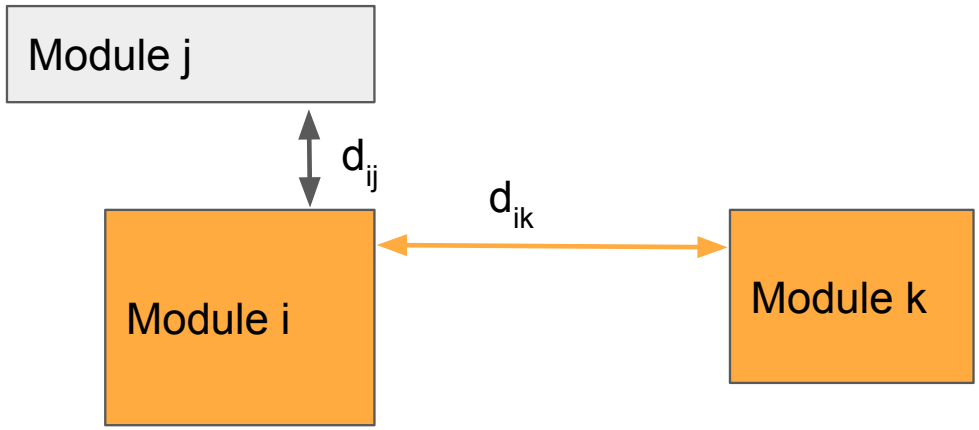
$$\text{hpwl}_x(i) = (U_x^{(i)} - L_x^{(i)})$$

where the *horizontal* HPWL and relative position constraints are given by

$$U_x^{(i)} \geq p_j^{(i)}(x), \quad L_x^{(i)} \leq p_j^{(i)}(x) \quad \forall j \in \mathcal{E}_i$$

$$\begin{aligned}
x_i + r_i h_i + (1 - r_i) w_i &\leq W && \text{width} \\
x_i + r_i h_i + (1 - r_i) w_i &\leq x_j + W(p_{ij} + q_{ij}) && \text{i-left-j} \\
x_i - r_j h_j - (1 - r_j) w_j &\geq x_j - W(1 - p_{ij} + q_{ij}) && \text{i-right-j} \\
x_i, y_i \geq 0, \quad r_i, q_{ij}, p_{ij} &\in \{0, 1\}
\end{aligned}$$

Relative Position Constraints



Add relative position constraint if $d_{ik} > d_{ij}$ and $d_{ik} > k$:

1. Prune variables p_{ik}, q_{ik}
2. Replace four constraints with a single constraint:

$$x_k - r_i h_i - (1 - r_i) w_i \geq x_i$$

PCB Benchmark Suite

design	$W \times H(mm^2)$	#comp	#locked.	util.	#nets	#pins
PCB1	21×14	8	1	0.59	15	40
PCB2	51×23	18	5	0.79	34	77
PCB3	55×28	34	2	0.44	38	138
PCB4	23×60	28	6	0.67	52	140
PCB5	41×22	48	2	0.40	54	163
PCB6	62×57	48	2	0.17	64	190
PCB7	51×23	46	2	0.55	69	211
PCB8	57×87	36	2	0.62	70	188
PCB9	44×36	58	2	0.60	80	229
PCB10	102×54	57	18	0.21	99	319
PCB11	89×58	64	2	0.10	134	401
PCB12	58×60	58	4	0.31	35	233
PCB13	86×72	61	4	0.51	63	314
PCB14	86×54	1570	947	0.64	386	1638

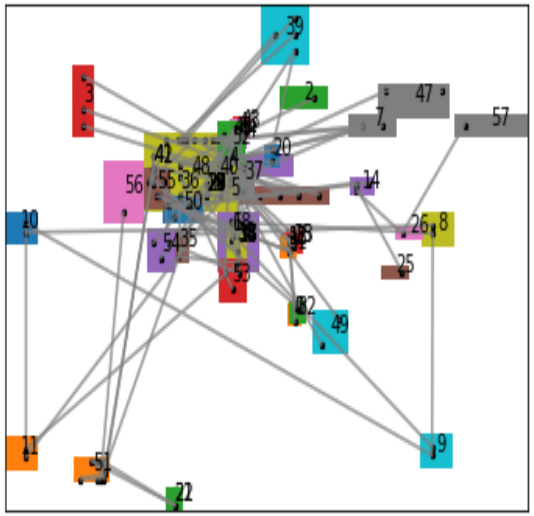
Quantitative Results

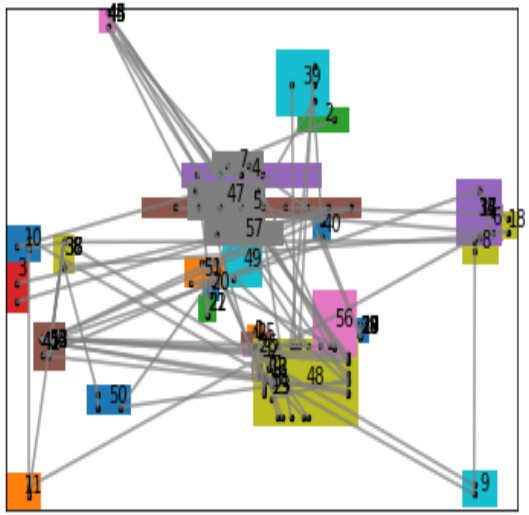
Design	HPWL (mm)				Net Separation Obj.				Runtime (s)		
	manual	MILP	GDMILP	NS-Place	manual	MILP	GDMILP	NS-Place	MILP	GDMILP	NS-Place
PCB1	110.22	**64.44 (41.50)**	68.90 (37.4)	72.10 (34.60)	192.13	192.11	192.11	**187.40**	2.70	4.90	5.10
PCB2	362.70	**291.10 (19.70)**	294.32 (18.80)	296.18 (18.30)	497.50	497.40	499.30	**493.10**	6.30	6.20	6.80
PCB3	312.60	**212.70 (32.0)**	252.40 (19.30)	271.30 (13.20)	1427.10	2124.30	1426.40	**1411.40**	14400.00	3793.00	3917.60
PCB4	603.30	-	536.48 (11.10)	**531.19 (12.00)**	3750.20	-	3753.10	**3746.13**	-	9.40	9.90
PCB5	654.10	-	**621.00 (5.10)**	637.00 (2.60)	2400.00	-	2400.00	**2300.00**	-	4231.20	4461.50
PCB6	771.80	-	**649.40 (15.90)**	708.60 (8.40)	1930.00	-	1940.00	**1740.00**	-	4893.10	5072.40
PCB7	2987.90	-	**563.10 (88.50)**	1601.40 (46.40)	1241.34	-	1239.70	**1017.16**	-	5927.30	6008.20
PCB8	766.10	**731.30 (4.60)**	748.40 (2.30)	756.40 (1.30)	98500.00	99500.00	99400.00	**96400.00**	14400.00	4360.90	4732.40
PCB9	714.90	-	677.60 (5.20)	**662.50 (7.30)**	2600.00	-	2600.00	**2400.00**	-	5327.30	5719.80
PCB10	4355.61	-	3317.94 (23.80)	**3315.46 (23.90)**	2117.80	-	2124.10	**2103.60**	-	5314.70	5417.20
PCB11	2941.90	-	**2573.20 (12.50)**	2618.10 (11.00)	9210.00	-	9210.00	**9070.00**	-	4651.90	4782.40
PCB12	972.50	929.30 (4.40)	**932.60 (4.10)**	941.30 (3.20)	10.73	11.31	11.47	**36.92**	14400.00	4619.10	4752.30
PCB13	2644.97	-	**2126.13 (19.60)**	2151.77 (18.60)	2400.00	-	2400.00	**2300.00**	-	3278.60	3416.30
PCB14	7069.26	-	**6432.19 (9.01)**	6691.34 (5.35)	29400	-	29870	**11186**	-	14400.00	14400.00

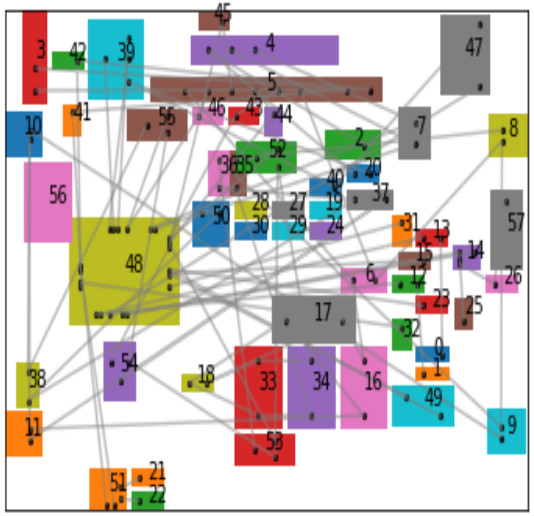
Quantitative Results

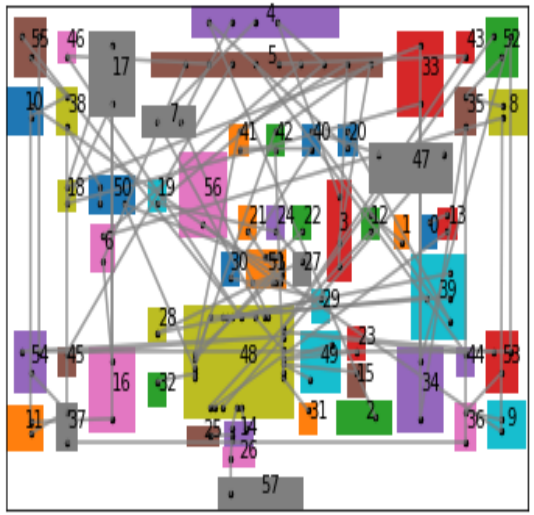
Design	Routed Wirelength (mm)				#Vias				#DRVs + #unrouted nets			
	manual	MILP	GDMILP	NS-Place	manual	MILP	GDMILP	NS-Place	manual	MILP	GDMILP	NS-Place
PCB1	129.00	123.00 (4.70)	194.00 (-50.4)	**121.00 (6.20)**	**0**	10	9	4	6	**0**	**0**	**0**
PCB2	**354.00**	632 (-78.50)	507.00 (-43.20)	421.00 (-18.90)	**3**	6	8	5	13	26	24	23
PCB3	638.00	682.00 (-6.90)	771.00 (-20.80)	**616.00 (3.40)**	17	21	24	**15**	11	2	3	**0**
PCB4	809.00	-	857.00 (-5.90)	**806.00 (0.40)**	**31**	-	59	54	17	-	4	**0**
PCB5	558.00	-	**538.00 (3.60)**	541.00 (3.00)	**32**	-	84	49	7	-	5	**3**
PCB6	1007.00	-	**854.00 (15.90)**	906.00 (10.00)	23	-	47	**19**	34	-	29	**0**
PCB7	3735.00	-	3140.00 (15.90)	**2949.00 (21.00)**	161	-	141	**93**	23	-	**0**	**0**
PCB8	913.00	854.30 (6.30)	713.40 (21.90)	**711.90 (22.00)**	57	73	89	**43**	27	6	5	**0**
PCB9	1069.00	-	**749.00 (29.90)**	772.00 (27.80)	**38**	-	87	64	17	-	7	**0**
PCB10	5043.00	-	5294.00 (-1.00)	**4914.00 (2.60)**	129	-	136	**97**	12	-	3	**0**
PCB11	3460.00	-	3271.90 (5.40)	**3107.80 (10.20)**	131	-	286	**109**	23	-	57	**13**
PCB12	1790.00	1960.00 (-9.40)	1930.00 (7.80)	**1720.00 (3.90)**	49	62	54	**45**	4	9	8	**0**
PCB13	3150.00	-	2903.00 (7.80)	**2897.00 (8.00)**	161	-	98	**83**	11	-	9	**0**
PCB14	9017.00	-	9643.00 (-6.94)	**8873.00 (1.60)**	976	-	1007	**942**	104	-	139	**92**

Qualitative Results

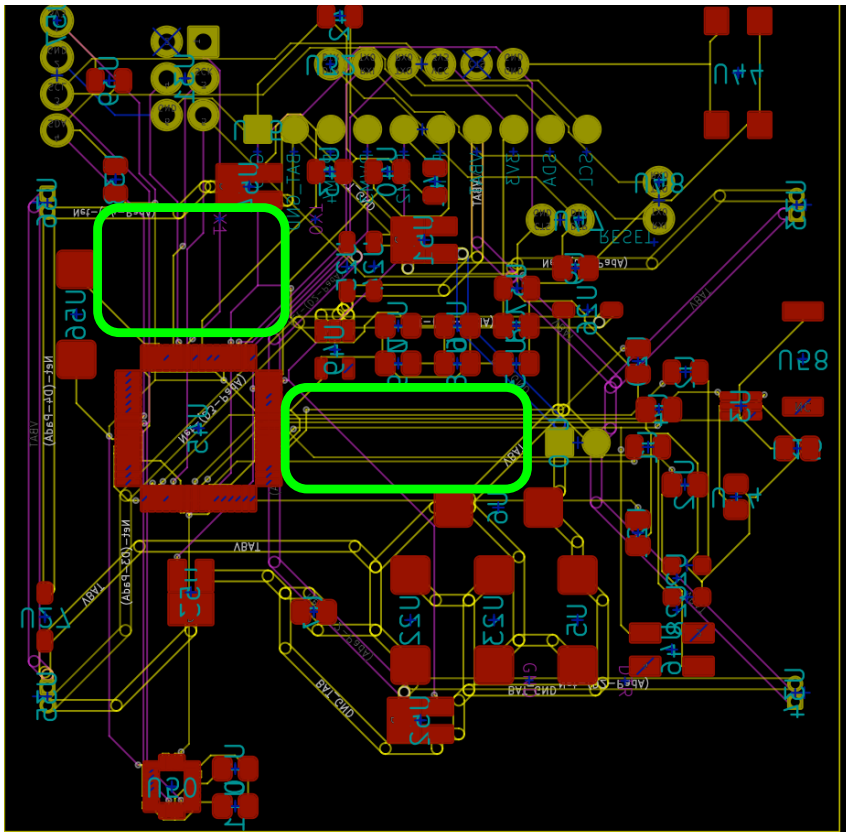


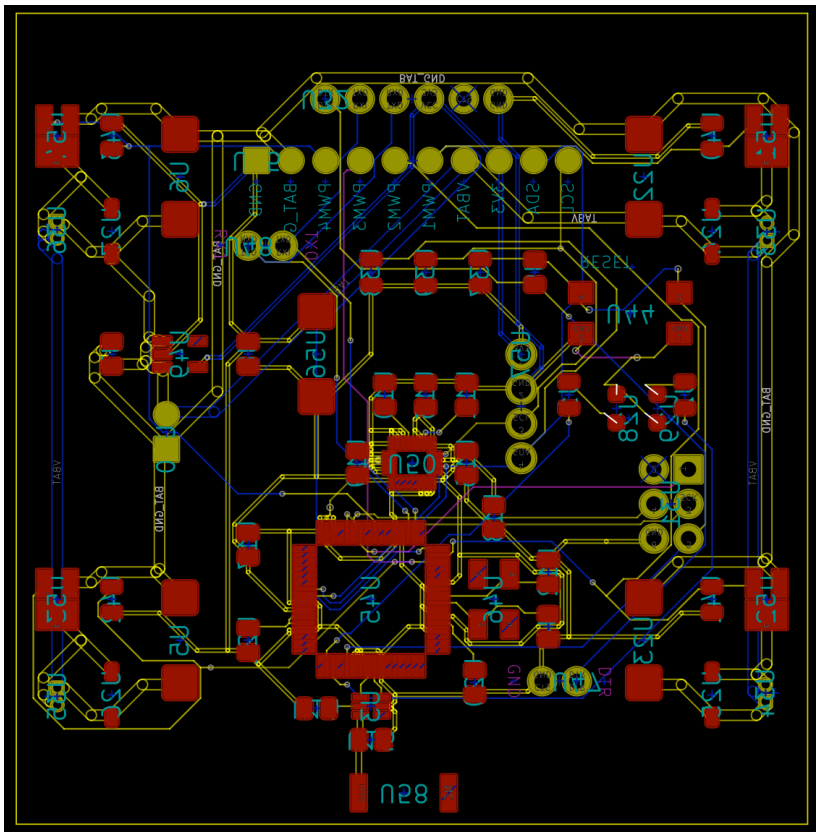






Qualitative Results





Conclusion and Future Work

- We have presented a novel algorithm which encourages routability of multi-pin nets in PCB designs.
- We perform an extensive study on 14 PCB designs
- 80.98%, 70.00%, and 74.68% reduction on average #DRVs and #unrouted nets for routability
- 34.36% fewer #Vias on average
- Investigating nonlinear separators, better initialization and optimization strategies