

CSE 243A (Section Id: 947925)

VLSI Computer-Aided Design

Synthesis Methodologies in VLSI Design & Test

Conference Reading List

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- Hsuan Hsiao and Jason H. Anderson. “Sensei: An area-reduction advisor for FPGA high-level synthesis” *Proceedings of the 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, March 2018, pp. 25-30. **Shaun; Nov. 28, 5:30 PM**
 - What are the similarities in the CNN models that the paper explored?
 - CNNs have been successful in capturing spatial features of images. The paper illustrates one possible approach to map DFG into an image as shown in Figure 6. What do you think are some strengths and shortcomings of the proposed mapping?
- Seogoo Lee, Lizy K. John and Andreas Gerstlauer. “High-level synthesis of approximate hardware under joint precision and voltage scaling” *Proceedings of the 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Lausanne, Switzerland, March 2017, pp. 187-192. **Elbruz; Nov. 28, 5:10 PM**
 - The paper solves the optimization problem by traversing the graph and greedily evaluates decision variables in a breadth-first manner in order of dependencies. Why does it choose this specific order?
- Shane T. Fleming and David B. Thomas. “StitchUp: automatic control flow protection for high level synthesis circuits” *Proceedings of the 53rd Annual Design Automation Conference, DAC*, Austin, TX, USA, June 2016, pp. 138:1–138:6. **Venkatesh; Dec. 3, 5:45 PM**
 - In what situations will the proposed soft error detection framework yield an LUT overhead similar to that resulted from DMR? Please explain.
- Matthew M. Ziegler, George Gristede and Victor V. Zyuban. “Power reduction by aggressive synthesis design space exploration” *International Symposium on Low Power Electronics and Design (ISLPED)*, Beijing, China, September 2013, pp. 421–426. **Darren; Nov. 28, 5:00 PM**
 - Ideally, the proposed exploration would investigate all parallel design points within a job step. What are some scenarios where a certain parallel design point is immediately withdrawn from consideration, or the creation of its derivative blast zone may be aborted?
- Ritchie Zhao, Mingxing Tan, Steve Dai and Zhiru Zhang. “Area-efficient pipelining for FPGA-targeted high-level synthesis” *Proceedings of the 52nd Annual Design Automation Conference*, San Francisco, CA, USA, June 2015, pp. 157:1–157:6. **William; Nov. 28, 5:50 PM**

- Suppose that the Reed-Solomon decoder shown in Figure 2 is to be instantiated with 4-bit LUTs without considering pipelining. what is the optimal number of LUTs? Please provide some justifications for your answer.
- Please summarize how the proposed MILP formulations handle the constraints related to pipelining.
- Feng Wang, Yuan Xie and Andrés Takach. “Variation-aware resource sharing and binding in behavioral synthesis” *Proceedings of the 14th Asia South Pacific Design Automation Conference*, Yokohama, Japan, January 2009, pp. 79–84. **Jinzhe; Nov. 28, 5:20 PM**
 - What are the metrics used to guide the optimization in resource sharing and binding? Why are they good metrics?
 - Section IV presents two atomic functions $sum(A,B)$ and $max(A,B)$. In what situations will we apply each function in the statistical timing analysis?
- Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo and Luca P. Carloni. “System-level memory optimization for high-level synthesis of component-based SoCs” *2014 International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2014*, Uttar Pradesh, India, October 2014, pp. 18:1–18:10. **Sivasankar; Nov. 28, 5:30 PM**
 - How does the proposed flexible memory controller allow the reuse of the same physical banks to store different data structures?
 - Please explain how the memory compatibility graph is constructed, and how to obtain the minimum number of parallel banks (M) from it.
- Xitong Gao, John Wickerson and George A. Constantinides. “Automatically Optimizing the Latency, Area, and Accuracy of C Programs for High-Level Synthesis” *Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, CA, USA, February 2016, 234–243. **Yiyu; Nov. 28, 6:00 PM**
 - The minimum latency transformation of Figure 1 is presented in the middle of page 3. Suppose that each operation is of unit delay. What is one possible execution order of instructions inside the loop? What is the minimum initiation interval (II_{min}) and the latency of the pipeline?
 - Comparing with SOAP2, whats the novelty of SOAP3 in its algorithm and transformation rules? Why are they introduced?