

CSE 243A (Section Id: 947925)

VLSI Computer-Aided Design

Synthesis Methodologies in VLSI Design & Test

Conference Reading List

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- Hsuan Hsiao and Jason H. Anderson. “Sensei: An area-reduction advisor for FPGA high-level synthesis” *Proceedings of the 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany, March 2018, pp. 25-30. **Shaun**
- Seogoo Lee, Lizy K. John and Andreas Gerstlauer. “High-level synthesis of approximate hardware under joint precision and voltage scaling” *Proceedings of the 2017 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Lausanne, Switzerland, March 2017, pp. 187-192. **Elbruz**
- Shane T. Fleming and David B. Thomas. “StitchUp: automatic control flow protection for high level synthesis circuits” *Proceedings of the 53rd Annual Design Automation Conference, DAC*, Austin, TX, USA, June 2016, pp. 138:1–138:6. **Venkatesh**
- Matthew M. Ziegler, George Gristede and Victor V. Zyuban. “Power reduction by aggressive synthesis design space exploration” *International Symposium on Low Power Electronics and Design (ISLPED)*, Beijing, China, September 2013, pp. 421–426. **Darren**
- Ritchie Zhao, Mingxing Tan, Steve Dai and Zhiru Zhang. “Area-efficient pipelining for FPGA-targeted high-level synthesis” *Proceedings of the 52nd Annual Design Automation Conference*, San Francisco, CA, USA, June 2015, pp. 157:1–157:6. **William**
- Feng Wang, Yuan Xie and Andrés Takach. “Variation-aware resource sharing and binding in behavioral synthesis” *Proceedings of the 14th Asia South Pacific Design Automation Conference*, Yokohama, Japan, January 2009, pp. 79–84. **Jinzhe**
- Christian Pilato, Paolo Mantovani, Giuseppe Di Guglielmo and Luca P. Carloni. “System-level memory optimization for high-level synthesis of component-based SoCs” *2014 International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2014*, Uttar Pradesh, India, October 2014, pp. 18:1–18:10. **Sivasankar**
- Xitong Gao, John Wickerson and George A. Constantinides. “Automatically Optimizing the Latency, Area, and Accuracy of C Programs for High-Level Synthesis” *Proceedings of the 2016 ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, Monterey, CA, USA, February 2016, 234–243. **Yiyu**