

INTERNATIONAL  
TECHNOLOGY ROADMAP  
FOR  
SEMICONDUCTORS

2011 EDITION

INTERCONNECT

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# INTERCONNECT

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## 1 SCOPE

The Interconnect chapter of the ITRS addresses the wiring system that distributes clock and other signals to the various functional blocks of a CMOS integrated circuit, along with providing necessary power and ground connections. The process scope begins at the contact level with the pre-metal dielectric and continues up to the wirebond pads, describing deposition, etch and planarization steps, along with any necessary etches, strips and cleans. A section on reliability and performance includes specifications for electromigration and calculations of delay. Expanded treatment of Emerging Interconnect and 3D integration are new features.

### 1.1 INTRODUCTION

The Interconnect chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap for Semiconductors (ITRS) emphasized an ongoing change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low- $\kappa$  dielectric introduction for microprocessors (MPUs) and application-specific ICs (ASICs) was one of the central issues for the 2003 ITRS Interconnect area. The 2005 ITRS showed the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A crosstalk metric was also introduced in 2007. Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, radio frequency (RF), or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuit/system functions on a chip. The fundamental development requirement for interconnect is to meet the high-bandwidth low-power signaling needs without introducing performance bottlenecks as scaling continues.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant indicated by the ITRS has been problematic. Fluorine doped silicon dioxide ( $\kappa = 3.7$ ) was introduced at 180 nm, however insulating materials with  $\kappa = 2.7$ – $3.0$  were not widely used until 90 nm. The reliability and yield issues associated with integration of these materials with dual damascene copper processing proved to be more challenging than expected. The integration of porous low- $\kappa$  materials is expected to be even more challenging. Since the development and integration of these new low- $\kappa$  materials is rather time invariant, the anticipated acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable  $\kappa$  to later technology generations. The various dielectric materials that are projected to comprise the integrated dual damascene dielectric stack for all years of the roadmap are depicted in the Dielectric Potential Solutions figure. The range of both the bulk  $\kappa$  values and effective  $\kappa$  values for the integrated dielectric stack are listed in the Technology Requirements Table INTC2. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge. (For a more thorough explanation, the Appendix illustrates the calculation of the effective  $\kappa$  for various integration schemes.) The imminent convergence of the M1 pitches for MPU and DRAM, expected by 2010, negates the need to identify a single technical product driver but technical specifications are included for both high performance logic and DRAM. A new table of INTC3 dedicated for flash memory is added because the most advanced M1 pitch is applied.

### 1.2 WHAT'S NEW FOR 2011?

- The Technology Requirements Table (INTC2) has been substantially kept with 2009 style as reorganized and divided into
  - General requirements – e.g., bulk resistivity and dielectric constant
  - Level specific requirements determined by the nature of the wire or via geometry – e.g., barrier thickness or effective resistivity

## 2 Interconnect

- Low- $\kappa$  roadmap – slightly changed
  - New range for bulk  $\kappa$
  - Air gaps expected to be solution for  $\kappa_{\text{bulk}} < 2.0$
  - First implementation will be for Flash
- ALD integration is still being investigated including the combination with appropriate dielectrics and barrier metals.
  - Barriers and nucleation layers are a critical challenge
  - Approaches of new liners (Co, Ru and others) stacked with barrier layers are proliferating
  - Capping metal for reliability improvement nearing production
- $J_{\text{max}}$  current limit model updated with relaxed on-chip clock frequency
  - Moves red zone by one to two years
- Revised 3D TSV roadmap tables
- Emerging interconnect solutions are being developed.
- All new interconnect variables are slow and will require substantial area savings to match/exceed the speed of repeated Cu/low- $\kappa$  with CMOS drivers; applications will likely be driven by new functionality enabled by emerging interconnects
- Novel state variables are slow relative to repeater-driven Cu/low- $\kappa$  and require significant area savings to maintain switching speed
- Evaluation of energy efficiency of emerging options necessitates joint consideration of switch and interconnect options

## 2 EXECUTIVE SUMMARY

For 2011, Interconnect performance is at the forefront as a key challenge to achieve overall chip performance. Air gap structures are now considered a mainstream potential solution for the ILD, recognizing their increased maturity. The ITRS team firmly believes that any substantial reduction in effective  $\kappa$  will not be achieved by further materials improvements of porous ultra-low- $\kappa$  ( $\kappa \leq 2$ ) but by the use of air gap structures. For low- $\kappa$ , this is the end of materials solutions and the beginning of architecture solutions. Delays in the emergence of quality ALD processes prevent the deposition of the required sub-2 nm barriers, and are a top concern. Discussions on 3D interconnects have been moved out of the emerging interconnect section, with TSVs nearing production.

In addition, the ITRS chapter contains significant new content on the search for Cu replacements and the need to consider interconnect requirements for the inevitable replacement for the FET switch. There are more radical options beyond even carbon nanotubes – including molecular interconnects, quantum waves and spin coupling – that are in the infant stages of development but, in each case, the goal is propagating terabits/second at femtojoules/bit.

### 2.1 DIFFICULT CHALLENGES

Table INTC1 highlights and differentiates the five key challenges in the near term ( $\geq 16$  nm) and long term ( $< 16$  nm). In the near term, the most difficult challenge for interconnects is the introduction of new materials that meet the wire conductivity requirements and reduce dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be mitigated.

Future effective  $\kappa$  requirements preclude the use of a trench etch stop for dual damascene structures. Dimensional control is a key challenge for present and future interconnect technology generations and the resulting difficult challenge for etch is to form precise trench and via structures in low- $\kappa$  dielectric material to reduce variability in RC. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low- $\kappa$  dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels.

*Table INTC1 2011 Interconnect Difficult Challenges*

<b>Five Most Critical Challenges <math>\geq 16</math> nm</b>	<b>Summary of Issues</b>
<b>Material</b> Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity	The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.
<b>Manufacturable Integration</b> Engineering manufacturable interconnect structures, processes and new materials	Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/package architecture design optimization tool
<b>Reliability</b> Achieving necessary reliability	New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.
<b>Metrology</b> Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.
<b>Cost &amp; Yield for Manufacturability</b> Manufacturability and defect management that meet overall cost/performance requirements	As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.

<b>Five Most Critical Challenges <math>&lt; 16</math> nm</b>	<b>Summary of Issues</b>
<b>Material</b> Mitigate impact of size effects in interconnect structures	Line and via sidewall roughness, intersection of porous low- $\kappa$ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.
<b>Metrology</b> Three-dimensional control of interconnect features (with its associated metrology) is required	Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.
<b>Process</b> Patterning, cleaning, and filling at nano dimensions	As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low- $\kappa$ dual damascene metal structures and DRAM at nano-dimensions.
<b>Complexity in Integration</b> Integration of new processes and structures, including interconnects for emerging devices	Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.
<b>Practical Approach for 3D</b> Identify solutions which address 3D structures and other packaging issues	3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.

## 2.2 INTERCONNECT ARCHITECTURES

### 2.2.1 INTRODUCTION

Two specific classes of products: Logic (MPUs and ASICs) and NAND flash memory are discussed. Technology requirement on NAND flash memory has been added for the first time as scalings on M1 interconnects pitches and its aspect ratio on contact layer are the most aggressive and they need further attention as the technology driver. Figure INTC1 shows a typical cross-section of hierarchical scaling for an MPU device (left), ASIC (middle) and Flash memory device (right).

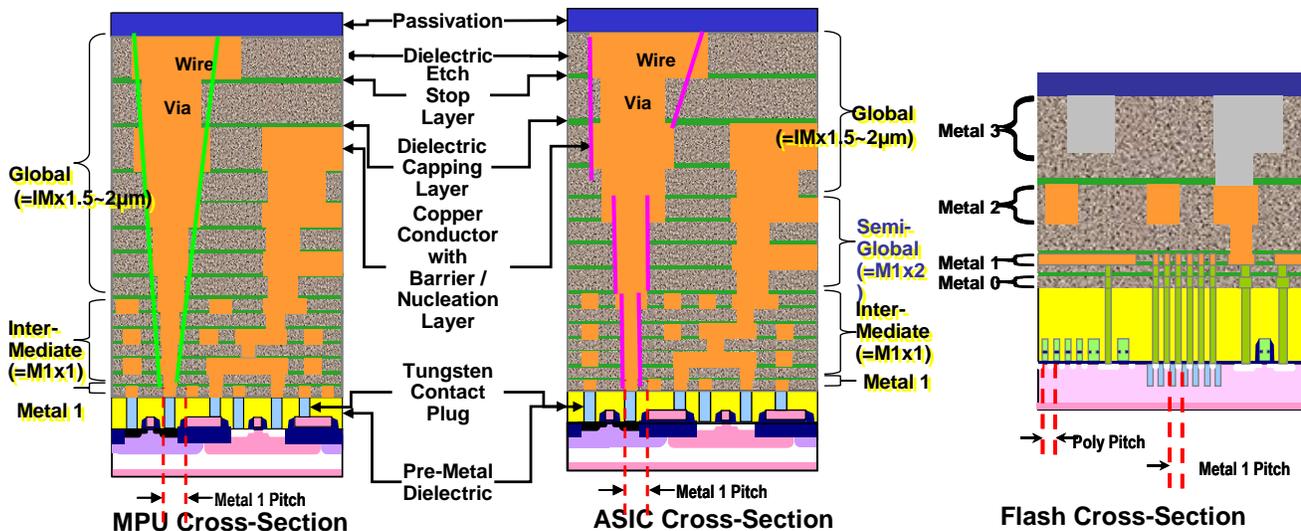


Figure INTC1 Typical Cross-sections of Hierarchical Scaling (MPU Device (left), ASIC (middle) and Flash memory (right))

### 2.2.2 LOGIC (MPU/ASIC)

MPUs utilize a high number of metal layers with a hierarchical wiring approach of steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified, solely to meet performance requirements. ASICs share many of the technology attributes of MPUs, for example, Cu wiring and low- $\kappa$  dielectrics. ASIC design methodology is generally more regular, consisting of M1, intermediate, semi-global ( $2\times$  intermediate) and global ( $4\times$  intermediate) wire pitches.

The accelerated scaling of MPU pitch has aggravated the copper electromigration problem.  $J_{\max}$  limits for current dielectric cap technologies for copper will be exceeded by 2017. Modification of the Cu surface to form CuSiN or use of alloys such as Cu-Al can yield significant electromigration improvements. Implementation of a selective metal cap technology for copper, such as CoWP, will result in even higher electromigration capability. However, there is still concern about yield loss due to metal shorts caused by these selective processes. Improved dielectric caps are also being explored.

Damascene process flows dominate MPU/ASIC fabrication methodologies. Figure INTC2 illustrates two typical inter-level dielectric (ILD) architectures used in the creation of interconnect wiring levels. Types of dielectric structures have been reduced from three to two (Inorganic/Organic hybrid structure has been removed). While current copper damascene processes utilize PVD Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to the end of the forecasted roadmap but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to

maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of damascene features. Surface segregated, CVD, ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required.

Accordingly, numbers of Cu resistivity for minimum M1, intermediate and global wires are now listed for all the years of the roadmap. The effect of this resistivity increase on the RC performance metrics is also calculated and included in the technology requirements table. The total variability of M1 wire resistance due to CD variation and scattering has been calculated and is also included in the MPU technology requirements table. Since the length of Metal 1 and intermediate wires usually shrinks with traditional scaling, the impact of their delay on performance is minor. Global interconnects, which have the greatest wire lengths, will be impacted most by the degraded delay. The benefit of materials changes or some amelioration of the Cu resistivity rise will be insufficient to meet overall performance requirements. The trend toward multi-core MPU design has alleviated some of the delay issues associated with ever increasing lengths of global interconnects

Introducing air-gap structures into Cu interconnects will be one of the most significant challenges in the coming decade. Several integration schemes and structures for air-gap formation have been reported. They can be classified into two categories according to whether gap formation is performed before or after the upper metal formation. In order to integrate air-gaps into Cu damascene structures, sacrificial materials located between metal lines must be removed because Cu-CMP should be carried out under non-gapped conditions.

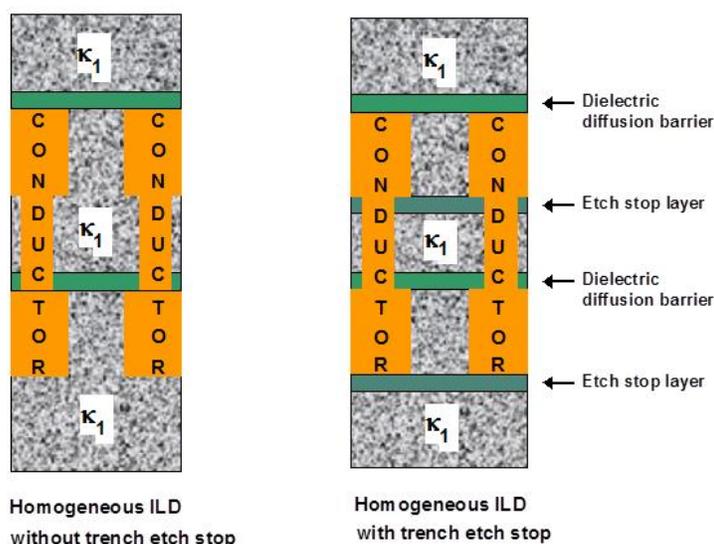


Figure INTC2 Typical ILD Architectures

### 2.2.3 MEMORY (FLASH)

Flash memory utilizes a simple hierarchical wiring with three or four metal layers. Bit-line (metal 1 layer) in flash memory reflects the most aggressive metal pitch, and its contact layer has the highest aspect ratio in all semiconductor devices. Therefore, they face the largest RC delay due to the size effect and the challenges on patterning and metal fill. Metal 2 layer and beyond utilize relaxed metal pitch.

As well as in logic device, process flows dominate flash memory fabrication methodologies. Copper damascene processes utilize PVD-based barriers and Cu nucleation layers and continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Technology requirements for metallization are listed in logic section above in detail. As a new trend, tungsten as the finest Bit-line interconnects material has been introduced for its advantage on metallization process, airgap formation and electromigration resistance. However it requires a design to deal with higher bulk resistivity than copper.

Electron scattering models have been improved and can now predict the Cu resistivity rise as a function of linewidth and aspect ratio. There is a significant contribution to the increase in resistivity by the electron scattering at both grain

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boundaries and interfaces. To date, research has not identified any potential solutions to this problem. Three-dimensional control of critical dimension (3DCD) interconnect features has been listed as one of the critical challenges in several editions of the ITRS.

Air-gap structure has been adapted ahead to other devices with the combination of tungsten interconnects. Formation of air-gap by plasma-CVD dielectric deposition into space between reactive ion-etched tungsten interconnects is a most promising solution. In copper damascene interconnects, introducing air-gap structure will still be challenging as well as in logic device. Usage of low- $\kappa$  materials in Bit-line can be effective to reduce capacitance; however, they need to have dielectric film properties to endure high voltage operations which are unique in flash memory.

*Table INTC2      MPU Interconnect Technology Requirements*

*Table INTC3      Flash Interconnect Technology Requirements*

*Table INTC4      DRAM Interconnect Technology Requirements*

## 2.3 3D INTERCONNECT ARCHITECTURES

### 2.3.1 INTRODUCTION

New developments in electronic system integration look increasingly to the third dimension for a variety of reasons, such as miniaturization, heterogeneous integration, improved circuit performance and lower power consumption. A broad variety of technologies is proposed by all players in the electronic manufacturing supply chain (IC foundry → wafer level processing (WLP) → semiconductor assembly and test (SAT) → printed circuit board (PCB) → assembly...), often blurring the traditional interfaces between them.

In order to come to a clear vision on roadmaps for 3D technologies, it is important to come to a clear definition of what is understood by 3D interconnect technology and to propose a classification of the wide variety of technologies. This definition should capture the functional requirements of 3D technology at the different hierarchical levels of the system and correspond to the supply chain manufacturing capabilities.

### 2.3.2 3D-INTERCONNECT TECHNOLOGY DEFINITIONS

When breaking down any electronic system into its basic components—the transistors, diodes, passive circuit elements, MEMS, etc.—we observe that electronic systems consist of two parts: the basic components and the highly complex interconnect fabric linking them. This interconnect fabric is organized in a hierarchical way, from narrow short interconnects between basic elements to longer and larger interconnects for interconnecting circuit blocks. For integrated circuits with well-defined local, intermediate and global interconnect layers, on chip circuit-hierarchy is organized from transistors to logic gates, sub-circuits, circuit-blocks, and finally, bond pad interface circuits. This is also the case for electronic systems as a whole, which typically consist of multiple integrated circuits, passive components, crystals, MEMS, etc., and which also are organized in different levels corresponding to, for example, the IC-package, system-on-package, module, board, rack, level. An example is the classification according to JISSO. [ <http://jisso.ipc.org> ]

Within a certain level of the interconnect hierarchy, interconnects are essentially routed in a 2D-topology: isolated lines are defined on a surface without crossing each other. Crossing of lines are realized on adjacent interconnect planes. Connections between planes are realized through features, such as vias, plated through holes, pins, solder balls, and/or connectors. These “via” interconnects allow for the 3D stacking of interconnect levels. The combination of basic circuit elements with multiple 2D-interconnect planes is considered a 2D-device, such as the integrated circuit or the printed circuit board.

What is commonly considered a “3D technology” today is a different type of “via” technology that allows for the stacking of basic electronic components in the third dimension, not only interconnect planes. This is the main distinctive feature of 3D integration technologies. It allows for the realization of electronic systems with very high packaging efficiency, measured either per unit area or per unit volume.

### **3D DEFINITIONS AND NAMING CONVENTIONS**

**3D Interconnect Technology**—technology which allows for the vertical stacking of layers of basic electronic components that are connected using a 2D-interconnect fabric are as follows:

- “Basic electronic components” are elementary circuit devices such as transistors, diodes, resistors, capacitors and inductors.
- A special case of 3D interconnect technology is the Si interposer structures that may only contain interconnect layers, although in many cases other basic electronic components (in particular decoupling capacitors) may be embedded into the interposer..

**3D Bonding**—operation that joins two die or wafer surfaces together

**3D Stacking**—operation that also realizes electrical interconnects between the two device levels

In table INTC5, a structured definition of 3D interconnect technologies is given based on the interconnect hierarchy. This structure also refers to the industrial semiconductor supply chain and allows definition of meaningful roadmaps and establishes targets for each layer of the interconnect hierarchy[1].

### **DEFINITIONS OF SUGGESTED NAMES**

**3D-Packaging (3D-P)**—3D integration using “traditional” packaging technologies, such as wirebonding, package-on-package stacking or embedding in printed circuit boards.

**3D-Wafer-Level-Packaging (3D-WLP)**—3D integration using wafer level packaging technologies, performed after wafer fabrication, such as flip-chip redistribution, redistribution interconnect, fan-in chip-size packaging, and fan-out reconstructed wafer chip-scale packaging

**3D-System-on-chip (3D-SOC)**—Circuit designed as a system-on-chip, SOC, but realized using multiple stacked die. 3D-interconnects directly connect circuit tiles in different die levels. These interconnects are at the level of global on-chip interconnects. This allows for extensive use/reuse of IP-blocks.

**3D-Stacked-Integrated-Circuit (3D-SIC)**—3D approach using direct interconnects between circuit blocks in different layers of the 3D die stack. Interconnects are on the global or intermediate on-chip interconnect levels. The 3D stack is characterized by a sequence of alternating front-end (devices) and back-end (interconnect) layers.

**3D-Integrated-Circuit (3D-IC)**—3D approach using direct stacking of active devices. Interconnects are on the local on-chip interconnect levels. The 3D stack is characterized by a stack of front-end devices, combined with a common back-end interconnect stack.

Table INTC5 presents a structured definition of 3D interconnect technologies based on the interconnect hierarchy. This structure also refers to the industrial semiconductor supply chain and allows definition of meaningful roadmaps and targets for each layer of the interconnect hierarchy. [1]

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*Table INTC5 3D Interconnect Technologies Based on the Interconnect Hierarchy*

Level	Suggested Name	Supply Chain	Key Characteristics
Package	3D-Packaging (3D-P)	OSAT, Assembly and PCB	<ul style="list-style-type: none"> <li>- Traditional packaging of interconnect technologies, e.g., wire-bonded die stacks, package-on-package stacks.</li> <li>- Also includes die in PCB integration</li> <li>- No through-Si-vias (TSVs)</li> </ul>
Bond-pad	3D-Wafer-level Package (3D-WLP)	Wafer-level Packaging	<ul style="list-style-type: none"> <li>- WLP infrastructure, such as redistribution layer (RDL) and bumping.</li> <li>- 3D interconnects are processed after the IC fabrication, “post IC-passivation” (via last process). Connections on bond-pad level.</li> <li>- TSV density requirements follow bond-pad density roadmaps.</li> </ul>
Global	3D-Stacked Integrated Circuit / 3D-System-on-Chip (3D-SIC /3D-SOC)	Wafer Fab	<ul style="list-style-type: none"> <li>- Stacking of large circuit blocks (tiles, IP-blocks, memory –banks), similar to an SOC approach but having circuits physically on different layers.</li> <li>- Unbuffered I/O drivers (Low C, little or no ESD protection on TSVs).</li> <li>- TSV density requirement significantly higher than 3D-WLP : Pitch requirement down to 4-16µm</li> </ul>
Intermediate	3D-SIC	Wafer Fab	<ul style="list-style-type: none"> <li>- Stacking of smaller circuit blocks, parts of IP-blocks stacked in vertical dimensions.</li> <li>- Mainly wafer-to-wafer stacking.</li> <li>- TSV density requirements very high: Pitch requirement down to 1-4 µm</li> </ul>
Local	3D-Integrated Circuit (3D-IC)	Wafer Fab	<ul style="list-style-type: none"> <li>- Stacking of transistor layers.</li> <li>- Common BEOL interconnect stack on multiple layers of FEOL.</li> <li>- Requires 3D connections at the density levels of local interconnects.</li> </ul>

### **3D-THROUGH-SI-VIA TECHNOLOGY DEFINITIONS**

A wide variety of technologies can be used to realize the 3D interconnect technologies described above. Of particular interest here are the so-called “Through-Si-Via” technologies used for 3D-WLP, 3D-SOC, and 3D-SIC interconnect technologies.

A Through Silicon Via connection is a galvanic connection between the two sides of a Si wafer that is electrically isolated from the substrate and from other TSV connections. The isolation layer surrounding the TSV conductor is called the *TSV liner*. The function of this layer is to electrically isolate the TSVs from the substrate and from each other. This layer also determines the TSV parasitic capacitance. In order to avoid diffusion of metal from the TSV into the Si-substrate, a *barrier layer* is used between the liner and the TSV metal.

Numerous methods have been proposed for realizing these TSV-stacked 3D-SIC and 3D-WLP structures. Common to all these approaches are three basic technology modules:

1. The Through-Si-Via process
2. Wafer thinning, thin wafer handling, and backside processing
3. The actual 3D-stacking process

The sequence of these process modules may vary, resulting in a large variation of proposed process flows, as shown in Figure INTC3.

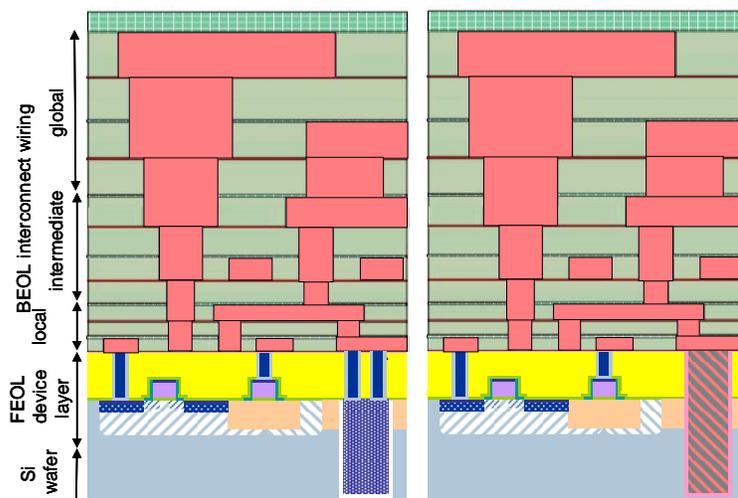


Figure INTC3 Schematic crosssections of TSV First and Middle/Last Process Flows

The different process flows may be characterized by four key differentiating characteristics:

1. The order of the TSV process with respect to the device wafer fabrication process: (see Figure INTC3)
  - “Via-first”—fabrication of TSVs before the Si front-end of line (FEOL) device fabrication processing.
  - “Via-middle”—fabrication of TSVs after the Si FEOL device fabrication processing but before the back-end of line (BEOL) interconnect process.
  - “Via-last”—fabrication of TSVs after or in the middle of the Si BEOL interconnect process from back side or front side.
2. The order of TSV processing and 3D-bonding—TSV before or after 3D-bonding<sup>1</sup>
3. The order of wafer thinning and 3D-bonding—Wafer thinning before or after 3D-bonding.
4. The method of 3D-bonding:
  - Wafer-to-wafer (W2W) bonding
  - Die-to-wafer (D2W) bonding
  - Die-to-die (D2D) bonding

In addition to these four main characteristics, three secondary characteristics are identified:

- *Face-to-Face* (F2F) or *Back-to-Face* (B2F) bonding
- For “via-last”: “*Frontside*” TSVs realized starting from the top surface of the wafer or “*Backside*” TSVs starting from the thinned wafer backside. (The top surface of the wafer being the side with the active devices and back-end interconnect layers)
- Removal of the carrier-wafer before or after bonding (i.e., temporary bonding and permanent bonding).

The generic flow characteristics defined above are applicable to 3D-WLP and global and intermediate interconnect level 3D-SIC process flows. For 3D-WLP TSV technology, the via-last flow is the most important and is realized before 3D bonding either as frontside or backside TSV, as shown in Figure INTC4.

The different approaches presented are not only applicable to regular semiconductor devices, but can also be applied to passive redistribution or interposer substrate layers. Key processing technologies for 3D integration are the various temporary or permanent bonding and debonding operations. The requirements for the materials and processes used may vary significantly, depending on the chosen route.

<sup>1</sup> In literature, sometimes TSV processing after 3D bonding is also referred to as “via last” technology. We however define “via last” in relation to the semiconductor wafer fabrication process, which makes the “via last” definition more general and not restricted to TSV after 3D bonding only.

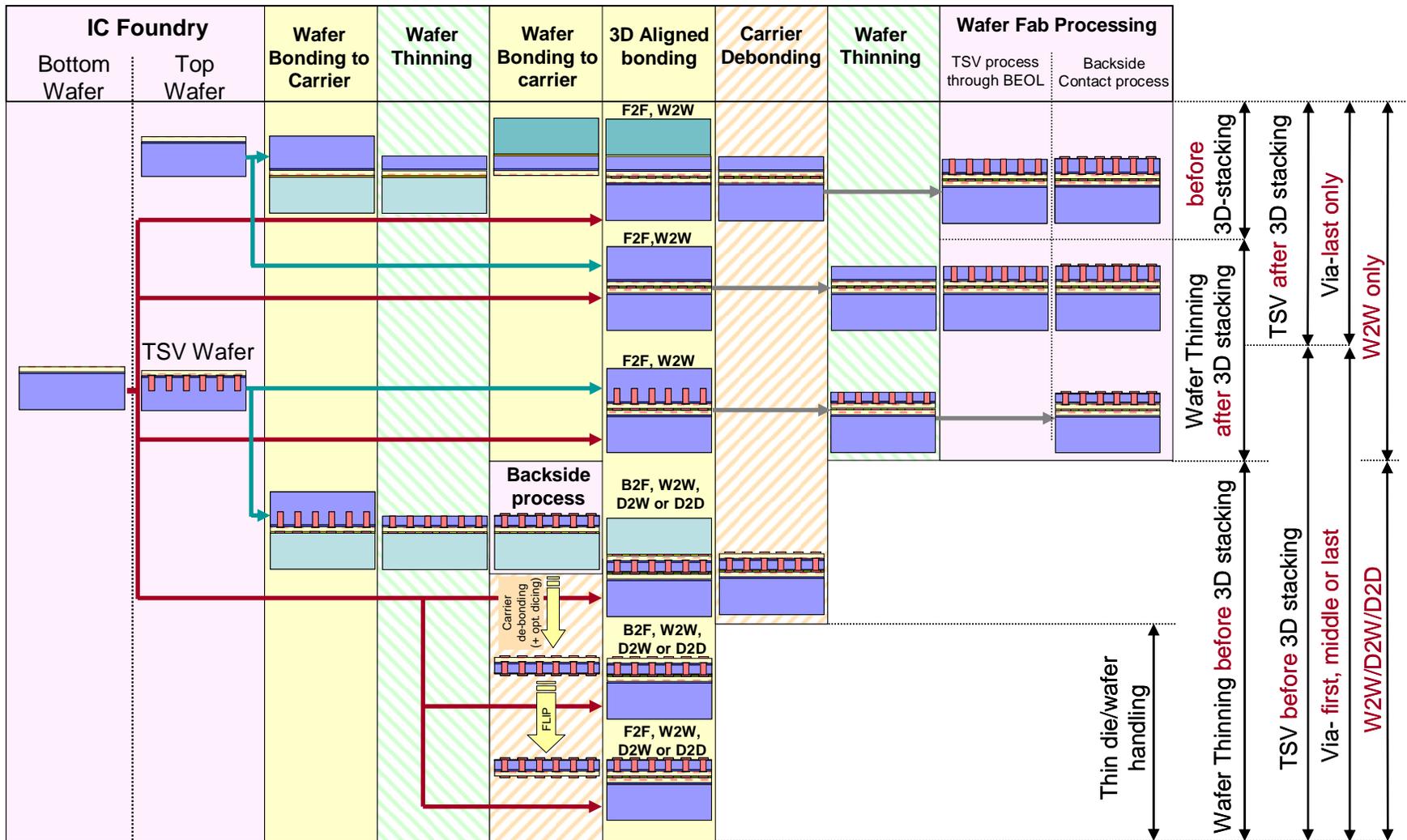


Figure INTC4 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-SIC Technologies<sup>2</sup>

<sup>2</sup> IMEC

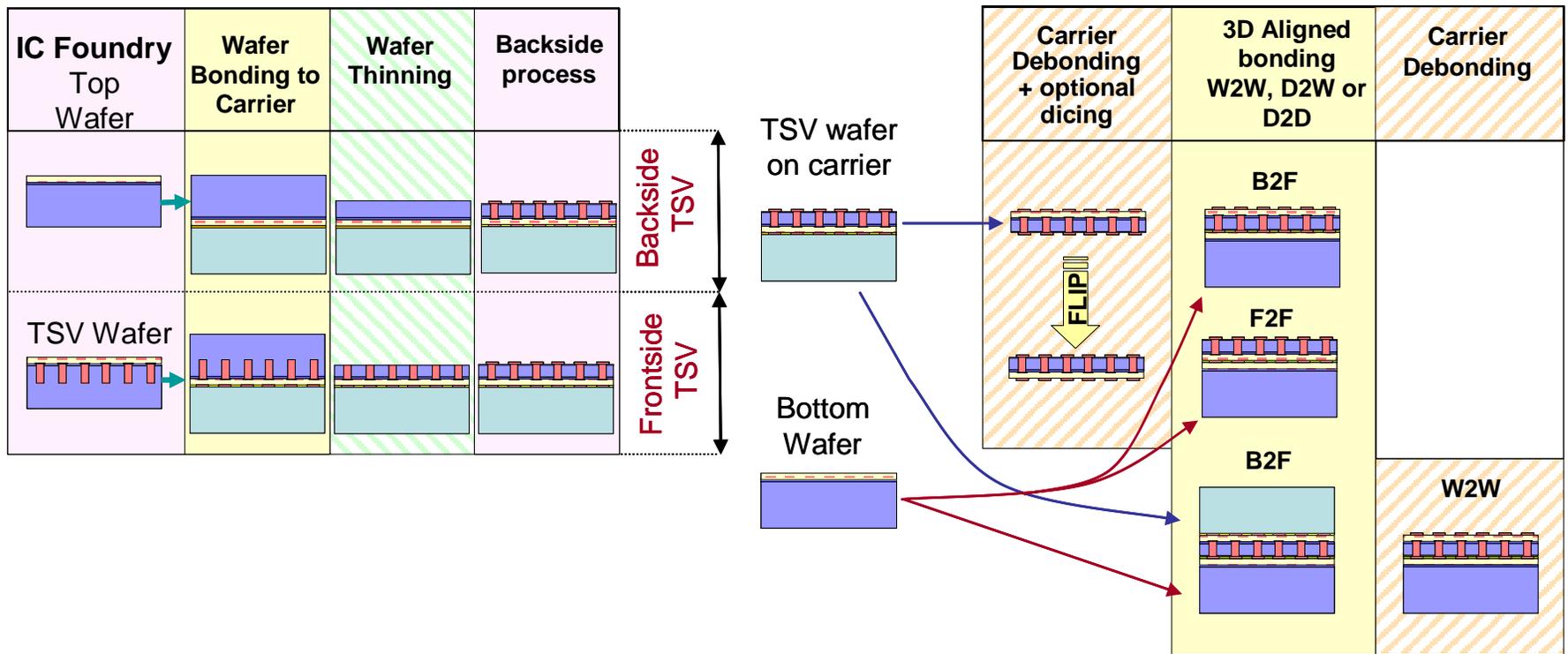


Figure INTC5 Schematic Representation of the Various Key Process Modules and 3D-stacking Options when using Through-Si-Via 3D-WLP Technologies<sup>3</sup>

<sup>3</sup> IMEC

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### 2.3.3 3D-TSV ROADMAP

Using the 3D interconnect hierarchy and 3D process definitions described above, it is possible to define TSV roadmaps in relation to the interconnect hierarchy they serve.

#### 3D-WLP

This is a 3D-technology for bond-pad level stacking. The 3D-TSV roadmap should therefore follow the chip I/O bond pad roadmap, as shown in Table INTC6.

*Table INTC6 3D-WLP Via Pitch Requirements Based on Table ORTC-4—Chip Pad Pitch Trend ( $\mu\text{m}$ )*

<i>Year of Production</i>	<i>2011</i>	<i>2012</i>	<i>2013</i>	<i>2014</i>	<i>2015</i>
1-row wedge-bond pitch ( $\mu\text{m}$ )	20	20	20	20	20
1-row ball pitch ( $\mu\text{m}$ )	35	35	30	30	25
2-row staggered pitch ( $\mu\text{m}$ )	45	40	40	40	40
Three-tier pitch ( $\mu\text{m}$ )	55	50	45	45	45
Area array flip-chip ( $\mu\text{m}$ ) (cost-performance, high-performance)	120	110	110	100	100

#### 3D-SIC

This technology is defined at two levels of the interconnect hierarchy.

1. 3D-SIC for connecting at the global interconnect level, e.g., 3D stacking of IP-blocks (3D-SOC). This technology allows for W2W, D2W and D2D stacking. This 3D-TSV process is typically integrated in the Si-wafer fabrication line. The 3D-stacking process is generally done outside the standard Si-process line. Details of the 3D-SIC/3D-SOC are shown in Table INTC7.

*Table INTC7 Global Interconnect Level 3D-SIC/3D-SOC Roadmap*

<i>Global Level, W2W, D2W or D2D 3D-stacking</i>	<i>2011-2014</i>	<i>2015-2018</i>
Minimum TSV diameter	4-8 $\mu\text{m}$	2-4 $\mu\text{m}$
Minimum TSV pitch	8-16 $\mu\text{m}$	4-8 $\mu\text{m}$
Minimum TSV depth	20-50 $\mu\text{m}$	20-50 $\mu\text{m}$
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 $\mu\text{m}$	0.5-1.0 $\mu\text{m}$
Minimum contact pitch (thermocompression)	10 $\mu\text{m}$	5 $\mu\text{m}$
Minimum contact pitch (solder $\mu\text{bump}$ )	20 $\mu\text{m}$	10 $\mu\text{m}$
Number of tiers	2-3	2-4

2. 3D-SIC for interconnects at the intermediate level, e.g., 3D stacking of smaller circuit blocks. This technology is mainly a W2W stacking technology.
3. Emerging Intermediate Interconnect Level 3D-SIC roadmap specifications are shown in Table INTC8. Both the 3D-TSV process and the 3D stacking are typically integrated in the Si-wafer fabrication line.

*Table INTC8 Intermediate Interconnect Level 3D-SIC Roadmap*

<i>Intermediate Level, W2W 3D-stacking</i>	<i>2011-2014</i>	<i>2015-2018</i>
Minimum TSV diameter	1-2 $\mu\text{m}$	0.8-1.5 $\mu\text{m}$
Minimum TSV pitch	2-4 $\mu\text{m}$	1.6-3.0 $\mu\text{m}$
Minimum TSV depth	6-10 $\mu\text{m}$	6-10 $\mu\text{m}$
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 $\mu\text{m}$	0.5-1.0 $\mu\text{m}$
Minimum contact pitch	2-3 $\mu\text{m}$	2-3 $\mu\text{m}$
Number of tiers	2-3	8-16 (DRAM)

### 2.3.4 3D-TSV CHALLENGES

- Large variety of approaches and compatibility with the microelectronic industrial supply chain  
Due to the large variety of approaches for 3D integration, the supply chain, and the possible flows for 3D integration, defining the limits or solutions is beyond the scope of this work. Many of the choices will be dictated by the available capabilities of the various manufacturers in the supply chain and business decisions. Clear definitions of ownership will be critical to the success of the non-IDM business.
- Compound yield—design and test strategies for obtaining high yield 3D-stacked devices
- Design challenges—required tool capabilities for seamless heterogeneous 3D system design
- Interactions between the 3D interconnect and the device packaging and assembly requirements
- Electrical requirements for 3D-interconnects—RLC values for different application regimes  
The main challenge with TSV parasitics is to achieve a low TSV capacitance. The delay and power consumption of 3D-interconnects using TSVs will be mainly determined by the TSV capacitance. This capacitance should be on the order of the capacitance of global interconnect wiring in equivalent 2D-circuits to avoid degradation of circuit performance by going to 3D stacking. This requirement puts an upper limit on the TSV capacitance for a given technologies
- Electrostatic discharge (ESD) protection of the devices during the 3D process sequence  
While 3D promises a dramatic increase in the number of I/O on a layer of Si, these implementations lead to a corresponding increase in the number of circuit elements exposed to ESD. The fine pitch of these new tier-to-tier I/O limit the Si area available to provide active ESD protection. Thus, the design and manufacturing of 3D devices require that attention is paid to the protection of circuits from ESD.  
3D manufacturing brings new sources of ESD during such steps as wafer handling, TSV etch, TSV liner, TSV fill, bonding, debonding and stacking. While little is currently known about the level of possible ESD damage these new steps may generate, every effort should be made to reduce ESD in 3D manufacturing. This is required to keep the size (cost) of ESD protection of 3D circuit elements to a minimum. Once the 3D structure is fully integrated, ESD protection is no longer required unless the 3D structure is part of an external path for I/O/P or G. Thus, any ESD protection for internal 3D elements will be a liability adding to the active power and reducing circuit performance.
- Cost of ownership
- Factory integration of processing using bonded and/or thinned wafers  
Backside processing of bonded and thinned wafers is required in many of the process flows described above. This presents a number of manufacturing and factory integration challenges. In many cases, these wafers will deviate from the SEMI M1.15 spec for 300 mm wafers. This spec covers such items as wafer diameter, thickness, notch, and edge bevel.<sup>4</sup> This standard is referenced by other SEMI standards that deal with FOUPs (E47.1), FOSBs (M31), Load ports (E15.1), and Wafer identification (T7).<sup>5</sup> Depending on the specific 3D processes used, bonded and thinned wafers may be in violation of several of these specs. Also, introducing bonded and thinned wafers into a fab requires ensuring that they can be safely re-introduced into the line without causing contamination or added particles, and qualifying them on each of the tools in the manufacturing flow for both wafer transport issues and tool-specific processing issues. Examples include possible hardware and/or software adjustments for handling thicker wafers and accommodations for the different edge zone.
- Particles and issues of cross-contamination
- Advanced process control requirements
- Environmental, Safety, and Health (ESH) regulation concerns  
Carbon emissions regulation—carbon footprint impact to the environment given the significantly larger volume of patterning feature sizes that require high chemical usage (e.g., SF<sub>6</sub>)

<sup>4</sup> M1.15. SEMI M1.15, Standard for 300 mm Polished Monocrystalline Silicon Wafers (Notched)

<sup>5</sup> E47.1. Mechanical Specification for FOUPS Used to Transport and Store 300 mm Wafers, 1997.

### 2.4 PASSIVE DEVICES

#### 2.4.1 INTRODUCTION

Recently an increasing trend was observed to move discrete passive devices from board level to the package level and to the chip level as well. This trend provides new and demanding challenges for on-chip interconnect architectures in current and future technology nodes. This request for precision and high quality capacitors, inductors and resistors is mainly driven by advanced mixed-signal, high frequency (RF) and system-on-a-chip (SoC) applications. Reduction and control of substrate coupling noise and other parasitics for mixed-signal and RF CMOS applications is one of the major tasks. From an application point of view the most important requirements for passives are listed in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter. In the past, the traditional method of realizing passive circuit elements (for example, capacitors, resistors) on ICs was the integration during front end processing. In this case doped mono-crystalline Si substrate, poly-crystalline Si and Si-oxides or Si-oxynitrides are used. Because of their vicinity to the Si substrate, those passive devices fabricated during front end processing suffer significant performance degradation, especially when used at high frequencies. Therefore, there is an increasing demand to realize low loss, low parasitics, but high quality passive devices in the interconnect levels, providing a larger distance to the Si-substrate.

For interconnect integration the key challenge is to achieve this goal in a modular and cost-effective way, without sacrificing the overall interconnect performance and reliability. Currently two fundamentally different approaches are pursued for on-chip integration. One is the introduction of optional or additional interconnect levels in combination with new materials to accomplish the necessary functions and attributes with the highest Q-factors and a minimum usage of additional chip area. In general, this approach has the disadvantage of higher process complexity and potentially higher manufacturing cost. The alternative is simply to design passive devices by using native or “parasitic” properties, e.g., capacitance, inductance and resistance, of the existing interconnect levels. This second approach is the least demanding for wafer manufacturing, but suffers typically by reduced Q-factors of the passive devices and a larger consumption of precious chip area. Other approaches make use of post-passivation redistribution layers of the wafer-level package or may integrate the passive devices directly into the package. Innovative system-in-a-package (SiP) modules or 3D IC stacking techniques with through-silicon-vias (TSV) may also be used more frequently to replace the highly complex and expensive SoC manufacturing process. In the end, cost considerations are expected to become the decisive arguments in the selection of the optimal approach to realize passive elements with sufficient system performance, quality and reliability.

#### 2.4.2 CAPACITORS

##### MIM CAPACITORS

High quality metal-insulator-metal (MIM) capacitors are widely used in CMOS, BICMOS and bipolar chips. Typical applications are filter and analog capacitors (for example, in A/D or D/A converters), decoupling capacitors, RF coupling and RF bypass capacitors in RF oscillators, resonator circuits and matching networks. Key attributes of MIM capacitors are high linearity over broad voltage ranges (low voltage coefficients), low series resistance, good matching properties, small temperature coefficients, low leakage currents, high breakdown voltage and sufficient dielectric reliability.

The economic demand for small chip area consumption leads directly to the request for higher MIM charge storage densities. Above a capacitance density of  $2 \text{ fF}/\mu\text{m}^2$ , a further thinning of the traditionally used Si-oxide or Si-nitride dielectrics is no longer useful because of increased leakage currents and reduced dielectric reliability. Therefore new high- $\kappa$  dielectric materials, such as  $\text{Al}_2\text{O}_3$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{HfO}_2$ ,  $\text{Nb}_2\text{O}_5$ ,  $\text{TiTaO}$ , BST, STO, etc. or laminated layer stacks of different materials are being evaluated as MIM dielectrics and may be used in future applications.

As always, the introduction of new materials leads to new challenges in material processing (such as advanced PVD, CVD or ALD deposition methods), process integration and reliability. High quality films with excellent thickness uniformity, low defect densities and high dielectric constants need to be deposited below  $450 \text{ }^\circ\text{C}$  to be compatible with the overall interconnect architecture. To reduce parasitic substrate coupling and allow for high quality factors of the MIM capacitors, integration into upper metallization levels is preferred.

Low resistive capacitor electrodes and perfectly engineered electrode-dielectric interfaces are necessary to achieve high MIM quality factors and the required reliability targets. Some promising integrations of high  $\kappa$  materials in MIM capacitors have been demonstrated in the literature (see the *Appendix: Passive Devices*).

## **INTERMETAL CAPACITORS**

The main disadvantage of MIM capacitors is the higher process complexity (i.e. typically 2 additional lithography and patterning steps) resulting in added cost during wafer manufacturing. Therefore alternative approaches making use of the native or 'parasitic' inter-metal capacitance between metal layers and metal lines in minimal design rules are getting more and more attractive, especially for advanced CMOS technologies beyond the 90nm node. Capacitors consisting of interdigitated metal fingers and interlayer vias are stacked over several metal layers and can be designed and built in the ordinary interconnect scheme without any additional process steps. Depending on the number of metal layers used and the minimum design rules it is realistic to achieve capacitance densities between 2 - 4 fF/ $\mu\text{m}^2$  or even more. Today these 3D stacks of vertical parallel plate (VPP) capacitors, vertical natural capacitors (VNCAP) or metal-over-metal (MOM) capacitors are standard offerings in advanced CMOS platform technologies with Q-factors > 20 at GHz frequencies. The increasing capacitance densities of VPP or MOM capacitors due to the scaling of metal line width and metal spacing makes their use even more attractive in future technology nodes. The only open question remains, whether the porous low- $\kappa$  dielectrics in between the minimum metal spacings are able to pass the leakage current and dielectric reliability targets of the capacitor structures.

### **2.4.3 INDUCTORS**

High quality on-chip inductors are critical components in analog/mixed signal and high frequency (RF) applications. Currently they are widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers and low noise amplifiers (LNA). Key attributes are high quality factors, Q, at high inductance, high self-resonance frequency, low ohmic losses, low eddy currents and low capacitive substrate losses.

Today, spiral inductors in the upper thick Al- or Cu-metallization levels are most widely used in order to fabricate low resistive coils with sufficient spacing from the Si-substrate to achieve optimized quality factors. These simple spiral inductors can be fabricated relatively easily using standard interconnect processes. In several standard CMOS platform technologies optional super-fat wiring levels with metal thicknesses between 2 - 8  $\mu\text{m}$  are offered to realize specific high Q inductors. But they may not in every case be good enough to fulfill all future RF requirements. Therefore, some more advanced constructions and approaches are being pursued.

Examples like shunted coils, realized in several metallization levels, the use of metallic or even magnetic ground planes, suspended spiral inductors in air-gaps, post passivation add-on modules with coils in fat redistribution metal layers (several  $\mu\text{m}$  metal thickness) or solenoidal inductors with and without ferro-magnetic core fillings have been successfully demonstrated. Other possibilities for reducing substrate losses is the use of high Ohmic Si substrates, SOI substrates or localized semi-insulating Si-substrate areas after ion- or proton- bombardment (see appendix: Passive devices).

However, not all of these alternative fabrication schemes are suitable for manufacturing, because of integration and process complexity issues or incompatibilities with device or product requirements. These different inductor concepts are an expression of the constant struggle between low manufacturing costs on the one side and the best possible performance (i.e. highest inductance at high frequencies; Q-factor improvement by reducing ohmic losses in the coil and by reducing parasitic substrate coupling) on the other side.

### **2.4.4 RESISTORS**

Precision thin film resistors are used in analog and mixed signal circuits and specific SoC applications. Key attributes are precise resistance control, excellent matching properties, high voltage linearity, low temperature coefficients, low 1/f noise and low parasitics resulting in high Q values. Today the most widely used Si-substrate-, poly-Si-, or silicide-resistors fabricated during front end processing suffer mainly from poor 1/f noise performance and substrate losses.

Thin film resistors in the metallization levels can significantly improve the 1/f noise performance and other substrate losses. Key challenges for resistors in the interconnect are finding materials with moderate and tunable sheet resistance compatible with the standard interconnect materials and integration schemes, excellent thickness control and good etch selectivity to dielectrics with a modular integration scheme. Especially for Cu-metallization schemes, TaN has been found to be a promising candidate; however, other materials may be used in the near future.

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More details on the applications, typical requirements, the processing and integration challenges of the different passive devices (capacitors, inductors and resistors), including a list of recent references, can be found in the interconnect appendix section on ‘Passive Devices’.

### 2.5 MORE MOORE VS. MORE THAN MOORE

More Moore from an interconnect perspective is the embodiment of continued conventional scaling. This scaling from an interconnect perspective includes the use of new materials, processes, tools and most importantly design. Layout and design will become ever more important to push More Moore by shorting the local interconnect. This trend will need to be maintained until material breakthroughs, especially in ULKs and copper replacements, occur that can overcome the current RC trends.

More than Moore still seems to be evolving. It is a push for much closer integration between CMOS other diverse analog applications including RF, Biochips sensors, actuators, power, and imaging, are applications. From an interconnect perspective these system could be incorporated with conventional CMOS through chip stacking using TSVs or in some cases optical interconnect. The details should be referred to the More than Moore White Paper.

## 3 RELIABILITY AND PERFORMANCE

### 3.1 RELIABILITY

#### 3.1.1 INTRODUCTION

Rapid changes are occurring in interconnect materials and structures resulting in significant new reliability challenges. Failures are further exacerbated by continued increases in interconnect density, number of layers, and power consumption.

An interconnect system is typically composed of insulating dielectric materials and conductors arranged in a multilevel scheme, followed by chip packaging. In the case of Cu-based metallization, metallic and dielectric diffusion barriers are used to prevent copper migration into the dielectric. Each of these components plays an important role in the reliability of the system. The implementation of today’s copper low- $\kappa$  interconnects is strongly impacted by reliability, both for metals and dielectrics.

Metal reliability is generally assessed by studying electro-migration (EM) and stress induced voiding (SIV), while dielectric reliability is assessed by leakage and time dependent dielectric breakdown (TDDB) or triangular voltage (TVS) sweep measurements. Numerous novel barrier metals, alloys of copper and copper cap layers were recently proposed in order to cope with the increasing current density that conductors have to carry. While the theoretical description of the EM phenomenon is well-understood, due to the large number of possible combinations, careful testing of these schemes is important, in order to identify active failure mechanisms. As dielectric spacing between adjacent copper wires scales, BEOL dielectric reliability is becoming an increasingly important challenge, both for advanced logic and for memory devices.

While concerns regarding the importance of dielectric reliability are widespread in the community, strategies to assess and predict the expected lifetime at product level are lacking in consensus. It is commonly acknowledged that ensuring the necessary low- $\kappa$  dielectric reliability margins is increasingly difficult [1-3] and that the importance of BEOL dielectric reliability increases with dimension and material scaling. The lack of consensus and of a fundamental understanding of BEOL dielectric reliability models, statistics and dominating controllable factors, calls for concentrated efforts on this topic.

Identification of failure modes and establishing correct prediction models is crucial. These models can be used for predicting reliability limits of entire circuits and of systems. In some cases, by monitoring the degradation of system and circuit parameters (due to degradation of metals and dielectrics) it may be possible to extend the reliability limits of the entire system by reducing the workload on one part of the circuit. Finally, in the context of full IC-system reliability, chip package interactions should not be neglected.

### 3.1.2 METALLIZATION RELIABILITY

#### ELECTROMIGRATION

Electromigration failures are generally described with Black's equation [4] which determines the maximum current density ( $J_{EM}$ ) which can safely flow in a wire. The most common metals in today's ICs are aluminum and copper. Cu interconnects were introduced in 1997, in a damascene scheme, to reduce wiring delay, but Al interconnects remain for specific applications and at several levels in multilevel interconnects. Electromigration limited current is currently investigated in Al interconnects using the usual EM physics rules.

#### ELECTROMIGRATION SCALING MODEL

In an interconnect subjected to an electrical current, the Cu atomic drift velocity is determined with an effective diffusion coefficient which takes into account the possible atomic diffusion paths existing in a metal [5]. An experimental EM activation energy (0.9eV) has been agreed upon and shown to remain constant over the interconnect nodes for the most common integration scheme: dual damascene Cu with a PVD TaN/Ta sidewall barrier and a Si(C)N dielectric cap layer. Following this, it is straightforward to consider that the EM-induced void growth rate remains constant for a given interconnect scheme, independent of interconnect geometry. Some authors report a risk of grain boundary diffusion in very narrow linewidths associated with an  $E_a = 0.85\text{eV}$ . [6]

The lifetime ( $\tau$ ) of an interconnect is the time to reach the minimum void size which is able to electrically open the interconnect. Using the assumption, that the void is located at the cathode end of the interconnect wire containing a single via (Figure INTC6) it has been shown [7] that  $\tau$  scales with  $w^3/h^2j$ , where  $w$  is the linewidth of the interconnect (or the via diameter),  $h$  the interconnect thickness, and  $j$  the electrical current density responsible for electromigration Cu diffusion.

Besides the decrease of lifetime by half each new generation for minimum designed metal linewidth (Figure INTC7), interconnects are ever more sensitive to small process variations. For instance 10 % increase of via height or reduction of line width may induce bimodal lifetime distribution and early failures that result in EM lifetime reduction significantly above the current density variation. This has been attributed to poor coverage of barrier or Cu seed which induces a risk of enhanced Cu diffusion. This may happen at via / trench transition and is critical for lifetime of interconnects with current upstream direction. Poor coverage may also be located at line sidewall as a consequence of trench profile and it is critical for lifetime with current downstream direction.

$J_{EM}$  is the maximum current density providing the targeted lifetime and scales with the product  $w^3/h^2$ .  $J_{max}$  is defined by the maximum equivalent dc current expected to appear in a high-performance digital circuit divided by the cross-sectional area of an intermediate wire, which was calculated by the model shown in Figure INTC8. The comparison of the evolution of  $J_{max}$  and  $J_{EM}$  limited by the interconnect geometry scaling is shown in Figure INTC9.  $J_{max}$  increases with scaling due to reduction in the interconnect cross-section and increase in the maximum operating frequency.  $J_{max}$  will exceed the  $J_{EM}$  limit of conventional copper interconnects.

#### PROCESS OPTIONS TO OVERCOME $J_{EM}$ LIMIT

Process options should be oriented towards solutions to decrease Cu drift velocity [8]. Recent research has shown that there are at least three main experimental directions to reduce Cu drift velocity:

1. Cu surface engineering before the SiCN deposition layer, also referred to CuSiN cap
2. Replacing the actual dielectric cap Si(C)N by a metal cap based on Co alloys such as CoWP or Co CVD deposited
3. Adding Ti, Al, Mn, Ge, Co, ... doping either with alloyed seed layers or by adding a CVD liner between the barrier and the pure Cu seed.

In these process options, the reduction of Cu drift is obtained with fine technology processing because dopants have to move from the trench sidewall and segregate at the trench surface. Strengthening the top interface is the way to reduce interface Cu diffusion. Another possible mechanism is simultaneously obtained with blocking grain boundary diffusion when dopants segregate at grain boundaries.

One should pay attention to the possible interconnect resistance increase of such Cu alloying processes [24]. (See also Figure INTC10 to compare the lifetime improvement versus the resistivity increase)

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### **LINE WIDTH EFFECT TO RELAX $J_{EM}$**

Because grain boundary diffusion may also be an active path for Cu electromigration for today's nodes, interconnect microstructure plays an active role in lifetime [25]. In the actual interconnect technology, very small grain size and polycrystalline microstructure have been obtained in the smallest linewidths [26]. Increasing linewidth has a positive impact to increase average grain size and to limit void growth rate. In recent research, [27] increasing linewidth around a ratio of 2 results in significant lifetime increase. This provides margins for maximum current capability in interconnect as a function of linewidth.

### **LINE LENGTH EFFECT (OR BLECH LENGTH) TO RELAX $J_{EM}$**

From early studies of electromigration, it has been shown that short length interconnects (also called Blech length  $L_B$ ) could be immortal [9]. Immortality is reached for any current density or wire length below the critical product:  $J_C * L_B$ . This critical product is the consequence of the mechanical confinement of the metal in the interconnect structure. Experimental research indicates a rather wide range of this immortality criteria with  $J_C * L_B$  ranging from 1500 and 5000 A/cm.

More recently, it has been shown that other immortality criteria can be considered to model electromigration behavior in actual interconnects. [10] This proposal is based on the observation that a void can nucleate and reach a saturation size as the consequence of the backflow effect first proposed by Blech. [11] There are current (J) and length (L) conditions [28] in which a stable void is created in interconnect without an open circuit. This new criterion is a function of  $J * L^2$ .

### **ELECTROMIGRATION IN INTERCONNECTS WITH TSV APPROACH**

For a copper metal line connected to a TSV, electromigration physics are still the same regarding void nucleation and copper diffusion. For instance with a TSV with a diameter in the 1 to 10 $\mu$ m range, and any aspect ratio, void is nucleated at the cathode side right below the TSV in the adjacent redistribution line (RDL) with in plane dimension at least equal of the TSV diameter. Then experimental activation energy of 0.9eV has been reported [29]. Similar methodology than for conventional interconnects can be applied to determine maximum current capability in interconnects with TSV.

### **ELECTROMIGRATION OF SAC BUMPS OR CU PILLAR**

A clear difference in electromigration behavior is expected with solder bumps or Cu pillar flip chip packaging. The formation of intermetallic compounds (IMC) occurs with thermal annealing during process and with current stressing during electromigration [30]. Two main cases can be distinguished:

- EM induced voiding may occur at the interface between the IMC and the solder (SnAg). Electromigration parameters could be derived by fitting Black's equation and gives an activation energy  $\sim 0.9$ eV and a current density exponent in the range of 1.5 to 3.5 [31, 32].
- On the contrary, when solder material can be fully transformed into IMC (e.g. with Cu pillar architecture) electromigration degradation is no longer expected during reasonable current and temperature stressing which are compatible with packaging material.

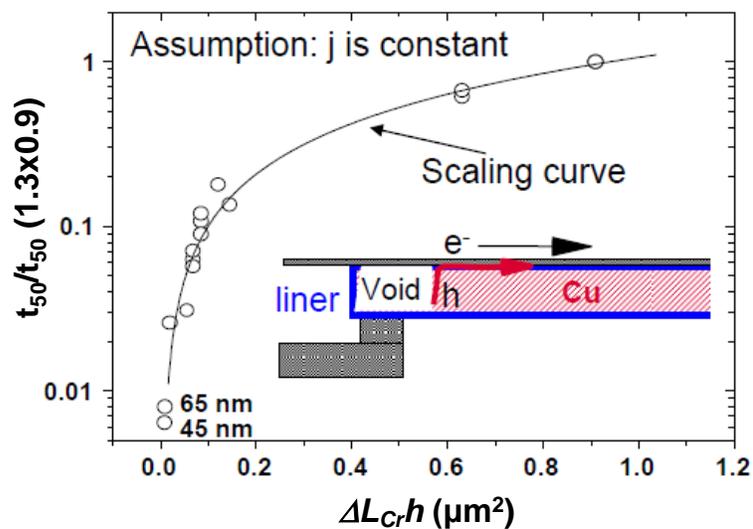


Figure INTC6 Experiment and model of lifetime scaling versus interconnect geometry (reprinted from Ref 7)

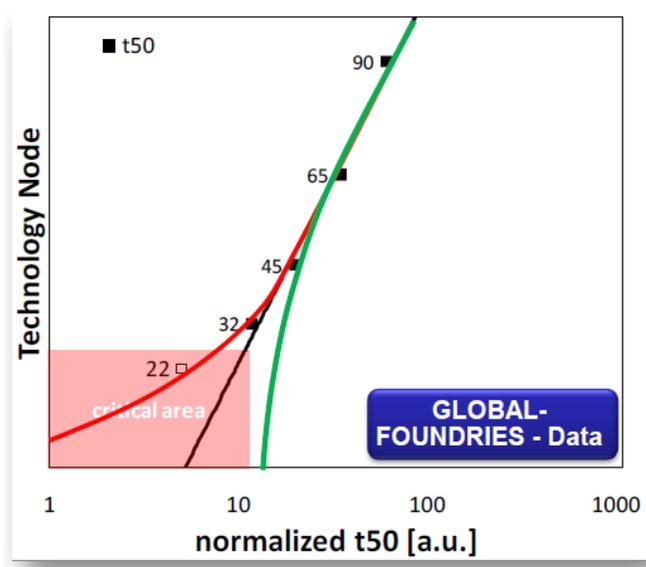
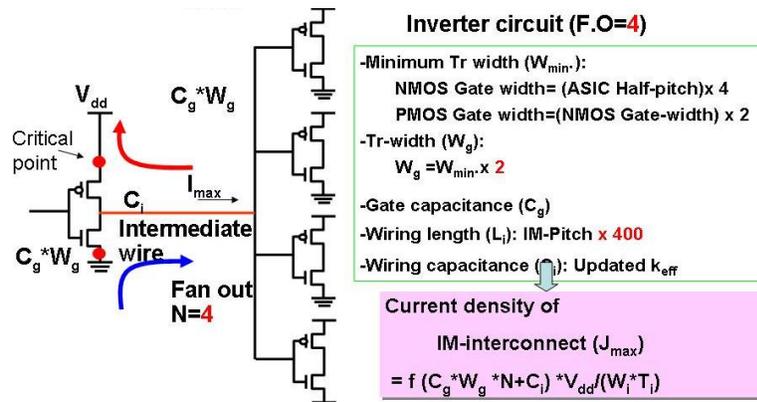


Figure INTC7 Evolution of lifetime versus technology node. Black line shows the effect of reduced critical void volume : Green line shows the EM enhancement urgently needed (Courtesies of A. Auel/ Globalfoundries)



Calculation model for  $J_{max}$ , which is the maximum equivalent dc current expected to appear in a high-performance digital circuit and divided by the cross-sectional area of an intermediate wire.  $J_{max}$  is calculated as a metric for EM reliability, and not taking requirement from RC delay into consideration. The model is basically the same from 1999, however, the parameters have been changed or updated to accord with realistic  $J_{max}$  value at the time.

Figure INTC8 Calculation Model for  $J_{max}$

(The maximum equivalent dc current expected to appear in a high-performance digital circuit divided by the cross-sectional area of an intermediate wire.)

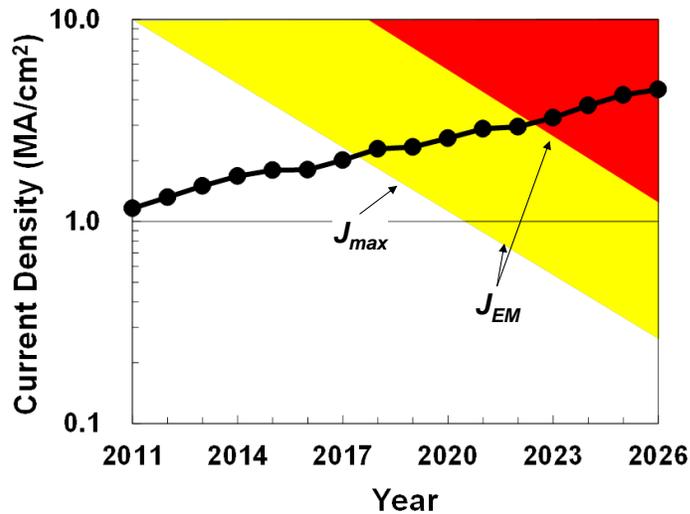


Figure INTC9 Evolution of  $J_{max}$  (from device requirement) and  $J_{EM}$  (from targeted lifetime)

( $J_{max}$  will increase with frequency and reducing cross-section, while  $J_{EM}$  will scale with the product  $w \cdot h$  according to EM lifetime dependence on wiring width.)

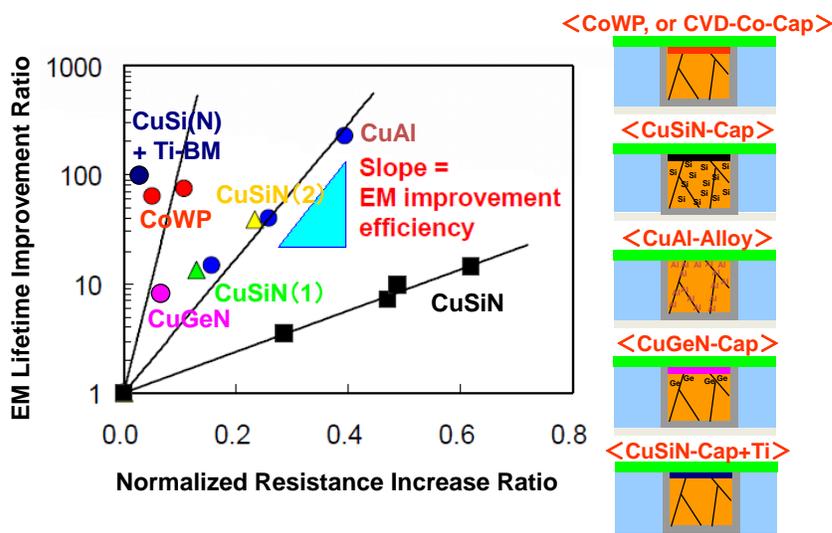


Figure INTC10 Comparison of the Lifetime Improvement versus the Resistivity Increase for Different EM Resistance Booster Technologies [24]

## STRESS MIGRATION

Stress induced voiding (SIV) is the result of vacancy movement driven by stress gradients in and around vias that are connected to different metal layers. According to the literature, SIV can happen both below and in vias. To get voiding below a via, the main vacancy diffusion path is the copper cap interface (and possibly the grain boundary) and a reservoir of vacancies needs to be present in the metal layer under the via [12]. To get voiding in a via, the main diffusion path is the copper barrier interface and a reservoir of vacancies needs to be present in the via itself. The literature attributes voids in vias to non-optimized via processing [13, 14]. A way to eliminate this failure mode is appropriate via to line geometry design with large metal reservoirs prohibited and with linewidth  $\sim$  via diameter.

### 3.1.3 DIELECTRIC RELIABILITY

#### TIME DEPENDENT DIELECTRIC BREAKDOWN

Time dependent dielectric breakdown (TDDB) has rapidly gained wide acceptance as the test method of choice for assessing BEOL dielectric reliability. While a large number of factors and mechanisms have already been identified, the physical understanding is far from complete. The role of the CMP interface on TDDB lifetime was recognized early and analyzed in great detail [1]. Accordingly, plasma treatments were optimized to allow for copper-oxide reduction left after a CMP surface was exposed.

Recently, a quantitative relationship between the amount of copper residue and dielectric reliability using partially patterned damascene wafers was established [15]. It was found that at least  $10^{12}$  atoms/cm<sup>2</sup> of residual copper are necessary for observing a noticeable copper-induced degradation. In these investigations, the degradation itself was not linked to copper migration during the electrical stress, but simply to the presence of a small amount of copper residue before even starting any reliability testing. Other investigations propose a link between copper drift and observed dielectric reliability during operation [3].

Another well documented damascene low- $\kappa$  integration issue relates to the degradation of the inter-metal dielectric during the patterning steps. When CDO, OSG (or SiCO:H) dielectrics are exposed to patterning plasmas, unwanted modifications, such as carbon depletion and the incorporation of silanol groups can occur. While the aforementioned effects have been identified and are being addressed, their interaction and the interrelation of damascene fabrication steps require further efforts. At this stage, the failure is generally attributed more to the integration scheme than to the intrinsic material properties of the dielectrics.

TDDB investigation under dynamic conditions is important, but rarely assessed. On one hand, with changing polarity (AC versus DC [16]) defect relaxation can occur, which results in longer lifetime. On the other hand, a typical interconnect structure is metal-insulator-metal type, where the dielectric defects that are created during stress cannot be

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healed and hence the expected lifetime increase by this effect is small. Interaction of TDDB with other phenomena such as EM, SIV, adhesion stresses, etc. has not yet been properly addressed.

Air-gap integration changes the relevant physics. For air gaps, only interfaces are expected to contribute, hence the reliability margin can be potentially better or worse than that of intermetal dielectrics, depending on the interface quality. For example, some air-gap schemes remove the critical CMP interface contribution.

Besides TDDB, TVS and various V-ramp methods can be used for identification of electrically active components. In general, stress conditions more closely resembling real situations are desirable. Finally, establishing intrinsic reliability specifications and limits is expected to become very important.

### **IMPACT OF LER AND VIA MISALIGNMENT ON DIELECTRIC RELIABILITY**

The electric field between wires is locally enhanced by the presence of LER and misaligned vias (MV). LER originates from lithography and etching of transistor gates and wires. It consists of an irregular side profile of the patterned poly or metal lines, featuring protrusions and notches with nanometer range amplitude. MV in interconnects are due to alignment limitations in patterning steps. In both cases, the field enhancement is caused by two distinct effects, namely the local space reduction between the wires and the increase of density charge in LER protrusions and in the steps formed by misaligned vias. Neither LER nor MV amplitudes scale with wire dimensions. Their relative importance becomes more pronounced with more advanced technology nodes.

LER and MV coexist in wires and the consequent field enhancement is not negligible in narrow lines. For short lines ( $\sim 10\mu\text{m}$ ) with vias, the impact of LER becomes probabilistic; in other words, the shorter the line, the more likely that the impact of MV is predominant. On the other hand, long lines ( $> 10\mu\text{m}$ ) will have the contribution of both MV and the full LER contributions to field enhancement; one of these effects will be predominant according to the relative contribution of these two field enhancement factors in different scaling scenarios [17].

### **3.1.4 RELIABILITY ASSESSMENT, MODELING AND SIMULATION**

TDDB acceleration models are fundamental for describing and predicting dielectric reliability margins at operating conditions. Typical tests are conducted at high electric field and these data are used for predicting lifetime at operating conditions. This often involves extrapolation of the data over several orders of magnitude. This is clearly an area where progress has to be made, because there is no consensus on prediction. As of today, the most conservative E-model is often used for prediction. However, there is significant work [3, 18] showing that the extrapolation to low field is characterized at least by a square root-E dependence. Such equations were derived from conduction mechanisms of electrons as well as from copper drift related phenomena. All acceleration models critically depend on the electric field. There are a number of factors that lead to local field enhancement in interconnects. Intrinsically, porosity introduction into a low- $\kappa$  material is important (electric field enhancement induced by presence of pores) together with line edge roughness which does not scale with materials.

The electric field enhancement caused by LER has an evident impact on TDDB in advanced wire architectures. For long wires, the LER enhancement coexists with the area scaling, thus further reducing the predicted lifetime without LER; accurate TDDB prediction models must take this effect into account [17, 19, 20]. Models should account for these effects as well. Furthermore, there are extrinsic layout and interconnect shape-related field enhancement factors that need to be taken into account, since electric field enhancement locations are expected to be critical. In particular, the layout topology (regular versus irregular) and hence the correspondent application (memory versus logic) determines the presence of specific features (wire corners, turnings in the wires, sloped wires, misaligned vias, local cross-section asymmetry) which need to be modeled. Typically used damascene TDDB test structures are meander-comb, comb-comb, parallel lines or via chains. Length dependence as well as the layout effects need to be characterized in order to relate these to real products. Once the models are known, they can be linked to tools for predicting system level behavior. In that respect, gradual wear-out phenomena are of particular interest, because they cause gradual slowing of the interconnect wiring, which can be addressed at system level, although today's tools fail to incorporate them. To date, the most commonly observed dielectric failures are linked to hard breakdown or abrupt failures. Nonetheless, soft breakdown and gradual wear-out have also been reported in a few cases, which deserve attention [21].

Electron and ionic transport in dielectric materials needs to be understood and described in order to predict current levels. Recently, the defect properties of low- $\kappa$  materials were studied by using photoemission [22, 23]. The defect density from measuring transient currents, after photo excitation was stopped, was also derived— a value of about  $6 \times 10^{16}$  traps/cm<sup>3</sup> was obtained, which is orders of magnitude higher than typical trap densities in silicon dioxide. It is apparent that low- $\kappa$

dielectrics are “intrinsically defective,” when compared to SiO<sub>2</sub>. Yet, the relation of defects to conduction and, in general the identification of electrically active defects still pose a challenge.

### 3.1.5 FUTURE CHALLENGES AND DIRECTIONS

- Description of the temperature and voltage acceleration of the dielectric lifetime, based on a commonly understood and acknowledged physical mechanism.
- Standardization of test methods (test conditions, structures, etc.).
- Setting of dielectric reliability figures of merit, commonly acknowledged by the interconnect community.
- Regular update of reliability understanding and consequent specifications in the roadmap, since materials and integration approaches are changing rapidly. Two examples: ultra low- $\kappa$ , air gaps.
- Identification of electrically active defects, which are responsible for conduction in dielectrics.
- Study of the interaction between different reliability phenomena (e.g., metal/dielectric interaction).
- Study of the cumulative impact of co-existing reliability factors on interconnect lifetime, to be included in the mentioned figure of merit.
- Study and analysis of chip package interactions from the reliability point of view.
- Assessment and prediction of dielectric reliability at system level.
- Reliability with Pb-free and environmentally friendly materials

By adopting state-of-the-art reliability models, together with stress conditions extracted from real applications running on real ICs, it is possible to create a system level time-dependent interconnect reliability analysis framework. It can evaluate the impact of the resistance and delay degradation of wires due to electromigration and TDDB on the system performance. Using such a tool, the designer can predict when reliability degradation mechanisms will start introducing timing violations, which will lead to system malfunction [21].

The limit of this approach is in the need for accurate models of failure modes, which are not available for all reliability issues. At system level, it is also theoretically possible to monitor reliability degradation on real ICs and counteract it by reducing the activity of that part of the circuit in which the degradation is occurring. This approach is possible if the degradation dynamic is slow, and is more independent of accurate models of failure modes. In this respect, the slow breakdown mode is a suitable degradation to be monitored at circuit level and counteracted by reducing the activity of the circuit which shows this type of degradation mode. Intrinsic reliability limits as initial material screening on low- $\kappa$  and ultra low- $\kappa$ . Accurate assessment of intrinsic reliability of low- $\kappa$  materials allows filtering out all the weak candidates which will fail the extrinsic (the materials are integrated in the real wire architecture) reliability criteria anyway.

Obviously, the materials passing the intrinsic reliability tests will have to be screened for extrinsic reliability as well. In general, it is expected that one or more alternate interconnect approaches, such as package-intermediated interconnect, 3D IC, or optical, will begin to be used within the next five years. It appears that carbon nanotube approaches are even further into the future. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

## 3.2 INTERCONNECT PERFORMANCE

### 3.2.1 INTRODUCTION

The adequacy of near-term interconnect technology (copper wires and low- $\kappa$  dielectrics) to continue meeting performance requirements for ICs of next technology generations varies with the intended function of interconnect net and technology used to fabricate Cu wires. As requirements are getting more stringent, it is increasingly necessary that interconnect be considered as part of a system that includes package and silicon chip to satisfy all technology needs for ICs.

The resistivity increase in narrow wires due to electron scattering [1] strongly impacts line resistance and led to a progressive increase of wire aspect ratio in ITRS tables to partially balance R increase, thus causing a slight increase in coupling capacitance between wires, which is the main component of total wire capacitance [2]. This problem is nowadays worsened by the current issues in low- $\kappa$  materials introduction: a) the increase of  $\kappa$  during integration of porous dielectrics with respect to the pristine value, due to processing damages, further exacerbated by dimension scaling (sidewall damage in Cu-low- $\kappa$  trenches) [3]; b) the contribution of integrated low- $\kappa$  materials to the reduction of total wire

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capacitance is becoming less and less important due to the presence of other dielectric materials with higher  $k$  in the wire architecture, such as adhesion layers, etch stop or hard mask layers and dielectric barriers [4].

How these issues, especially a), will limit circuit performance depends on circuit architecture and interconnect networks properties, making a strong collaboration between design and technology worlds mandatory to face the performance challenges of future technology nodes.

### 3.2.2 SIGNAL PROPAGATION

The most critical phenomenon affecting high performance products is delay of interconnects. Generally, wire performance is related to RC product or RC delay. Actually, the critical length of interconnects, below which delay is C dominated and above which delay depends on both R and C, is rapidly decreasing from one node to the other (from a few hundreds of micrometers in 2000 down to a few tens of micrometers in 2010 [5]). However, the interconnect length scaling down in local and intermediate hierarchies has kept RC delay almost constant in the past years. On the other hand, semi-global and global wires represent a real performance bottleneck, since their typical wirelength does not scale, worsening the RC increase issue [6]. In this case, it is necessary to insert repeating inverters in the wires to keep the RC delay within viable limits [7]. This approach requires additional chip area and increases the power consumption.

Crosstalk and noise associated to decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits [8]. These trends are a strong function of design strategy, and should be considered in that context. Crosstalk also induces delay uncertainty increasing the unpredictability of system performance.

The use of advanced patterning techniques alternative to EUV to pursue dimension scaling of local interconnects might further exacerbate RC and cross-talk issues. Double patterning techniques as Litho-Etch Litho-Etch (LELE), might pose new local variability problems [9] other than line-edge roughness. In fact, odd and even LELE wires a) might have different cross-section dimensions due to CD variations between the two separate patterning steps and b) might be not equally spaced at their sides, due to overlay errors in the alignment of the second patterned wire with respect to the first one. Problem a) causes a different RC delay in adjacent wires; problem b) causes a different cross-talk coupling at the 2 sides of the same wire. IC applications based parallel wires for massive signaling (buses) and memory arrays are potentially very sensitive to these wire unbalance issues.

### 3.2.3 POWER CONSUMPTION

Power dissipated in digital IC interconnects is dynamic and depends on the capacitance of the wires as  $\sim \alpha \cdot C_{int} \cdot V^2 \cdot f$  for a wire, where  $f$  is the frequency of digital signal,  $\alpha$  is wire activity factor,  $V$  stands for voltage swing between the two digital levels, and  $C_{int}$  is total interconnect capacitance of a certain wire length [9]. Dynamic power is directly impacted by wiring capacitance and can be minimized most efficiently by reducing  $V$ . Interconnect power is strongly influenced by capacitive coupling in the most dense hierarchy levels, at local and intermediate levels, thus creating a highly sensitive issue for low power applications.

In addition to the problems with scaled wires for clock and signaling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to the decreasing supply voltage  $V$ , causes an increased voltage drop between the power supply and the bias point for fixed length wires. This issue is made critical by the resistance increase due to conductive section reduction and  $Cu$  resistivity increase. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires.

### 3.2.4 SYSTEM-LEVEL PERFORMANCE

Evaluation of IC performance requires dedicated modeling and simulation tools including accurate technology modeling and system level considerations. Technology modeling should incorporate the additional variability effects in local interconnects caused by double-patterning issues, mentioned in the signal propagation section of this chapter. The impact of these effects on circuit speed and energy should be evaluated starting from the characterization of the cell library, where local interconnects are mostly used. At system level, critical paths are generally dictating performance of an IC system. These paths have to be carefully simulated taking into account the entire link made of transmitter circuit, interconnect and receiver, each element with its own electrical characteristics as input/output resistance and capacitance. Interconnect RC delay is not sufficient to evaluate performance of a critical path accurately, especially considering current return path and its impact on parasitic inductance [10]. High frequency behaviour might also be needed to be taken into account if the signals propagating through the wires have stringent requirements in terms of high frequency contents and limited distortion.

Alternative solutions at system design level are based on modular architectures to reduce the need for fixed length lines. One recent approach in this direction is the dual- or multi-core architecture in state-of-the-art microprocessors. Parallel data processing in the multi-cores allows comparable or even higher processor performance at lower core frequencies and reduced power consumption as compared to a single core high performance processor. Multi-core strategy allows to

reduce the interconnect length, and consequently  $C_{int}$ , frequency  $f$  due to the exploitation of parallelism of multiple cores in executing certain tasks, and supply voltage  $V$ , since a lower operating frequency requires lower  $V$ , thus reducing dynamic power consumption. The development of multicore architectures underline the need for a new kind of interconnects with high bandwidth (i.e. low  $C$ ) to support inter-core communication through a chip level network on chip. However, such significant modifications to circuit architecture suffer from the disadvantages of needing new design tools and new software and are not generally applicable to all designs. Revolutionary solutions include different interconnect concepts such as optical interconnects.

*Table INTC9 Surface Preparation Interconnect Technology Requirements*

## 4 PROCESS MODULES

### 4.1 DIELECTRIC POTENTIAL SOLUTIONS

Damascene has been the dominant process scheme for fabricating Cu interconnect structures. In particular, dual damascene, in which there are fewer metallization and planarization steps than in single damascene, has generally been used since 1997. Following the adoption of Cu as the conductor, intensive research and development efforts have been carried out to minimize wire capacitance by incorporating dielectrics with lower dielectric constants ( $\kappa$ ) than conventional oxides. The pace of incorporating advanced low- $\kappa$  materials has been slowing down as compared to the earlier ITRS projections because of difficulties in manufacturing, including cost, and reliability.

Low- $\kappa$  materials have been targeted mainly for use as intra/inter-layer dielectrics (ILD). But the influence of other dielectric layers, typically having higher  $\kappa$  values, on the effective  $\kappa$  has been growing. The effective  $\kappa$  value does not decrease in proportion to the decrease in the bulk  $\kappa$  value. Moreover, thinning of relatively high- $\kappa$  layers tends to be more challenging than conventional ILD since the layers are already as thin as possible. In the Passive Devices Appendix, Figures A1 and A2 show cross-sections of interconnect structures and the corresponding effective  $\kappa$  values. Historically, the highest- $\kappa$  layers are Cu diffusion barriers. There have been high- $\kappa$  materials at the top of the ILD to protect the porous low- $\kappa$  ILD from the damage during CMP and plasma deposition, but they will be sacrificial with implementation of air-gap features. Reduction of thicknesses and bulk- $\kappa$  values of diffusion barriers will be most important for decreasing RC delay. In addition to the improvement in capacitance reduction, diffusion barrier deposition pre-treatment has been investigated as a means of obtaining higher reliabilities. Scaling down the metal/hole-size and -spacing degrades electromigration (EM) and time-dependent dielectric breakdown (TDDB), respectively. The interfaces just below the diffusion barriers will require improved adhesion, fewer defects, less damage, etc.

Reduction of the ILD  $\kappa$  value is slowing down because of problems with manufacturability. The poor mechanical strength and adhesion properties of lower- $\kappa$  materials are obstructing their incorporation. Delamination and damage during CMP are major problems at early stages of development, but for mass production, the hardness and adhesion properties needed to sustain the stress imposed during assembly and packaging must also be achieved. The difficulties associated with the integration of highly porous ultra-low- $\kappa$  ( $\kappa \leq 2$ ) materials are becoming clearer, and air-gap technologies are likely to be introduced earlier than projected in the previous editions of the ITRS.

Due to the increase in the development costs of process design kits, once a process technology is established, only relatively minor changes are made in the course of its improvement. In the future, new materials are expected to be introduced only when migrating to a new technology. The bulk  $\kappa$  values of ILD layers and the  $\kappa_{eff}$  roadmaps for MPUs, Flash and DRAM are shown in *Table INTC2-Table INTC4* respectively. The slowdown in the decrease of  $\kappa$ -values since the 2007 edition of the ITRS was partly reflected in the 2008 update. In this edition, the trend is further reflected by delaying low- $\kappa$  progress by one year with narrower range of bulk low- $\kappa$  materials in light of the actual pace of deployment of new technologies (Figure INTC11).

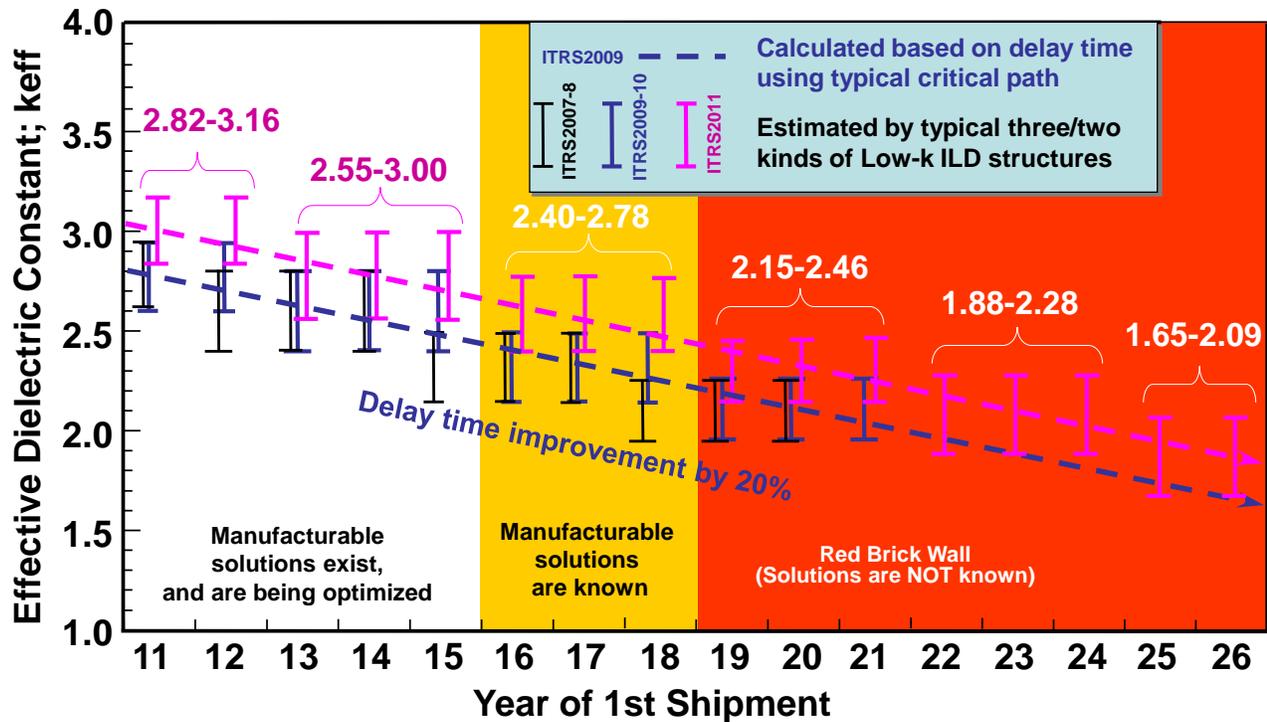


Figure INTC11 Low- $\kappa$  Roadmap Progression

#### 4.1.1 PRE-METAL DIELECTRIC (PMD)

The pre-metal dielectric (PMD) potential solutions chart (Figure INTC13) has been significantly updated. PSG (Phosphorous-doped spin-on glass) and BPSG (Boron-doped PSG) were deleted from the solutions because they are no longer used for gettering of heavy metals. Low- $\kappa$  OSG, MSQ, and HSQ were also deleted because the high- $\kappa$  stress liner (SiN), used for improving mobility of MOSFETs, dominates the capacitance at the PMD level.

While the requirement for the reduction of  $\kappa$  value has been dropped, the need for filling ability is becoming more critical. To fabricate small contact holes uniformly, the space between the side-walls of transistors must be filled without any voids. Combination of conventional and conformal deposition techniques is a possible way to achieve both fine-pitch filling and low cost. Thermal and plasma-assisted CVD SiO<sub>2</sub> and its planarization process will be used continuously because of their low cost, efficiency, and reliability. Two-dimensional miniaturization is no longer a sufficient, nor the most effective means to increase the capacity of memories, and consequently three-dimensionally stacked memory cell structures have been reported for NAND Flash [1, 2]. In these devices, the gate electrode of a memory cell has a stepped structure, and very large steps are formed between the memory cell area and its periphery during fabrication. The stepped surface thus formed must be filled with an insulator, without leaving voids, and a contact hole must be made for each gate electrode. For this process, spin-on dielectrics (SOD) might be used because of their superior gap filling capability versus conventional CVD materials. In this case, the spin-on conditions required for filling a relatively large area with challenging topography must be investigated. The SOD must also be amenable to planarization by CMP. A new class of carbon free flowable CVD film has recently made their appearance, renewing interest in CVD based gap-fill technologies.

#### 4.1.2 CONVENTIONAL LOW-K ILD

The primary conductor material changed from Al to Cu, and the damascene process became the dominant process for interconnect fabrication. The damascene process does not require dielectrics of high gap-filling capability because it is Cu that fills trenches and/or holes in the dielectrics. PECVD-SiO<sub>2</sub>, which has lower gap-filling capability than HDP-SiO<sub>2</sub>, has been used as an ILD material since the dawn of Cu interconnects. For the top few metal layers, used mainly for power/ground lines, attaining high mechanical strength to avoid cracking and/or delamination during assembly and

packaging processes is more important than capacitance reduction. Given its cost effectiveness, PECVD-SiO<sub>2</sub> will continue to be used for thick layers.

For the bottom few metal layers with thin wires, reduction of  $\kappa_{\text{eff}}$  is still critical. Many low- $\kappa$  materials have been studied for use as inter/intra-layer dielectrics in order to decrease the interconnect capacitance. There are still difficulties in low- $\kappa$  material integration caused by their poor mechanical and chemical strength. Further improvement of their material properties, as well as design and structural changes, will be required for the integration of highly porous ILDs.

Spin-on dielectrics have the benefit of less dependence on precursors than CVD, that is, one tool can handle a variety of materials, including porogen. Various spin-on low- $\kappa$  materials including porous materials have been studied. However, PECVD-SiCOH has been the dominant low- $\kappa$  ILD film. Non-porous spin-on materials have not been used except in some special cases. Spin-on polymer and spin-on MSQ with  $\kappa \geq 2.4$  are unlikely to be used for logic/memory devices, consequently spin-on materials except porous-MSQ have been deleted from the dielectric potential solutions figure (See Figure INTC13).

In order to decrease  $\kappa_{\text{eff}}$  by adopting increasingly porous low- $\kappa$  ILD materials, challenges in integration processes such as etching, CMP, and deposition on porous ILD layers must be tackled. Photolithography for porous ILD usually requires a dense layer to ensure a uniform resist coating and to prevent damage during resist strip. The layer can also act as a stopper during metal-CMP. SiO<sub>2</sub> has been widely used as a “hardmask” layer; however, low- $\kappa$  ILD is damaged by active oxygen in the initial stages of the hardmask deposition. The hardmask and damaged layers must be removed in order to decrease the capacitance, especially in intra-layers. Those layers should be removed during CMP after the barrier metal is cleared up in order to minimize process steps. However, it also exposes the porous low- $\kappa$  material to CMP conditions. For ultra-low- $\kappa$  ILD ( $\kappa \leq 2.3$ ) minimal dielectric constant increase due to damage from CMP slurries and cleans is key for successful low- $\kappa_{\text{eff}}$  interconnects.

Dry etching and resist removal for trench or via formation also damages low- $\kappa$  ILD. To minimize damage from strip, Via first tri-layer schemes have been replaced with trench first TiN HM based dual damascene fabrication. In order to minimize damage done by active species, “closed-pore” porous low- $\kappa$  materials are actively being researched. For ULK films ( $\kappa < 2.3$ ), all damage scenarios get amplified, and the need to have packaging compatibility (i.e. high mechanical strength) limits the degrees of freedom to develop a damage resistant ULK. Thus,  $\kappa$  recovery with low  $\kappa$  repair techniques is becoming increasingly important to be able to integrate bulk films with  $\kappa \leq 2.3$  with packaging integrity. The development of ultra-low- $\kappa$  ILD ( $\kappa < 2.3$ ) that aid in damage recovery through low  $\kappa$  repair with acceptable mechanical strength will become increasingly important in meeting harsh performance demands.

Formation of porous or ultra-porous low- $\kappa$  films requires appropriate cure technologies such as complete decomposition and evaporation of porogen and chemical-bond bridging that gives higher mechanical strength. UV and e-beam assistance has commonly been used in low temperature cure processes, but their cost effectiveness and effects on underlying layers invite serious consideration when applied to multiple thin interconnect layers. With the assistance of cure processes, spin-on materials will be a realistic solution for ultra-low- $\kappa$  ILD. However, PECVD has the advantage of easier integration of the cure system into a cluster tool. PECVD followed by UV cure is now the predominant choice for  $\kappa \geq 2.2$  low  $\kappa$  film deposition.

In spite of the tremendous efforts being made, a broad consensus is forming that  $\kappa_{\text{eff}}$  cannot be lowered much further by reducing the bulk  $\kappa$  value of ILD, once it has reached 2.0, due to mechanical integrity and plasma damage problems with porous low- $\kappa$  materials. Ultra low- $\kappa$  materials with  $\kappa < 2.0$  are discussed in the *Emerging Research Materials* chapter. A different, architectural (as opposed to material) approach to lowering  $\kappa_{\text{eff}}$  is to introduce air-gaps (described below) into ILD layers.

### 4.1.3 AIR GAPS

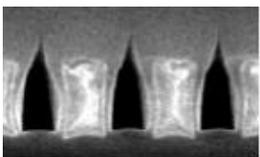
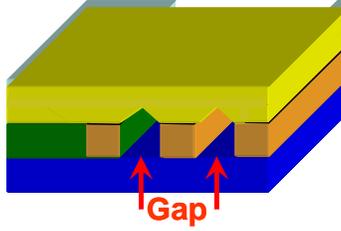
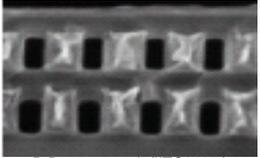
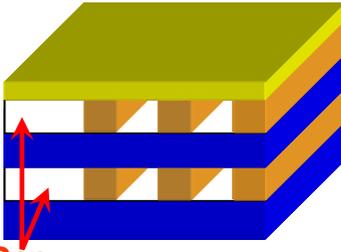
Porous low- $\kappa$  materials have poor mechanical integrity and sustain significant damage from plasma etching. Integration of porous low- $\kappa$  materials with  $\kappa \leq 2.0$  is deemed to be extremely difficult. A gradual transition from ultra low- $\kappa$  materials to air-gaps is now considered a real possibility. A hybrid of low- $\kappa$  materials and air-gaps will be the most realistic solution to lowering  $\kappa_{\text{eff}}$  in the foreseeable future.

Introducing air-gap structures into interconnects will be one of the most significant challenges for semiconductor device fabrication in the coming decade. Several integration schemes and structures for air-gap formation have been reported and the most likely are shown in Figure INTC12. They can be classified into two categories according to whether gap formation is performed before or after the upper metal formation. In order to integrate air-gaps into Cu damascene

structures, sacrificial materials located between metal lines must be removed because Cu-CMP should be carried out under non-gapped conditions.

In integration schemes in which gap formation is performed before the upper metal is formed, the sacrificial parts are removed after CMP, and then air-gaps are formed by dielectric deposition with low filling capability[9, 10]. The removed parts consist mostly of the sacrificial material. The gap shape is defined by the spacing between and aspect ratio of metal lines along with deposition conformality. In most cases of gap formation during inter-layer dielectric deposition, air-gaps are formed in regions having a narrow line-to-line spacing, but the dielectric is also deposited in regions having a wider spacing. This gives different total ILD thicknesses in dense and sparse regions and necessitates a planarization process. Another process flow in this category uses the damage done by dry etching to the sides of trenches. Uniform gaps are formed during the subsequent wet treatment for any line-to-line spacing selectively in damaged regions. The gap formation before upper metal formation creates a serious alignment challenge for fine-pitched interconnects. Misaligned vias do not sit exactly on a metal line. If a via opening connects to an air-gap region, appropriate barrier metal deposition and Cu filling cannot be carried out. Exclusion of regions around upper vias from air-gap formation has been presented, but it is accomplished at the cost of more process steps, including an additional lithography step.

In the integration schemes in which air gaps are formed after the upper metal layer is constructed, there is no misalignment problem because via holes are filled with metal before gap formation[11-13]. Removing the sacrificial parts of multiple layers may be desirable for minimizing the number of process steps. The removal process applied in this scheme produces large gaps, which degrade the mechanical strength of the whole chip. Ceaseless efforts will be needed to develop air-gap structures with sufficient mechanical strength and can be formed with minimal process steps.

Process	Schematic	(Dis)advantages	
<p><b>CVD gap process</b></p>  <p>T.Harada et al. (IITC2006)</p>	 <p>Gap</p>	<p><b>Process step increase</b></p>	<p><b>Additional lithography and removal process steps for each wire level</b></p>
<p><b>Gap formation by removing sacrificial material</b></p>  <p>R.Daamen et al. (IITC2007)</p>	 <p>Gap</p>	<p><b>Process step increase</b></p>	<p><b>Minimal process step increase by all-in-one post-removing process</b></p>
		<p><b>Mechanical strength</b></p>	<p><b>Air-gap region can be defined by lithography</b></p>
		<p><b>Borderless capability</b></p>	<p><b>No Cu-filling capability due to via to under-metal misalignment</b></p>
		<p><b>Process step increase</b></p>	<p><b>Minimal process step increase by all-in-one post-removing process</b></p>
		<p><b>Mechanical strength</b></p>	<p><b>Poor mechanical strength by air-gap formation in a whole wafer</b></p>
		<p><b>Borderless capability</b></p>	<p><b>Not sensitive to via to under-metal misalignment</b></p>

**A realistic air-gap formation process should be proposed with minimal process step increase, maintained mechanical strength and sufficient borderless-via capability.**

Figure INTC12 Typical Air-Gap Integration Schemes

#### 4.1.4 DIFFUSION BARRIER DIELECTRIC

Dielectrics for diffusion barriers typically have the highest  $\kappa$  values in conventional Cu interconnect structures. In a conventional Cu damascene process flow, the bottom and sides of Cu lines are covered by barrier metal, which is deposited before the Cu seed layer. Only the top of the Cu lines is covered by the diffusion barrier dielectric after CMP. Diffusion barriers must be free of pinhole defects and function as etch stop layers during via formation. These layers were referred to as the “via etch stop layers” in the 2007 edition of the Interconnect chapter.

Silicon nitride (SiN), whose  $\kappa$  value is over 6, was adopted as a diffusion barrier dielectric at the inception of Cu interconnects with PECVD-SiO<sub>2</sub> ILD. Since low- $\kappa$  ILD materials were introduced, SiC, SiCN, or SiCO [3], whose  $\kappa$  value is between 4 and 5 have been used as diffusion barrier dielectrics in order to decrease  $\kappa_{\text{eff}}$ . However, these lower  $\kappa$  (<5.0) dielectric barriers have scaling issues due to stress and leakage challenges on UV exposure required to cure low  $\kappa$  films ( $\kappa < 3.0$ ). As the ILD layers become thinner, the relative contribution of the diffusion barrier  $\kappa$  to  $\kappa_{\text{eff}}$  is growing. While alternative lower- $\kappa$  diffusion barriers have not been used to date, thinning of diffusion barriers and  $\kappa$  reduction are critically required without reliability degradation.

The metal-capping process, in which a metal barrier is grown selectively on Cu lines, offers the possibility of omitting the insertion of a diffusion barrier between the low- $\kappa$  ILD and the Cu lines. Because of the imperfect selectivity of existing metal capping processes, both capping metal and thin diffusion barrier dielectric can coexist in a transitional stage, but such redundant combinations should ultimately be avoided to reduce process costs. However, a selective metal cap that is also a diffusion barrier has not materialized and needs to be an active area of research.

#### 4.1.5 CAPPING BARRIER DIELECTRIC

The interface between a diffusion barrier and the top of a Cu line has a direct impact on the reliability of damascene Cu interconnects [4]. Minimum spacing between metals usually appears at such interfaces by misalignment of vias with Cu lines. Time-dependent dielectric breakdown (TDDB) lifetime and electromigration reliability are strongly affected by the cleanliness of the interfaces. Dominant electromigration paths usually run along the interfaces of Cu lines, which are not covered with barrier metal. The requirement for fine interface formation will become more stringent as the metal width and spacing become narrower; EM and TDDB lifetimes will also be shortened.

Metal capping using Electroless CoWP has been shown to give longer EM lifetimes compared with the conventional structure with a dielectric barrier on Cu. The capping metal, selectively grown on Cu lines, produces a strong metal connection between the wires and the via bottoms. Capping metal growth must be carried out with near perfect selectivity on fine-pitched Cu lines to prevent leakage and TDDB. The selectivity is improved by pre and post cleaning, but, this adds cost, and manufacturability concerns as the cleaning process itself also has a selectivity problem. Improvement of the EM lifetime by the use of Cu-alloy seed and/or by barrier metal optimization is also being studied. Several metal materials are considered but tend to increase the resistance of Cu lines. Continuous research and development are needed to find feasible and cost effective solutions.

Another process that gives better interface characteristics is pre-treatment of the Cu before the deposition of the dielectric diffusion barrier. *In-situ* CuSiN formation using silane and ammonia plasma, in the same apparatus as that used for the dielectric barrier deposition, gives a longer EM lifetime without TDDB degradation [5]. The resistance of the Cu wires depends on the silicon diffusion condition, so the exposure to silicon and nitridation must be carefully controlled. Recently, CuGeN formation using germane instead of silane was reported [6]. The resistivity of CuGeN is more controllable than CuSiN. Silane/germane sources, combined with ammonia, are suitable for mass production. But there will be possibilities for other powerful treatment processes with different materials. The recently proposed pre-treatment for preventing Cu migration by impurity metal doping is also a potential solution to high-reliability interface formation [7]. A different approach was recently reported where a selective Co cap deposited by CVD demonstrated a 30X improvement in electromigration without TDDB or resistance degradation [8]. A good capping scheme needs to provide the required EM performance improvement with minimal impact on RC (<5%), equivalent TDDB reliability and manufacturability at low additional cost.

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
<b>PRE-METAL DIELECTRIC (PMD)</b>																
HDP silicon dioxide ( $\kappa = 4.2$ )	[Continuous Improvement]															
SA CVD ( $\kappa = 4.5$ )	[Continuous Improvement]															
<b>INTER/INTRA LAYER DIELECTRIC (ILD)</b>																
PECVD silicon oxide ( $\kappa \sim 4$ )	[Continuous Improvement]															
PECVD SiCOH ( $2.8 \leq \kappa \leq 3.2$ )	[Continuous Improvement]															
PECVD porous SiCOH ( $2.4 \leq \kappa \leq 2.7$ )	[Continuous Improvement]															
PECVD ultra-porous SiCOH ( $2.0 \leq \kappa \leq 2.3$ )	[Research Required]		[Continuous Improvement]													
Spin-on porous MSQ ( $2.0 \leq \kappa \leq 2.3$ )	[Research Required]		[Continuous Improvement]													
Alternative air-gap ( $\kappa \leq 2.0$ )	[Research Required]		[Continuous Improvement]													
<b>DIFFUSION BARRIER DIELECTRIC</b>																
CVD silicon carbide ( $\kappa > 3.5$ )	[Continuous Improvement]															
CVD silicon carbide ( $\kappa \leq 3.5$ )	[Continuous Improvement]															
PECVD SiCOH ( $\kappa \leq 3.5$ )	[Continuous Improvement]															
Spin-on porous MSQ ( $2.4 \leq \kappa \leq 2.7$ )	[Research Required]				[Continuous Improvement]											
<b>CAPPING BARRIER DIELECTRIC</b>																
CuSiN or CuGeN	[Continuous Improvement]															
Alternative treatment on Cu before diffusion barrier deposition	[Research Required]				[Continuous Improvement]											

*This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.*

Research Required   
 Development Underway   
 Qualification / Pre-Production   
 Continuous Improvement 

Figure INTC13 Dielectric Potential Solutions

## 4.2 BARRIER POTENTIAL SOLUTIONS

Ti/TiN films [1] will continue to be used as barriers for tungsten local wiring, which is sometimes called metal zero, and for contact fill in the near term. Established deposition techniques such as ionized PVD, long throw PVD, along with CVD are being enhanced to improve compatibility with key-hole free W used for high aspect ratio DRAM contacts. Development of ALD Ti/TiN is underway and is likely to improve the overall W fill process by improving barrier conformality and reducing the top of contact “pinch-off” that leads to difficulty in W filling. Even with improvements, the Ti/TiN barrier is expected to be a significant contributor to future contact plug resistivity because of film thickness requirements and high resistivity. Development of alternative ALD barriers for W contact plugs, such as WN [2, 3], is underway and it appears that barrier resistivity and thickness can both be reduced versus Ti/TiN. In this case, the barrier contribution to overall contact plug resistance can be reduced.

Research is also underway to explore alternate materials and fill techniques for high aspect ratio contact structures which would allow simplification of the current contact/barrier/conductor film stack. Since one of the primary functions of the TiN or WN barrier is to prevent interaction of Ti with F from the  $WF_6$  precursor, a change to non-fluorine containing tungsten precursors could allow for elimination of the barrier film entirely. Serious consideration is also being given to the use of Cu to replace W in contact studs. In this case, the standard PVD TaN/Ta [4], Ti [5], Ru or ALD Cu barrier alternatives would be used.

Cu wiring barrier materials must prevent Cu diffusion into the adjacent dielectric but also must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta [4] has become the predominant industry solution but other nitrides and silicon nitrides have also shown promise. Ionized PVD, and CVD deposition continue to be improved (while long throw transitions to a legacy status), enabling them to meet the challenging sidewall coverage requirements of future dual damascene structures. In fact, it appears that improvements in ionized PVD technology [6] will continue to be used toward 14 nm. In addition, since the critical dimensions and aspect ratios for the upper global wiring levels for logic products remain relatively unchanged for future technology generations, they will continue to be compatible with PVD barrier technology. However, even these advanced PVD deposition techniques tend to narrow the upper part of the dual damascene trench and limit the fill capability of the ECD Cu process.

A great deal of effort is underway to develop ALD [7-10] barriers which are expected to become the predominant future solution for copper. ALD TaN and WNC (carbide) are further along in development but questions remain concerning their interface properties with Cu and whether adequate electromigration performance can be ensured. One potential solution to this issue is a PVD Ta flash layer followed by PVD Cu to provide the required interface to ECD Cu. ALD Ru appears to be compatible with direct plating of ECD Cu and also provides a good Cu interface, however, its barrier properties are suspect. Two advanced potential solutions are ALD TaN/ALD Ru and ALD WNC/ALD Ru bi-layer barriers. One major obstacle to the adoption of ALD for barriers is penetration of the precursor materials into the porous low- $\kappa$  dielectrics targeted for future technology generations. *In situ* modification of the etched low- $\kappa$  sidewalls may be used either with ALD or as a stand alone barrier to resolve this issue. The other major obstacle regarding adoption of ALD barriers is low throughput. This results in a significant increase in factory floor space and cost of ownership for ALD barrier/seed technology versus PVD barrier/seed solutions.

One promising area of development for Cu wiring technology is self-forming barriers, specifically Cu-Mn alloys [11]. This process eliminates the PVD barrier and instead utilizes a PVD Cu-Mn alloy seed layer. After ECP Cu deposition, an anneal causes the Mn to diffuse to the Cu surface and form a thin barrier. The Mn at the top surface of the annealed Cu is removed by the subsequent CMP operation. Another advantage of this process is that the Mn does not form a barrier in the underlying via region, resulting in a Cu-Cu via interface with very low via resistance.

Another focus area for metal barriers is the Cu top interface. PECVD dielectric Cu barriers such as  $Si_3N_4$ , SiCN, and SiC are predominately used for this application. Disadvantages are degraded Cu electromigration properties and a rise in the overall  $\kappa_{eff}$  of the structure because of their higher  $\kappa$  values. For improving in Cu electromigration properties, some of the selective metal capping barriers such as W [12], CoWP [13], NiMoP [14], CVD Co [15], or CVD Ru [16] have been explored and employed on the manufacturing process. The other major candidate for a capping process is formation of a CuSiN layer at the top Cu surface [17]. This is accomplished by sequential exposure of the surface to  $SiH_4$  and  $NH_3$ . While the degree of electromigration improvement is not as large as with CoWP, there is also a much decreased risk of reliability issues due to metal shorts or leakage.

A great deal of research and development in the area of advanced barrier materials and deposition techniques is needed, since engineering the smoothness and other properties, such as the lattice mismatch between the barrier and the Cu interface, may help to ameliorate the expected Cu resistivity increase from electron scattering effects. Practical approaches to simultaneously suppressing electromigration and resistivity increases are essential.

32 Interconnect

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
<b>Metal 0/Contact plug Barrier</b> Ti/TiN, WN,... barriers for CVD W																
TaN/Ta, Ta, Ti, Stacked Ru... barriers for alternative conductors																
<b>Metal 1, Intermediate wiring Barrier</b> ionized PVD TaN/Ta, Ta																
TaN, TiN,Ti, WNC...(CVD, ALD)																
Self formed/restored barriers: MnSiO, MnTaO etc																
<b>Capping</b> E-less CoWP																
Selective CVD metal (Co, Ru, W...)																
<b>Semi-Global/Global Barrier</b> TaN, TiN, ... (ionized PVD)																

**This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.**

Research Required

Development Underway

Qualification / Pre-Production

Continuous Improvement



Figure INTC14 Barrier Potential Solutions

### 4.3 NUCLEATION POTENTIAL SOLUTIONS

The conformality and coverage of the nucleation layer is often the critical factor in determining whether the subsequent conductor deposition will be free of voids. Figure INTC15 shows the current and future nucleation potential Solutions. For local wiring and contact fill, there will be continued improvement in ALD W nucleation layers which have been used to enable high aspect ratio W fill. These ALD nucleation layers are usually extremely thin so that the overall conductivity of the plug is generally improved.

The alternatives to W as a contact plug include ECD Cu. The potential nucleation layers for Cu are discussed below while Ru [1], Co by CVD or ALD have been proposed for nucleation layers [2]. Development is still underway for alternative materials and processes for high aspect ratio DRAM contacts, but ALD nucleation layers will likely be needed for this technology. For Metal 1, intermediate and global wiring, enhanced PVD Cu [3] deposited through various ionized techniques, occasionally combined with long throw, continues to be the dominant nucleation layer for ECD Cu. Improvement has been made in the sidewall coverage and uniformity of these layers, which will allow their use toward the tightest dimensions of 14 nm technology. In addition, PVD Cu nucleation layers will continue to be used on the global wiring levels with larger critical dimensions. Eventually, these enhanced PVD techniques will not be able to provide reliable nucleation layers at the M1 and intermediate wiring levels and will be replaced by ALD technology, which includes obtaining Cu by hydrogen reduction. Several nucleation layer options, including electroless [4], ALD, and electrografted Cu technology [5], continue to be researched. Although ALD Ru [6] seems to be only a marginal barrier to Cu diffusion, it does appear to be a very good nucleation layer for ECD Cu. Therefore, it may be used in conjunction with other barriers, such as either ALD TaN or ALD WNC. Another potential solution to the problem of marginal PVD Cu sidewall coverage is repair of the nucleation layer [7] through ECD techniques. A more elegant solution involves modification of the ECD process and/or barrier to self-nucleation, thereby eliminating the need for a Cu nucleation layer.

34 Interconnect

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
<b>Metal 0/Contact plug</b>																
<b>Liner/Nucleation</b>																
CVD W reduced by B2H6																
E-less or plated Cu seed																
ALD/CVD Ru, Co for Cu plug																
<b>Metal 1, Intermediate wiring</b>																
<b>Seed/Liner/Nucleation</b>																
Enhanced PVD Cu																
E-less or plated Cu seed																
CVD(ALD)-Co, Ru for Cu-wettability improvement or direct plating																
CVD or ALD Cu seed																

**This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.**

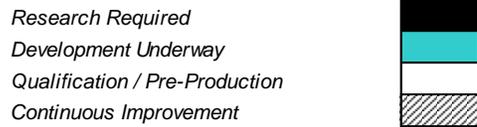


Figure INTC15 Nucleation Potential Solutions

#### 4.4 CONDUCTOR POTENTIAL SOLUTIONS

Local wiring is limited to very short lengths and usually contacts adjacent transistors. Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, MPU/ASICs, Flash, and DRAM devices. ALD, in conjunction with CVD techniques, is being utilized first in the W deposition area. There has been a problem associated with the standard silane nucleation step in the CVD W process in that this Si-rich film takes up an ever-larger portion of the plug and will result in unacceptably high resistance for future technology generations. Modification of the process to minimize or eliminate this layer is an area of focus. Alternative materials and processes such as electroplated Rh [1] and electroplated Cu [2] which exhibit superfilling behavior are also being investigated as a replacement for W contact plugs. Continued development of ALD tungsten deposition has been examined to accomplish W fill of high aspect ratio contacts for stacked capacitor DRAM designs. Alternate materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts.

Cu will be the preferred solution for the Metal 1 and intermediate wiring levels in MPUs and ASICs and ECD continue to dominate the market in the near term [3-5]. There will be continuous improvement in plating chemistry and ECD tool design to allow seamless fill of smaller geometry, higher A/R structures. CVD technology is also needed for minimum feature sizes [6]. It has been reported that even with the normal Cu overburden, there is ever increasing difficulty in transforming ECD Cu in minimum feature size damascene wires into the large-grain bamboo structures desired for good electromigration performance. As a consequence, Cu grain boundaries, as well as surface diffusion, must both be considered as potential failure modes for electromigration in the future. One potential solution to improving electromigration lifetime of the Cu conductor is through the use of Cu alloys such as Cu-Al [7], or Cu-Ti [8]. The alloying element is introduced through the use of PVD Cu alloy seed layers and then diffused through the entire conductor with a post-plating anneal. As one example of this, the use of this Cu-Al alloy along with an optimized Cu to dielectric cap interface resulted in a 50× improvement in electromigration lifetime. One downside to the use of alloying elements is an increase in resistivity when compared to the pure conductor.

Minimum feature size M1 and intermediate Cu wiring, in MPUs and ASICs, has already experienced a resistivity increase due to electron scattering [9-11]. The line lengths of these wiring levels tend to scale with technology generation so the impact on performance has been minimal. Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. The resistivity of the smallest pitch global wiring level is expected to increase about 40% by the end of this decade. This is more problematic, since global wiring traverses longer lengths and is more likely to impact performance than M1 and intermediate wiring. Cu interfaces, microstructures, and impurity levels will need to be engineered to alleviate the impact of this resistivity rise.

MPUs use a hierarchical wiring approach in which the pitch and thickness of the global wires are increased at each level. Indeed, the final global wiring level is little changed from one generation to the next and so will not be affected by electron scattering effects. In the 2011 table, the global wiring pitch will be estimated to be constant because significant changes are not expected. The resistivity of metals is a function of temperature and therefore cooling of IC chips is one potential solution to improved wire conductivity. However, this is probably not practical for most consumer and portable devices so it is likely that aluminum will continue to be used for global wiring and enhanced CVD/PVD flow techniques [12] will continue to be improved for damascene architectures.

Other design alternatives are the use of repeaters or oversized drivers, both of which impact chip size and power. The most likely near-term solution is the use of very high density TSVs as an enabling technology for three-dimensional chip stacking. This technology can reduce overall interconnect wire lengths while allowing incorporation of non-Si solutions for improved functional diversity. The other near-term solutions are judicious use of design and signaling options and packaging to minimize the effect of the narrower more resistive global wires. A great deal of research is underway on the use of either RF or optical techniques to resolve this issue. More radical solutions include superconductors, carbon nanotubes, etc. A full discussion of 3D IC, a proposed roadmap for high density TSV and other alternatives is contained in a TSV related section.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of MIM capacitors to improve yield and reliability. Both Al and Cu are in use for standard spiral inductors, but various magnetic materials may emerge with different inductor designs to reduce the area of these devices.

36 Interconnect

First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
<b>Metal 0/Contact plug</b>	CVD W															
	ECD Cu, Rh, ...															
	Barrier less conductor															
<b>Metal 1, Intermediate wiring</b>	ECD Cu															
	Alloy additions to Cu for reliability improvements (CuAl, CuMn, CuTi)															
	PVD Cu reflow															
	Alternative materials with weaker size effect (W, Mo, Ru ...)															
	CVD Cu															
<b>Semi-Global/Global Conductor</b>	ECD Cu															
	PVD(reflow) or CVD Al															

**This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.**

- Research Required
- Development Underway
- Qualification / Pre-Production
- Continuous Improvement



Figure INTC16 Conductor Potential Solutions

## 4.5 ETCH / STRIP / CLEAN POTENTIAL SOLUTIONS

### 4.5.1 INTRODUCTION

Beyond the 20nm technology node, porous low- $\kappa$  dielectric with  $\kappa$  value below 2.3 will be required to reduce RC delay for Cu interconnects. In order to achieve effective integrated k-value ( $\kappa_{\text{eff}} < 2.5$ , for advanced technology nodes [1], lower k-value assist layers will need to be integrated. Bulk low- $\kappa$  materials with  $\kappa < 2.3$  alone will not be able to fulfill the requirements even when thinning currently used silicon oxy-carbide - based assist materials.

Process unit integration affects the final  $\kappa_{\text{eff}}$  value. Etching and ashing processes are the worst processes for inducing damage to the low- $\kappa$  material, degrading electrical reliability and increasing defectivity. Wet cleaning process also affects the electrical performances by consuming part of the damaged dielectric. Foremost among process integration considerations for ULK patterning is profile control. Controlling the profile taper and roughness with minimal low- $\kappa$  damage will be a key to maintaining a useful  $\kappa_{\text{eff}}$  value.

Profile control: The control of critical dimensions (CD), width and depth, are directly linked to the integration strategy and the etching chemistry process. Straight profiles are generally desired but there is always a compromise between a more tapered profile versus a more bowed profile. The tradeoff has implications for the effective metal filling of narrow dimension trenches with PVD or CVD. Additionally, reliability considerations must be included into the integration scheme.

Change of dielectric properties: Plasma induced damage of low- $\kappa$  leads to an increase in k value and a degradation of the electrical properties. Increased moisture uptake and enhanced species diffusion through the dielectric pore network is believed to be the fundamental cause. In addition, the low- $\kappa$  material properties can also be negatively impacted through the diffusion of metallic barrier precursors into pores of the low- $\kappa$ .

Sidewall and bottom surface roughness: The introduction of plasma induced roughening of the bottom as well as the transfer of sidewall roughness from the photoresist can impact reliability and electrical dispersion. This roughness can directly impact the Cu diffusion barrier layer by preventing the formation of a continuous layer. Scaling of the barrier to  $\leq 3\text{nm}$  makes a suitable integration scheme all the more challenging.

### 4.5.2 PLASMA PROCESS CONTROL

Successful integration schemes require that the etch plasma be optimized for each material and structure. A tapered profile is preferred over a bowing profile for metal filling consideration. The desired profile can be achieved using the proper hard mask faceting management and good control of the passivation layer created during etching process. Additionally, bottom trench surface roughness has to be minimized. This roughness is minimized by optimization of the carbon / fluorine ratio in the etching chemistry and ion bombardment conditions including the flux and energy. The etching chemistry choice could also impact the sidewall modifications and feature scaling CDs. Development of an effective post-etches treatment for the removal of fluorocarbon species is needed. Additionally, given some integration damage of porous low- $\kappa$  is likely, some process for  $\kappa$ -value restoration must be developed.

At the advanced research level, it has been shown that the reactive radicals from UV radiation, intrinsic to many plasma processes, and ion bombardment are responsible for low- $\kappa$  damage. It has also been shown that the introduction of iodine based process gases including  $\text{CF}_3\text{I}$  can minimize the low- $\kappa$  damage due to lower UV radiation between 250 and 350 nm [2].

For better profile control, better in-line characterization of the profile is mandatory. Scatterometry technology is under evaluation as an alternative to conventional CD SEM and TEM cross section [3].

Potential solutions for reducing low- $\kappa$  damage in production environments include the use of hydrogen-containing chemistries ( $\text{H}_2$ ,  $\text{CH}_2\text{F}_2$ ,  $\text{CHF}_3$  ...) instead of the more damaging oxygen-containing chemistries ( $\text{O}_2$ ,  $\text{CO}$ ,  $\text{CO}_2$  ...). It is clear that with continued aggressive scaling that equally aggressive damage mitigation and restoration processes will have to be established.

### 4.5.3 PLASMA HARDWARE CONTROLS

Continual refinement of current Capacitive Coupled Plasma (CCP) source technology is expected to be able to adequately address the material challenges as well as shrinking trench and via dimensions at nearly constant aspect ratios. With the

introduction of porous low dielectric constant materials, ULK materials and selective air-gap technology, the implementation of a metal hard mask to reduce the ash damage is gaining momentum. The development of specific cleaning procedures for recovering the initial chamber wall conditions is required between multiple etching processes. For, example, the removal of fluorine containing species is critical in order to avoid electrical dispersion and increased defectivity. The plasma chamber cleaning will require a high-quality Si-based top electrode associated with good cleaning chemistries utilizing either oxidizing or reducing gases. Special attention has to be paid concerning development of cleaning procedures for waferless auto clean (WAC) to improve the mean time before wet clean (MTBC).

At the research level, Plasma Atomic Layer Etching (PALE) may be an emerging technique; however, the concept has to be studied further in order to prove the feasibility and global benefit for porous low- $\kappa$  material etching. Currently, the CCP source with double frequency is the accepted technology used in production.

### 4.5.4 INTEGRATION STRATEGY

Regarding process windows, the 20nm node and beyond will require the use of thinner photo resists as the critical dimension shrinks and the aspect ratio limitations remain. Two masking strategies are in competition and are used in production today. These include the metallic or organic hard mask. A multiple layer resist scheme will be required for upcoming process nodes for better dimensional control.

Delays in the implementation of EUV lithography have necessitated the use of double patterning to achieve the 32nm half-pitch. In the near term EUVL is likely to be delayed until at least the 16nm node for production, this will require the continued use of DP along with multiple patterning. This strategy is complex and expensive but is currently the only economic option [4]. At the research level several alternative lithography techniques are being explored including: Multi-beam lithography (Mask Less Lithography); and Di-Block copolymers, directed self assembly (DSA) [5]. Both techniques also have significant challenges remaining which are described in the lithography section. For example, ML2 lithography at low accelerating voltage will need a thin resist (40nm) which will require a new hard mask strategy using an adapted thickness or multi layer strategy in order to protect underlying low- $\kappa$  or ULK materials [6].

Any integration strategy must include both damage repair and pore sealing steps for porous ULK dielectrics after etching [7, 8]. These requirements might force etching or stripping tools into multi-station systems. Problems such as moisture absorption or the reaction of moisture with damaged dielectrics could require *in situ* process flows that include etch, dry strip, wet strip, damage repair, degas and pore sealing steps.

It has been shown that damage repair of ULK material can be achieved using a silylation process which replaces a silanol with a  $\text{CH}_3$  moiety. The replacement of the OH will make the low- $\kappa$  less susceptible to moisture absorption [9]. Partially or totally sealing pores in ULK materials may be realized using a “soft” plasma treatment with adapted chemistries such as  $\text{NH}_3$  [10] or alternatively  $\text{CH}_4$  to create a carbon rich layer. For both ULK damage repair and pore sealing, trench sidewall and bottom characterization must be addressed. For ULK material characterization (before and after etch) one possible emerging technique uses scatterometry / porosimetry to evaluate the percentage of porosity as well as the pore size.

This “Hybrid” approach means, that the porogens from the porous ULK are still present during etching, stripping and cleaning of the (dual-) damascene features and possibly even during Cu- and barrier-CMP after the metal fill [11, 12]. After finalization of these process steps the organic porogens in the ULK are then removed by thermal furnace, Ebeam or UV cure. This approach may significantly relax the requirements illustrated in figure INTC17 for etching, stripping, cleaning and CMP processes, because they are performed on a “quasi dense” or “hybrid dense” low- $\kappa$  material. Thus, the amount of processing induced low- $\kappa$  damage may be significantly reduced. However, concerns with the porogen approach remain which include film thickness loss, lateral shrinkage and porogen residue. Both issues could lead to reliability concerns. Recent work has shown that a low- $\kappa$  refilling process may compensate for the film thickness loss after the porogen is removed [13].

### 4.5.5 CLEANING PROCESS

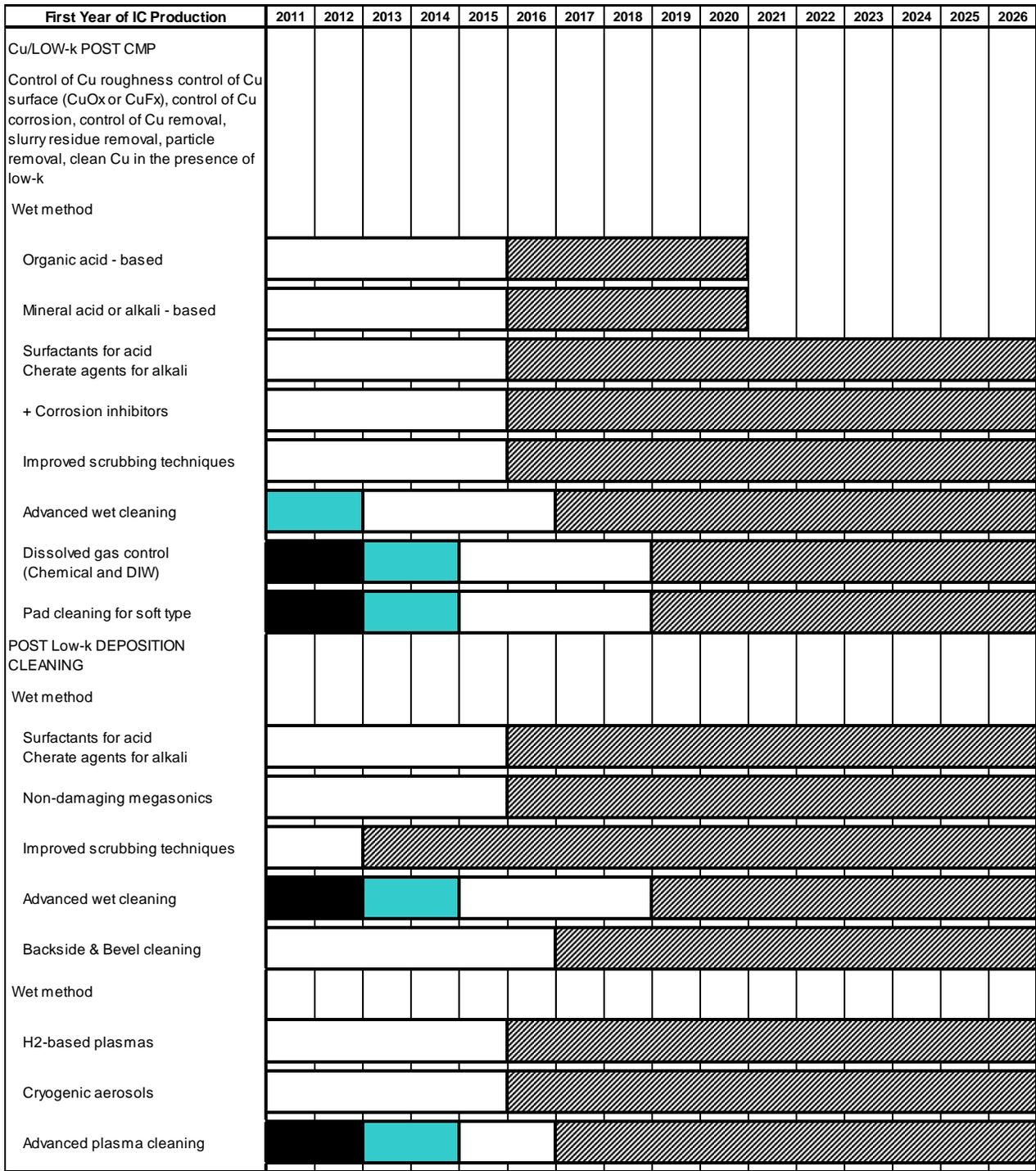
Wet cleaning is required in order to remove plasma sidewall polymer and metallic contamination. This cleaning process is commonly used between dual damascene etch and metal deposition steps. The clean is necessary to remove trapped fluorine gas; moisture on porous low- $\kappa$ ; residual sidewall polymers; and also any copper oxidation. All of these residues can impact the global yield of the overall processing. Figure INTC18 shows the current post-dielectric cleans roadmap. For example, copper surface control for successful subsequent processing is critical for reliable electrical performance. This includes addressing the process queue time between etching and cleaning.

According to these criteria, good advanced wet chemistries formulations have to be efficient for removing native  $\text{CuO}_x$  and post etch residues and at the same time prevent copper surface corrosion and re-oxidation especially since copper is not electrochemically stable.

Conventional solvent chemistry commonly used for previous nodes could be replaced by diluted organic acids in wet or vapor phase processing mainly for efficiency and cost considerations [10, 14]. Short process time with fresh chemistries is preferable. The organic acids have a chelating effect with copper while very dilute HF chemistry can address sidewall polymer removal with respect to CD control.

The successful integration of new ULK materials will depend on a stronger collaboration between the deposition, lithography, cleans, and etching groups. Reduction of the RC delay will be a requirement for the continued conventional scaling in the semiconductor industry. Successful new integration schemes will depend on novel etch and cleans enabling adoption of ULK materials with a  $\kappa_{\text{eff}} < 2.3$ .

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This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.

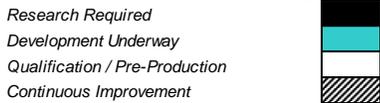
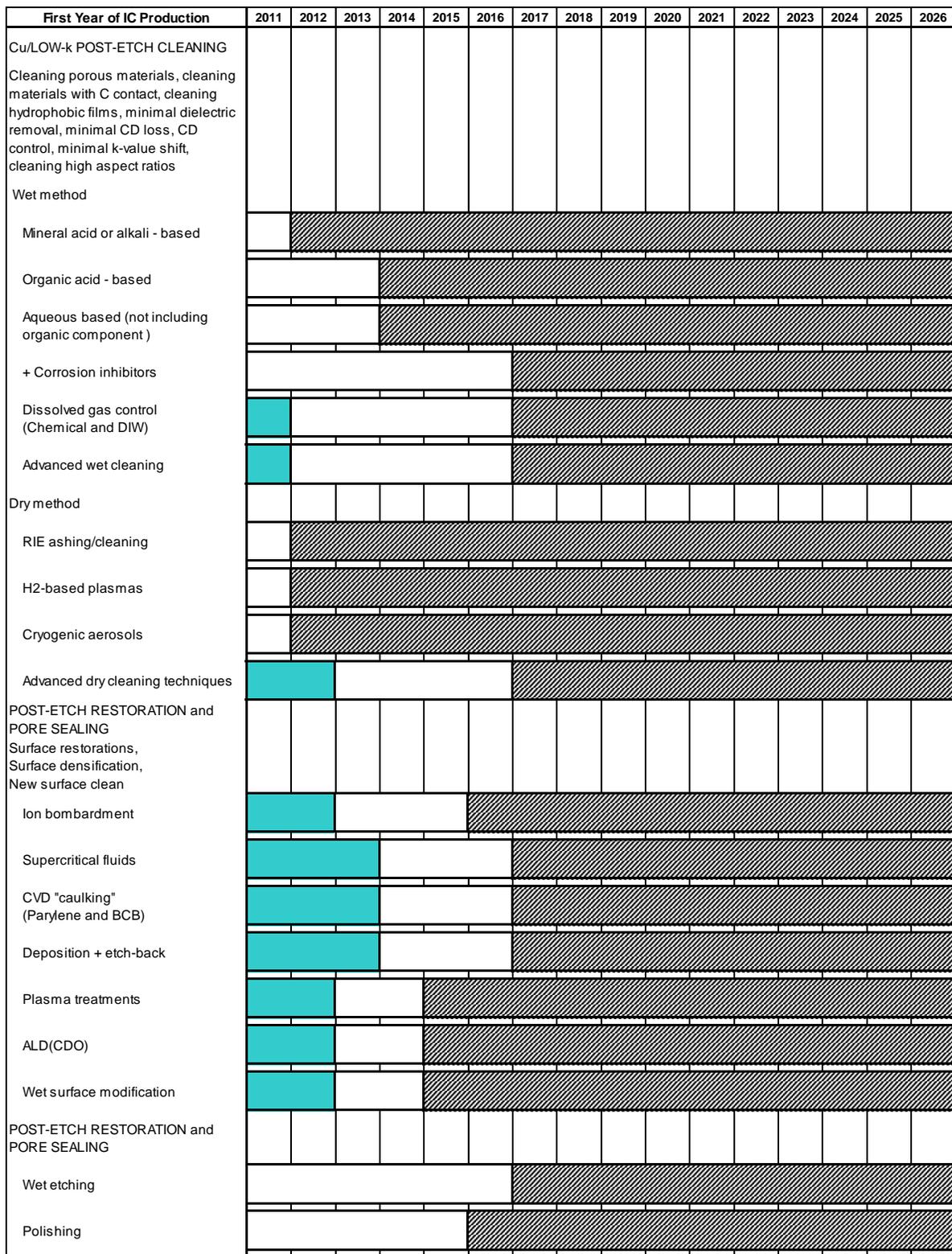


Figure INTC17 Post-CMP/Deposition Clean



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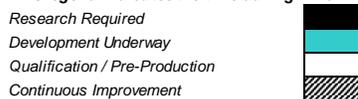


Figure INTC18 Post Dielectric Etch Clean

## 4.6 PLANARIZATION POTENTIAL SOLUTIONS

### 4.6.1 INTRODUCTION

Chemical mechanical polishing (CMP) has become the standard technology for the planarization necessary to make leading interconnects. Any planarization process has the requirement of producing an adequately flat surface across the wafer that is free of significant defects. This must be accomplished consistently and at a reasonable overall cost. Since feature size decreases and wafer size increases will continue, these planarization requirements become more severe over time. A brief overview of planarization technology, the latest problems, and potential solutions are discussed.

Before CMP, the main dielectric planarization techniques were processes such as bias CVD [1], TEOS-O<sub>3</sub> CVD [2] and Spin-On-Glass (SOG) [3]. Planarization of metals was done through processes such as reflow of Al interconnects [4] and etch-back after W CVD [5]. Those technologies have largely been replaced by CMP for advanced devices. The initial purpose of CMP, which was initially adopted in early 80's, was planarization of Inter-level dielectric (ILD). Since then, CMP has been adopted for a wide variety of structures and materials. With each technology generation, the number of CMP steps being employed continues to steadily rise [6]. The average process complexity is also rising as more materials need to be planarized within a single process step and as more CMP solutions involve multiple steps. All this is in addition to the significant challenge of meeting the new planarization needs for shrinking dimensions. An overview of planarization concepts is given in Figure INTC19.

# Brief History of Planarization Solutions

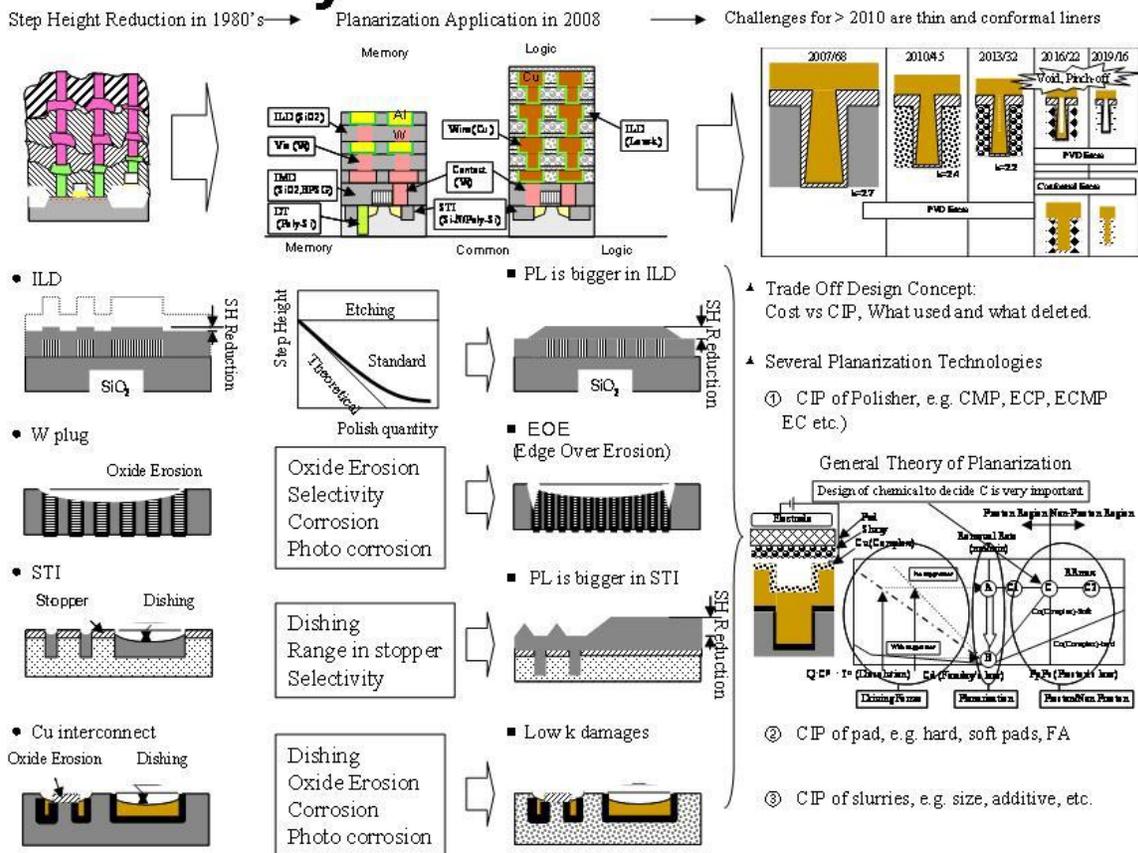


Figure INTC19 Brief History of Planarization Solutions

The planarization potential solutions chart, Figures INTC20 and INTC21, is broken into three sections. The first details a timeline for the major applications. This timeline serves as a preface to the potential solutions described in the equipment and consumables sections.

#### 4.6.2 DIELECTRIC CMP

For most ICs, PMD CMP is the first interconnect planarization process. The PMD film is planarized and then thinned down to a desired target thickness over the gate stack. Defectivity is especially important for this step. It is standard in DRAM for the PMD CMP step to remove the dielectric down to the gate stack and stop on it with high selectivity.

The most common use of ILD CMP today is for the storage node and interconnects in memory devices. Figure INTC19 shows how ILD CMP can minimize step height created by lines and spaces. As scaling has progressed, the initial film profile entering CMP has drastically changed. Instead of creating a separate hump over each line, the dielectric creates a raised block or wide planarization length (PL) over the array of lines. The increased length effect has also been seen in shallow trench isolation (STI) CMP, which is discussed in the *Front-End Processes* chapter. In addition, nano-topography and roll off in the incoming material [7] need to be minimized to avoid affecting planarization performance. With scaling, the range in remaining thickness after CMP that can be tolerated also decreases.

Changes in structures and materials being utilized continue to lead to the creation of new planarization applications. Starting with hp45nm technology, metal gates were introduced. In the gate last integration scheme for creating metal gates, CMP of the pre-metal dielectric can be done with high selectivity to Silicon nitride followed by a CMP step that polishes the nitride over the dummy gate while stopping on the pre-metal dielectric. A leading alternative for the floating gate for flash memory also involves polishing dielectric and stopping on polysilicon. CMP has been used as an option to aid lithography in double-patterning schemes and in planarization of photoresist for dual damascene patterning. New ways of creating non-volatile memories and logic devices with air gaps for the lowest effective K values are driving the need for ILD-like steps where Low- $\kappa$  and Ultra-Low- $\kappa$  dielectrics are planarized. An optional final backside Si thinning step for 3DIC's can also be considered a new dielectric step where a high removal rate is desired. 3DIC's also require the passivation dielectric stack to be removed, exposing the metal Through-Silicon-Via, which can be accomplished with CMP.

#### 4.6.3 CONDUCTOR CMP

The implementation of metal gates at 45 nm also led to a new planarization step. A bulk metal such as Al or TiN is deposited over the gate work function metal in the recess left by the dummy poly gate that was removed. The metal is polished back, stopping on the remaining pre-metal dielectric. Planarity and film loss control are important.

Polysilicon is still widely used for contacts and landing pads in DRAM technology. Over time, the contact process is moving from one that simply stops on dielectric to one that removes a combination of dielectric and nitride. Planarization of polysilicon stopping on dielectric is common for flash floating gates.

The first implementations of W for contacts and vias employed etchback processes. Manufacturability was enhanced by replacing these processes with CMP of the W and Ti-based liner. Leading logic devices today use W only at the contact level. In DRAM, the interconnect steps are migrating away from W and ILD CMP to Cu and barrier CMP. Due to the replacement of polysilicon etchback and emergence of double contact schemes, however, the overall number of W CMP steps is not dropping. An issue in W CMP has been the edge-over-erosion (EOE) effect where erosion increases at the edge of pattern arrays. This has been improved by development of slurries and pads. One avenue to improving overall planarity has been implementation of slurries with lower selectivity to dielectrics.

The use of selective W CMP in memory for creation of bitlines and wordlines has been rising. Cu and Barrier CMP see more planarization steps than any other l type. A multi-step process is performed in which the Cu is polished back to the Ta-based barrier layer and then Cu, the barrier, any hardmask material, and then the desired amount of dielectric are removed at rates that optimize the final topography and thickness. Corrosion including galvanic and photo-corrosion [8] is regarded as an eternal problem for conductor polishing in a conductive liquid. As technology progresses, the dielectric constant is being driven down. The combined effect of smaller features built from more fragile materials is driving the need to reduce maximum stresses applied during planarization to prevent structure damage. Stress improvements are being sought with CMP and alternatives such as ECMP (Electrochemical Chemical Mechanical Polishing), ECP (Electro Chemical Polish) and CE (Chemical Etching), and combinations of these are being investigated [9]. As the mechanical component of Cu removal is decreased, the chemical component is being increased. This must be done in such a way that corrosion protection is maintained and planarization is not only maintained but improved.

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Barrier CMP processes for the future need to deal with these issues, plus more. As patterning and metal fill become more difficult, CMP is being asked to remove new barrier layers and an increasing number of dielectric or metal hardmask films. The effective dielectric constant needs to be minimized, which means polishing onto or into dielectrics with increasing porosity. Preventing change to the dielectric is being done through a combination of optimized CMP, post-CMP cleaning, and restoration techniques. Since the number of Cu and barrier steps in advanced flows is high, there is special attention placed on solving all the issues already mentioned in a way that drives throughput up and overall cost down.

There are several impending needs for new planarization applications for conductors. Considered a Front-End Process, polysilicon is increasingly being planarized before gate patterning, particularly for multigate transistors. W contact processes for memory now often stop in a mixed dielectric surface. Redesign of W contact structures in conjunction with metal gates has created an alternative where the W bulk and buff processes must stop in a mixed surface of dielectric and metal. W for contacts will eventually need to be replaced by a better conductor. New elements competing for adoption in barriers such as Ru, Mn, and Co will be needed and will add challenges to the planarization processes. Increasing porosity will eventually likely give way to air gap structures, which will add challenge to the planarization steps for copper and barrier. DRAM capacitors are starting down the long-delayed path of implementation of noble metals and a special planarization step will likely be required. A variety of non-volatile memory technologies beyond flash are being developed. Formation of the storage cells in those technologies is expected to shift towards damascene processing and CMP as they mature, which is being seen for the GeSbTe layer for PRAM today. As 3DIC technologies are becoming more widely adopted, improvements are needed in special high rate bulk metal and barrier processes to create those large features with low cost.

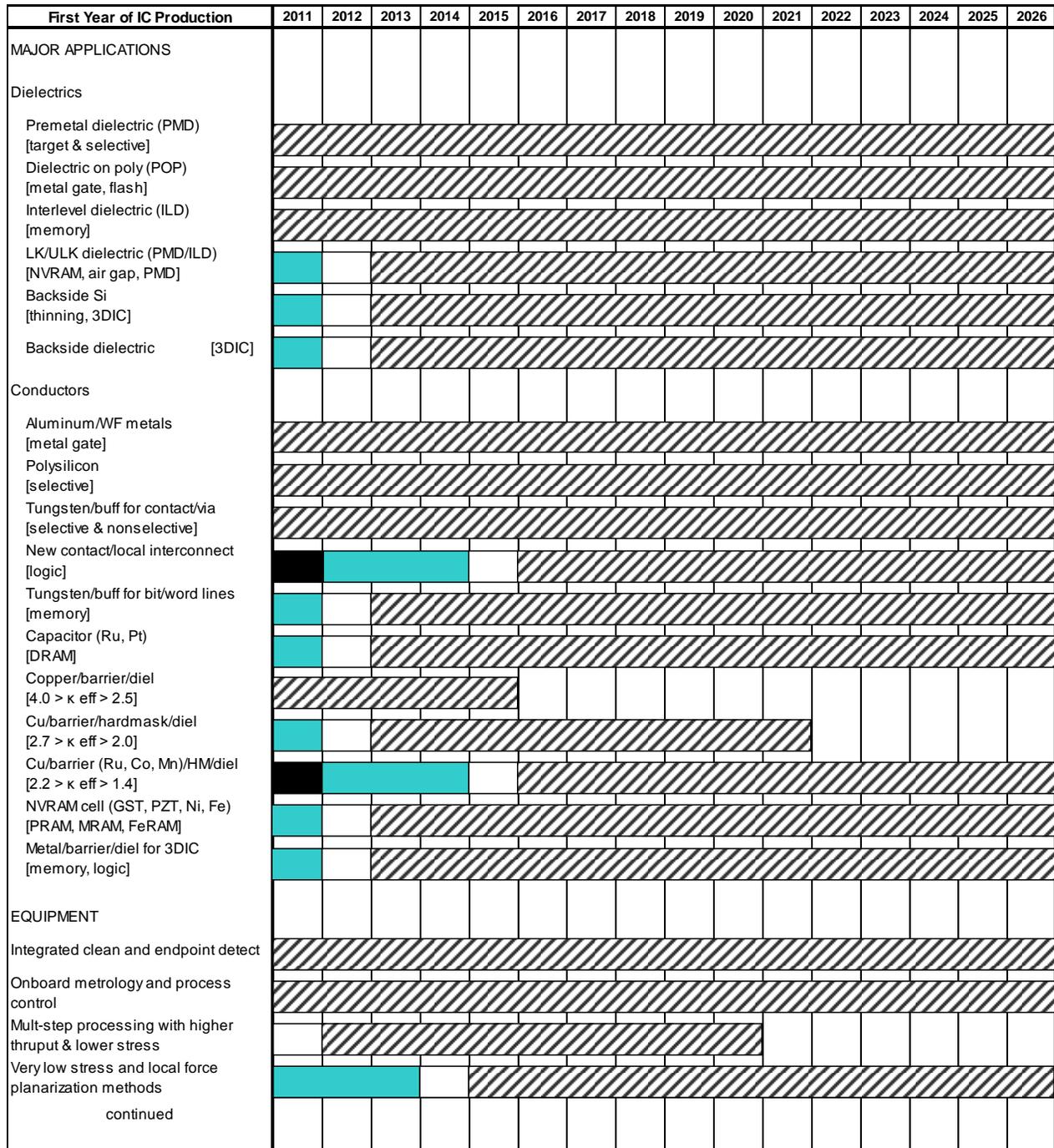
### 4.6.4 EQUIPMENT

Polishers with rotary motion and integrated cleaning, called dry-in and dry-out concept, have been widely adopted. Although equipment is now more mature, modification and improvement must be continued to meet the needs of the new processes described above. Efforts to enhance Overall Equipment Efficiency (OEE) will also be continued. In addition, a new concept called “Trade-off design” in which parts necessary would be added and unnecessary parts abandoned is needed to decrease CMP equipment cost. Greater emphasis is being placed on endpoint and measurement capability which improve process control and non-uniformity. Endpoint metrology is preferred versus inline measurement, due to the delay between measurement and process adjustment. Barrier CMP is an application today where measurement technology is used, but a true endpoint is wanted. Equipment is being designed for lower pressures for lower stress. Equipment must be created for novel low-stress planarization methods and must be designed together with the consumables. Both standard and novel methods need innovation to achieve tighter non-uniformities with smaller edge exclusions. The shift coming soon to 450 mm will drive a large amount of additional work.

### 4.6.5 CONSUMABLES

Consumables are the largest contributor to many planarization performance metrics, so significant advances will be required. High solids slurries utilized today are being driven to increased consistency, especially in defectivity. Development must be done for a wide variety of slurries that must simultaneously lower defectivity, improve planarity, and decrease cost to support increasingly complex applications. Current trends to drive down solids and improve chemical activity will continue. The abrasives being used are increasingly being engineered specifically for CMP. The abrasives must be made with acceptable purity and unique surface and bulk characteristics. Combinations of chemistries and particles that create tunable platforms are being leveraged to make robust achievement of all the needs and easier support of those needs possible. Many of the alternative planarization techniques will need new robust manufacturing-ready fluids in order to enable each technique. Cleaning chemistries must also be developed which optimize removal for specific slurries and substrates, without inducing issues such as corrosion. This challenge is especially steep for interconnects with porous films. New materials and form factors for the brushes in the cleaners are needed.

Significant advances will also be needed from today’s urethane pads to extend the range of hardness and chemical transport options for use across different applications. Pads containing abrasives are mainly used for STI. There is a strong need for development of a wide range of pad types that can be paired with slurries by application. Advanced pad conditioning methods are also needed, especially for new pad types.



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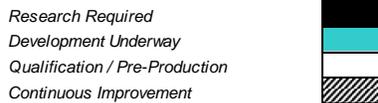


Figure INTC20 Planarization Applications and Equipment Potential Solutions

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First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
CONSUMABLES																
Fluids																
High solids slurries																
Slurries with low solids/defects/cost																
Tailored slurry formulations from tunable platforms																
General cleaning solutions																
Cleaning and buff solutions tailored to applications																
Pads																
Urethane pads for new applications																
Abrasive containing pads																
Range of alternative pads for planarity/defects/cost																

**This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution.**

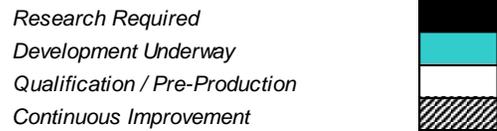


Figure INTC21 Planarization Consumables Potential Solutions

## 4.7 THROUGH-SI-VIA (TSV), 3D STACKING TECHNOLOGY

### 4.7.1 INTRODUCTION

The 3D interconnect technology based on TSV interconnects basically consists of three main process modules: (1) the TSV module itself, (2) wafer thinning and backside processing, and (3) the die or wafer stacking process (permanent bonding and/or temporary bonding). Each of these steps requires rather specific equipment and process technologies and may be executed by different parts of the microelectronic supply chain. The discussion below on process modules is therefore organized along these three basic elements.

### 4.7.2 THROUGH SI VIA TECHNOLOGIES

A wide variety of techniques to realize via-connections through the Si-substrate of an integrated circuit have been proposed. The actual processing may be performed before, during, or after the IC fabrication process. Processing can also be done with the sole intention of forming silicon interposers without embedded active devices. However, a number of common features can be clearly defined: a hole has to be etched in the Si substrate; an isolation layer has to be provided to isolate the TSV electrically from the Si-substrate; a barrier layer has to be provided to prevent diffusion of metals into Si, and the via must be filled with a conductive material. The most common approaches to TSV technology are to provide for the TSV function before finalizing the wafer, (prevalent for 3D-SIC technology) or to realize the vias after finalizing the wafer (prevalent for 3D-WLP technology).

#### TSV ETCHING TECHNOLOGY

TSV holes are generally not etched through the entire wafer. Wafer processing with actual through-Si holes is not compatible with standard semiconductor or wafer-level-packaging processes and equipment. The prevalent technology is to use a “blind” via approach from the front side or the TSV is etched until an etch-stop layer from the back side, as shown in Figure INTC22

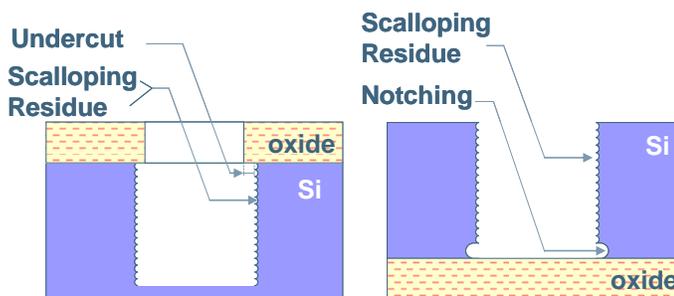


Figure INTC22 Schematic Crosssections of the Challenges for Si-TSV Plasma Etching

#### ETCHING THROUGH MASK, OXIDE OR BEOL LAYERS

Depending on the actual integration scheme used, etching a via hole in the Si substrate may require etching through resist, oxide or BEOL layers such as SiO, SiN, SiON, SiO(C) and, in certain cases, low- $\kappa$  materials, as indicated in Figure INTC22. Before etching the TSV-via in the Si, the masking layers have to be etched. This can be done using a separate tool or chamber prior to the Si-etch or in the same tool as the Si-etch. Depending on the selectivity of the Si-etch with respect to the passivating or masking layers, there will be etch process development challenges when thick passivating/masking layers are used. There are also concerns with Si etch undercutting below the patterned passivating/masking layer.

### ***ETCHING HIGH ASPECT RATIO SI HOLES/TRENCHES***

The actual fabrication of the Si hole is commonly realized by plasma etching. A specific feature of TSV Si via etching is the need for etching deep, and often high aspect ratio holes in Si. This may require long processing times on expensive equipment, so fast etching processes are highly desirable.

Critical aspects of via hole etching include good control over sidewall tapering angle (both global and local), minimal sidewall roughness and scalloping, minimal residue/defect issues, minimal undercutting and notching issues, minimal local bowing effects right below masking layers, respectable etch rates, and excellent repeatability and within wafer center-to-edge depth and profile uniformity.

In order to avoid isotropic etching of the Si, the etching recipe balances sidewall passivation with bottom Si-etch process chemistries. The prevalent technique used is the “Bosch” recipe, in which passivation and etch steps alternate in time. During the passivation step, a polymer is deposited on the Si surface. During the Si etch step, the polymer is easily removed from the bottom surface of the hole, while remaining on the via sidewall, protecting the previously etched Si sidewall. An undesired characteristic of this technique is “scalloping” on the Si sidewall, as can be seen schematically in Figure INTC22. The periodic circular ridges formed along the perimeter of the sidewall after each cycle can add complexity to the following steps.

Depending on the critical dimensions, aspect ratio, and final depth of the TSV etch process, there are also non-Bosch RIE process solutions. These usually involve hardware upgrades, followed by advanced process development to existing CMOS plasma etchers (oxide or polysilicon) [1] and primarily address three main attributes unique to the nominal feature size of a TSV structure: 1) high etch rates on the order of 5–15 $\mu\text{m}$  per minute, 2) high anisotropy/ability to modulate the taper angle, and 3) high selectivity to Si etch. From a manufacturing perspective, the main advantages of the non-Bosch RIE process over the Bosch process include smooth sidewalls with no scalloping; ability to modulate sidewall tapering angle; re-use of existing tools; minimal F-containing polymer residues, and minimal undercutting. It is noteworthy that when the critical dimension becomes too small (usually less than 1 micron) and the aspect ratio becomes too high (usually greater than 20:1), the type of RIE used may tip to favor Bosch etch.

After etching, cleaning the Si via hole is a critical process. In particular, the F-containing polymers deposited during the passivation cycle of a Bosch etch need to be fully removed before further processing.

Another inherent characteristic of deep Si etching processes is the aspect-ratio dependent etch rate. As vias are etched deeper into the Si wafer, or as viadiameter decreases, etch speed goes down. This typically causes a linear dependence between the average etch rate and the feature size aspect ratio. The consequence is that CD control for TSV patterning is critical to obtaining a uniform wafer-to-wafer processing speed.

### ***TSV LINER PROCESS—ISOLATION LAYER, DEFINES TSV CAPACITANCE***

In order to electrically isolate the TSV connections from the Si substrate, an isolation layer is required. The key requirements for this layer are that it should exhibit low leakage current, sufficiently large breakdown voltage, and low capacitance.

Deposition of the TSV liner layer must be compatible with the device process flow. For the deposition temperature, this implies for “via middle” a deposition temperature acceptable to the front-end process devices and for “via last” deposition temperatures, acceptable temperature for the back-end interconnect processes and, when processing on carriers, compatibility with the temporary bonding materials. In particular, for post-processing on DRAM memory devices, temperatures below 200°C may be required to avoid damage to device wafers.

Ideally this layer should planarize the Si sidewall roughness (e.g., scallops from Bosch etching). Conformal deposition on sidewall scallops may cause a more difficult surface topology for the following processing steps.

The most popular liners are oxide or nitride layers, deposited by CVD, although PVD techniques are also being evaluated. Obtaining a conformal fill is more difficult at low processing temperatures. Nitride results in a higher capacitance, but can also act as a barrier layer to prevent metal diffusion.

For 3D-WLP via-last TSVs, the use of polymer isolation layers is also possible. This allows for a significantly lower capacitance of these larger diameter structures and also allows the metal in the TSV structure to absorb some strain. [2]

### TSV BARRIER LAYER

In order to avoid migration of TSV metal into the Si, a high quality, pin-hole free barrier layer is required. The prevalent barrier materials are Ta and TiN, which also improve adhesion between the TSV metal and the liner.

Prevalent technologies for barrier deposition are PVD and CVD. Different forms of CVD allow for barrier deposition on the most challenging, high aspect ratio TSV via holes. PVD technology has more limitations, with respect to coating conformality and via aspect ratio, but is often preferred because of superior adhesion, the barrier properties of films and lower operational costs. Improvements in PVD equipment have extended the process window for PVD barrier deposition.

### TSV METAL FILL PROCESS

The main approaches to realize conductive TSV structures are using electrochemical deposition (ECD) of Cu, CVD of W, CVD of Cu or, for via first approaches, poly-Si via fill. Several process options for Cu or W fill are available, and are discussed in more detail below. Figure INTC23 maps the different process options for Cu and W-based TSVs as a function of TSV diameter and aspect ratio, in relation to the 3D-TSV roadmap.

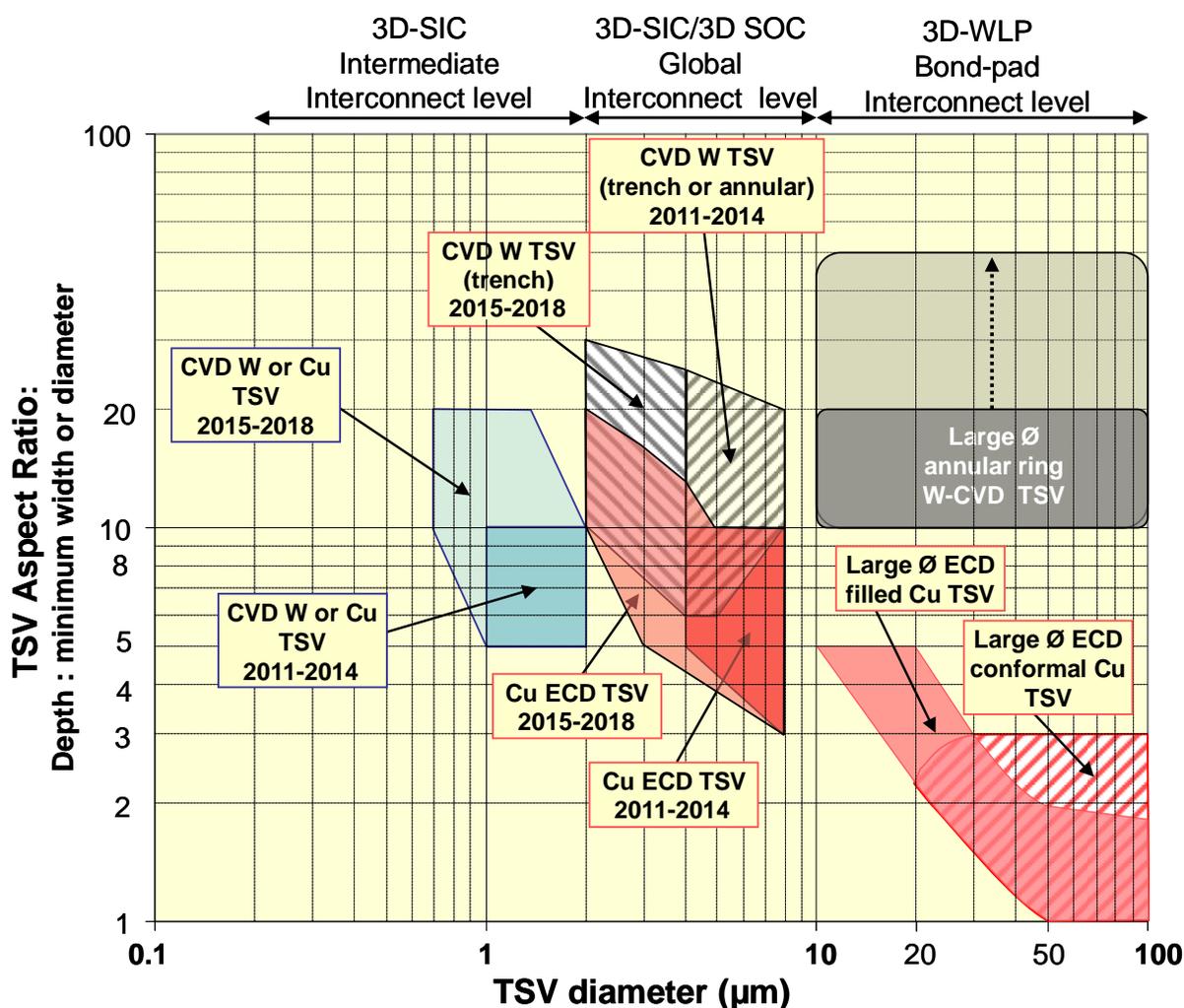


Figure INTC23 Cu and W-based TSV Options as a Function of TSV Diameter and Aspect Ratio, in accordance with the 3D Interconnect Hierarchy and Roadmap

(Trench and annular TSV refer to non-cylindrical TSV shapes which are narrow in one lateral dimension.)

### **Cu TSV**

The process steps in Cu TSV are: Cu seed deposition, Cu-via fill by ECD, and CMP removal of Cu-overburden.

The prevalent technology is derived from commonly used single damascene Cu plating BEOL processes. The main difference is the high aspect ratio of the Cu TSV features. [3]

For the Cu seed deposition process, the prevalent technology is PVD. The main challenge is to obtain a continuous Cu seed layer in high aspect ratio TSV structures. The highest TSV aspect ratios successfully realized using Cu PVD are 5 to 10. Alternative technologies for high aspect ratio TSVs are CVD Cu, electrografting of Cu seed layers, and direct-on-barrier plating.

The main challenge for the ECD Cu filling process is to realize void-free Cu-filling of the Cu-TSV structures. This requires a “superfilling” of the etched via structures. This is achieved by carefully controlling additives to the plating solution which accelerate plating in the bottom of the via and suppress and smooth plating on the wafer top surface. The resulting processes are slow and require equipment that can run multiple wafers in parallel on a single tool.

After ECD Cu deposition, the Cu is annealed. A typical via-middle process is followed by Cu-CMP. In addition to the Cu CMP, the barrier and liner layer must be removed to allow further BEOL processing.

### **W TSV—W CVD FILL, CMP**

CVD can be used to fill narrow TSV structures with large aspect ratios. TSV with diameters up to 3 $\mu$ m have been reported. [4] Larger TSV structures are realized by combining multiple TSVs in parallel, using narrow slits or using annular ring TSVs. The W CVD process is highly conformal. A typical W TSV filled structure is characterized by a center-seam void.

Since relatively thick tungsten layers are required to fill the TSVs, a partial blanket W etchback to a resulting film thickness < 500 nm is carried out, avoiding any peeling or delamination. The partial etchback also helps to decrease wafer bow to a moderate level.

After CVD W fill, the typical process consists of W CMP to remove the W on the wafer field. After this step, a barrier/liner layer CMP may have to be performed to allow for further wafer processing.

As an alternate to W CMP step, an etchback process can be used to define the contact pads to the W TSV structures. [5]

### **POLY-Si TSV: VIA-FIRST TECHNOLOGY**

For via-first technologies, Cu and W TSV cannot be used because of compatibility problems with the FEOL process. Poly-Si can be used as a TSV fill. In this case, only a liner (no barrier layer) is required. After polysilicon deposition the wafers are polished and the standard Si process flow can be performed. This requires high quality pre-processing steps to avoid yield loss during device manufacturing. The higher resistivity of polysilicon limits the use of this approach to applications that allow for high-impedance TSV interconnects.

## **4.7.3 WAFER THINNING AND BACKSIDE PROCESSING**

### **TSV BEFORE 3D-BONDING**

This is a parallel processing approach to 3D integration. Wafers are prepared for 3D stacking by performing TSV processing and contact pad formation in parallel. At the end of the process, the different die or wafers are combined to realize the 3D-stack. (See Figure INTC24.)

Realizing TSV-vias before 3D-bonding implies processing on thinned wafers. For a via-last process this can be the actual fabrication of the TSV connections. For via-first and via-middle processes this typically consists of processes to expose the TSVs on the wafer backside, provide a backside passivation, and create redistribution and bump structures on the wafer backside. These processes may be extensive and require relatively high temperatures.

For flows using wafer thinning before bonding, a robust thin wafer carrier process is required. The requirements for 3D-stacking are significantly more stringent than classical wafer thinning and singulation processes used for 3D-SIP applications and require dedicated solutions.

The key steps for this process are as follows:

### THIN WAFER TEMPORARY CARRIER SYSTEMS

The thin wafers carrier system should allow for extensive post-processing of the thinned wafers in standard semiconductor processing tools. The temporary glue layer between the thin device wafer and the carrier should be stable during all the (high temperature) TSV processing steps and should be able to detach, without leaving residues or damaging the thin 3D die.

Two main strategies are followed:

a) One strategy is to use glass substrates as carriers. This allows for the use of optical techniques to cure (e.g., UV-cure) or debond (e.g., laser ablation) the carrier wafer from the thin TSV wafers at the end of the process. It also allows for optical back-to-front alignment for backside processing. Disadvantages of glass carriers are the need for special Si CTE-matched glass, the cost of the carrier wafers, and compatibility with standard semiconductor processing tools.

b) The alternative option is to use Si wafers as a temporary carrier substrate. A typical process flow is shown in Figure INTC24. In order to avoid problems with the razor-sharp edges of silicon wafers after thinning, wafer edge trimming is performed. As a result, the thin wafer has a smaller diameter than the carrier wafer after thinning. This allows for more robust handling of the wafer in standard semiconductor equipment.

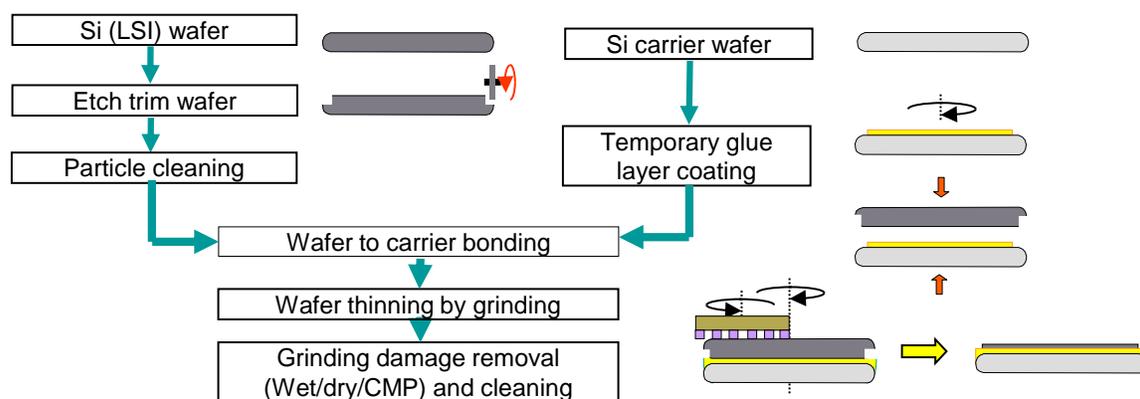


Figure INTC24 Temporary Carrier Strategy for Thin Wafer Post-processing

The temporary glue layers for this process are challenging and critical to the success of 3D-integration schemes. A complex combination of properties is required: Stability during processing with the capability of easy debonding. A wide variety of debonding mechanisms is being studied, such as laser-assisted (glass carriers), melting and sliding (thermoplastic adhesives), dissolution in solvents, and mechanical debonding (peeling).

### WAFER THINNING

Wafer thinning by grinding is a well established process in semiconductor packaging. Critical for TSV technology is Si thickness control and surface quality. The total thickness variation of the thinned wafer is a combination of the thickness variation of the carrier wafer, the temporary glue layer thickness variation, and the accuracy of the grinding tool. After mechanical grinding of the wafer, a thin damaged Si layer is present on the wafer backside. CMP, dry etch and wet etch techniques are used to remove this damaged layer. When grinding Si wafers with already processed TSV structures, particular attention must be paid to exposing the TSV structures from the wafer backside. This may require additional processing steps.

### WAFER CLEANING AFTER THINNING.

Mechanical back grinding may leave particles on the wafer backside. In order to allow re-introduction of these wafers into a process line for backside processing, a thorough particle cleaning is essential.

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### **WAFER BACKSIDE PROCESS REQUIREMENTS**

The thin wafer on carrier must be compatible with standard semiconductor processing equipment to allow for processing such as:

- Via-last TSV processing (particularly typical for 3D-WLP)
- Backside wafer passivation
- Optional backside interconnect redistribution
- Backside interconnect “bumping”

### **GETTERING PROPERTIES**

After thinning the wafer the gettering properties should be considered

### **4.7.4 TSV AFTER STACKING OPTION**

This is a sequential processing approach to 3D integration. Wafers are bonded together before 3D TSV processing. The process is repeated for multiple tier stacking. As a result, the bottom wafer goes through all TSV-processing steps:

- Wafer-to-wafer permanent bonding to bottom wafer or wafer stack
- Wafer thinning, total thickness variation and Si-surface quality, impact on devices
- Wafer cleaning after thinning, allowing re-introduction into a process line for further processing
- Wafer backside process requirements, TSV or pad metallization layer process

### **4.7.5 STACKING TECHNOLOGY MODULE**

- Wafer-to-wafer bonding approaches:
  - Polymer or oxide W2W bonding
  - Metal to metal W2W bonding
  - Metal/oxide or metal/polymer W2W bonding
- Die-to-die or die-to-wafer bonding approaches:
  - Metal/metal thermo-compression bonding
  - Cu/Sn and similar  $\mu$ bump interconnect techniques
  - Other approaches: e.g., caulking

## 5 EMERGING INTERCONNECT SOLUTIONS

### 5.1 OVERVIEW

It is clear that while transistor performance intrinsically improves with geometric scaling, interconnect performance does not. This implies that unless revolutionary interconnect solutions are found, interconnects will increasingly limit the performance and power efficiency of new products. Looking forward, a coherent vision for both global and local interconnects faces numerous challenges and few potential solutions.

For global interconnects, multi-core designs reduced the longest interconnect path lengths and helped mitigate the problem, but extreme parallelism has limitations for most applications; however, 3D interconnects still faces integration and reliability challenges. For global interconnects, the geometrical path length reduction solution using 3D stacking is a potential solution. Another viable RC alternative for global interconnect is optical interconnects, which will be discussed in more detail later in this section.

For local interconnects the sidewall and grain boundary scattering in narrow metal trenches rapidly increases the resistivity and delay. The rapid increase in resistivity in narrow trenches requires the consideration of new conduction systems which do not suffer from either sidewall or grain boundary scattering. Ballistic transport in one dimensional systems, such as silicides, carbon nanotubes, nanowires, graphene nanoribbons or topological insulators offers potential solutions. While ballistic transport has many advantages in narrow dimensions, most of these options incur fundamental, quantized resistances associated with any conversions of transport media, such as from Cu to CNTs. In addition to the

quantum resistance, the technological problems of utilizing an additional conduction medium with its interface, substrate and integration issues, pose substantial barriers to the implementation of ballistic transport media.

It is important to note that the research to find new transistors or switches to replace FETs may present an important opportunity to implement new transport media for local interconnect. For example if graphene-based switches are identified as promising replacements to CMOS transistors, then it would be logical to use graphene conductors as the local interconnects. For these interconnect applications, referred to as native device interconnects, one needs to explore the combined switch and local interconnect properties of the new system. In other words, a great switch which cannot communicate effectively with its neighboring switches would not improve system performance. The section on Si CMOS Replacements discusses these implications in more detail.

There are two classes of emerging interconnects: Cu replacements, and native device interconnects. The Cu replacement options replace the copper communication medium with other less mature technologies, including carbon-based and optical options. The native device interconnect options are highly speculative since they are by definition dependent upon the use of new types of switches, but the consideration of their properties is essential for driving the roadmap towards the correct solutions beyond the timeframe of the FET switch. Table INTC10 lists brief summaries of the principal advantages and concerns for thirteen different emerging interconnect options.

*Table INTC10 Advantages and Concerns for Cu Extensions, Replacements and Native Device Interconnects*

Application	Option	Potential Advantages	Primary Concerns
<b>Cu Replacements:</b>	Other metals ( Ag, silicides, stacks)	Potential lower resistance in fine geometries	Grain boundary scattering, integration issues, reliability
	Nanowires	Ballistic conduction in narrow lines	Quantum contact resistance, controlled placement, low density, substrate interactions
	Carbon Nanotubes	Ballistic conduction in narrow lines, electromigration resistance	Quantum contact resistance, controlled placement, low density, chirality control, substrate interactions, parametric spread
	Graphene Nanoribbons	Ballistic conduction in narrow films, planar growth, electromigration resistance	Quantum contact resistance, control of edges, deposition and stacking, substrate interactions
	Topological Insulators	Suppression of elastic backscattering, spin polarized transport	No suppression of inelastic backscattering, inability to stack
	Optical (interchip)	High bandwidth, low power and latency, noise immunity	Connection and alignment between die and package, optical /electrical conversion efficiencies
	Optical (intrachip)	Latency and power reduction for long lines, high bandwidth with WDM	Benefits only for long lines, need compact components, integration issues, need WDM
	Wireless	Available with current technology, parallel transport medium, high fan out capability	Very limited bandwidth, intra-die communication difficult, large area and power overhead
	Superconductors	Zero resistance interconnect, high Q passives	Cryogenic cooling, frequency dependent resistance, defects, low critical current density, inductive noise and crosstalk
<b>Native Device Interconnects:</b>	Nanowires	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, substrate interactions, fan out/branching and placement control
	Carbon Nanotubes	No contact resistance to device, ballistic transport over microns	Quantum contact resistance to Cu, fan out/branching and placement control

	Graphene Nanoribbons	No contact resistance to device, ballistic transport over microns, support for multi-fanouts	Quantum contact resistance to Cu, deposition and patterning processes.
	Spin Conductors-Si(Mn), Ga(Mn)As	Long diffusion length for spin excitons	Low T requirements, low speed, surface magnetic interactions

## 5.2 CU REPLACEMENTS

Since the bulk electrical resistivity of Cu is superior to nearly all conventional metals (except Ag), a metal's suitability as a potential Cu replacement is determined primarily by the impact of finite size effects on its electrical transport properties. Alternative materials have been investigated that may possess superior electrical resistivity to Cu at wire-widths consistent with end-of-roadmap dimensions, although the bulk electrical properties of these materials are inferior to those of Cu. Also, novel quantum effects in ultra-thin film or nano-line geometries of metallic non-Cu multi-layers may provide improved performance compared to conventional Cu/barrier systems. Potential options are described below.

### 5.2.1 METAL SILICIDES

The bulk electrical resistivity of nickel monosilicide conductors ( $\sim 10 \mu\Omega\text{-cm}$ ) has been shown by several researchers to be unaffected by lateral wire dimension for single-crystal nanowires (SCNWs) approaching 50 nm [1-3]. This is attributed to the small electron mean free path ( $\sim 5$  nm) in NiSi. The preservation of bulk resistivity in NiSi SCNWs with diameters as small as 15 nm has been reported by one group to date [3] and compares favorably to expectations for polycrystalline Cu at those dimensions. Intrinsic integratability with Si-based devices and the prevalence of NiSi contacts in current FEOL processing is likely to keep interest high. Other nickel silicide phases have also shown bulk-like electrical resistivity in sub-50 nm diameter SCNWs. NiSi<sub>2</sub> SCNWs with diameters as low as 40 nm [4] exhibited an effective resistivity of  $30 \mu\Omega\text{-cm}$ , in line with bulk NiSi<sub>2</sub> values. Likewise, Ni<sub>2</sub>Si SCNWs with diameters as low as 34 nm have shown an effective resistivity of  $21 \mu\Omega\text{-cm}$  [5]. Ultra-thin annular coatings of ALD-based NiSi<sub>2</sub> ( $\sim 10$  nm) on Si nanowires also point to bulk-like resistivity ( $\sim 35 \mu\Omega\text{-cm}$ ) [6]. By virtue of their single-crystalline nature, several of these NiSi nanowire stoichiometries have demonstrated maximum current densities nearing or exceeding  $10^7\text{-}10^8$  A/m<sup>2</sup>. Although the stability of bulk-like electrical resistivity in nickel silicide nanowires has been confirmed by several groups, it is only the monosilicide phase in particular that is relevant as a Cu replacement for BEOL processing as it approaches the effective Cu line resistivity at the 11 nm node.

Important demonstrations of top-down nickel monosilicide nanoscale wire processing have also been reported recently and will continue to receive experimental attention. Ni silicidation of patterned Si has yielded effectively single-crystal NiSi wires with widths below 25 nm. Bulk-like resistivity ( $\sim 15 \mu\Omega\text{-cm}$ ) for wires fabricated via this approach for wire widths  $> 50$  nm has been reported [4] while NiSi wire widths  $\leq 30$  nm exhibited a resistivity  $\sim 23 \mu\Omega\text{-cm}$  [7]. In contrast, virtually no change in the measured electrical resistivities of  $19.5 \mu\Omega\text{-cm}$  and  $19.7 \mu\Omega\text{-cm}$  for similarly fabricated NiSi nanowires with cross sections of  $23 \times 31 \text{ nm}^2$  and  $455 \text{ nm} \times 27 \text{ nm}$ , respectively, has been observed [8]. This and the previous work clearly document a relatively low dimension impact factor for NiSi although maintaining a resistivity at or less than  $10 \mu\Omega\text{-cm}$  in a fully processed NiSi interconnect structure has yet to be demonstrated.

### 5.2.2 SILVER

Dimensional effects can substantially increase Ag electrical resistivity in thin films and narrow wire geometries due to its large mean free path ( $\sim 58$  nm) as documented recently in the literature [9-11]. More recent work has confirmed this trend, documenting an average electrical resistivity for single crystal FCC Ag wires of  $11.9 \mu\Omega\text{-cm}$  for wires with average diameters of 40-50 nm [12]. Still, there are examples of nanoscale Ag wires which have exhibited attractive values of electrical resistivity. Sub 100 nm diameter single-crystal Ag nanowires exhibiting a resistivity  $\sim 2.6 \mu\Omega\text{-cm}$  have been demonstrated [13]. Although a relatively large wire diameter, this low value of resistivity indicates a substantial sensitivity to processing and will motivate continued work in Ag nanolines. Due to issues related to FAB introduction and added cost Ag will have to show significant improvement vs. Cu at narrow line dimensions for industry adoption to occur.

### 5.2.3 METALLIC PHONON ENGINEERING

Electron-phonon scattering contributes substantially, 20 to 40%, to electrical resistivity at room temperature and above in narrow dimensions [14, 15]. Although surface scattering is expected to dominate at sub-32 nm wire widths, reduction of electron-phonon scattering should be pursued. Metal quantum wells have been shown to reduce electron-phonon coupling in the proper geometry and material. Ultra-thin (3 nm) Ag films on vanadium substrates have exhibited a reduction in electron-phonon coupling by 38% over bulk Ag [16]. This is expected to translate roughly to a 30% reduction in phonon-induced electrical resistivity or approximately a 10% reduction in total resistivity at room temperature with nominal impact on local density of states and surface scattering [17]. Similarly, 13 nm Ag films on a Cu (111) substrate exhibit a 42% reduction in electron-phonon coupling compared to the bulk [18] holding the same promise for reduction of electrical resistivity. Although imperfect metal-metal interfaces may mask resistivity benefits due to reduced electron-phonon coupling, such multilayer geometries bear continued research.

### 5.2.4 METALLIC GEOMETRIC RESONANCE

Quantum confinement effects are generally deleterious regarding electrical resistivity. Such effects typically enhance electron scattering (whether from surfaces or phonons) due to restriction in density of states or inter-sub-band scattering [17, 19]. These effects result from finite size restrictions on electron quantum-state wave vectors [20]. A distinct type of quantum confinement effect was predicted based on electron surface scattering [21-23]. One implication was the presence of geometric resonances for multilayer films in which a layer interface coincided with a node in the transverse wave function (or its derivative). Several resonances existed for individual layer thicknesses in the range of 1-3 nm, in line with current and future cladding technologies. The end effect is a predicted reduction in inter-sub-band scattering which could enable near-ballistic transport (neglecting phonon-induced scattering). The investigations of such effects will see expansion as more core-shell nanoline geometries are investigated in conventional metallics as an alternative to Cu and carbon-based interconnects.

### 5.2.5 CARBON NANOTUBES

Carbon nanotubes (CNT) have aroused major research interest in their applicability as very-large-scale integration (VLSI) interconnects for future generations of technology because of their desirable properties such as large electron mean free paths, mechanical strength, high thermal conductivity, and large current carrying capacity. CNTs can be either single-wall (SWCNT) or multi-wall (MWCNT). SWCNTs consist of only one graphene shell, and diameters may vary from 0.4 nm to 4 nm with a typical diameter of 1.4 nm [24, 25]. MWCNTs consist of several concentric graphene cylinders, whose outer diameters may vary from a few to 100 nm [25, 26]; the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite [25]. Graphene cylinders, SWCNTs or shells forming MWCNTs, can be either metallic or semiconducting, depending on their geometrical structure (chirality). However, large diameter semiconductor shells ( $D > 5$  nm) have bandgaps comparable to, or smaller than, the thermal energy of electrons and act like conductors at room temperature [25-27].

### ADVANTAGES OF CNTS

CNTs offer several advantages compared to Cu/low- $\kappa$  interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms:

1. *Higher conductivity*— Due to their one-dimensional nature, the phase space for electron scattering in CNTs is limited, and electron mean free path is in the micron range for high quality nanotubes, in contrast to 40 nm in bulk copper [28]. The conductivity of densely-packed CNTs is higher than scaled Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 k $\Omega$  [25, 29].
2. *Resistance to Electromigration*— The strong sp<sup>2</sup> carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs; 10<sup>9</sup> A/cm<sup>2</sup> in contrast to 10<sup>6</sup> A/cm<sup>2</sup> in Cu [30]. In practice, however, contacts may limit the maximum current density in CNT interconnects.
3. *Thermal conductivity*— The longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W/mK, as suggested by theoretical models [31] and extrapolations on measured data from porous bundles [32]. The thermal conduction in CNTs is highly anisotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction.

### CNT INTEGRATION OPTIONS

CNTs can potentially replace Cu/low- $\kappa$  interconnects at most levels of interconnect hierarchy [33] except in places where low-resistance short interconnects are needed e.g., power and ground wires in the first interconnect level. CNTs can be integrated for on-chip interconnect applications in the following forms:

1. *SWCNT-Bundles*—A bundle of densely packed SWCNTs with the same dimensions as Cu/low- $\kappa$  interconnects with high-quality contacts with the electrodes would be an ideal candidate for replacing Cu/low- $\kappa$  interconnects to lower the interconnect resistance and address the problem of size effects in copper wires. This integration option provides significant delay improvement for long interconnects where the RC delay is dominant [24, 33-35].
2. *Few-Layer SWCNT Interconnects*—A few-layer arrangement of SWCNTs can reduce the capacitance of the CNT-based interconnects by as much as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects where the delay is dominated by capacitive loading and not resistance [36].
3. *Large-Diameter MWCNTs*—It has been proven both theoretically and experimentally that all shells within MWCNTs can conduct if proper connections are made to all of them [26, 27, 37]. There are reports of very large mean free paths in high-quality MWCNTs [26, 38], and theoretical models suggest that long large-diameter MWCNTs can potentially outperform Cu and even SWCNTs if the level of disorder in these tubes can be kept as low as those in SWCNTs and all shells can be properly connected to metal contacts [39]. Such MWCNTs would be suitable for semi-global and global interconnects. Recently MWCNT interconnects operating at gigahertz frequency range have been demonstrated. Conductivity of MWCNTs in these experiments, however, has been considerably lower than the theoretical models, mainly because of large defect density and a small ratio of outer to inner diameters [40].

### CNT CHALLENGES

There are numerous technical challenges that remain to be addressed before CNTs can be utilized as interconnects. The important challenges facing CNT integration are the following:

1. *Achieving a high-density integration with CNTs*—CNT-bundles can outperform copper wires in terms of conductivity only if they are dense enough. While dispersed SWCNTs can form dense regular arrays with constant 0.34 nm inter-tube spacing [36], in-place grown CNTs reported to date have been quite sparse. *Table INTC11* gives the minimum densities of metallic SWCNTs required to outperform minimum-size copper wires in terms of conductivity. As technology advances and size effects become more severe for Cu wires, the required minimum density becomes smaller. The material and size of catalyst particles are the key parameters determining diameter and density of nanotubes.  
The diameter of SWCNTs is assumed to be 1 nm, at which the phonon-limited electron mean free path is 1  $\mu\text{m}$  at room temperature [41-43]. Contact resistance is assumed to be less than 10% of the intrinsic resistance of SWCNTs, which means longer bundles can tolerate larger contact resistances. Ideal density for a densely-packed all-metallic bundle of SWCNTs with 1 nm diameter is  $0.66 \text{ nm}^{-2}$ .
2. *Selective growth of metallic SWCNTs*—SWCNT growth processes developed to date cannot control chirality. Statistically, only one third of SWCNTs with random chirality are metallic [25]. Improving the ratio of metallic to semiconductor tubes would proportionally increase the conductivity of SWCNT-bundles. Semiconductor SWCNTs are not fatal for interconnect applications, and in contrast to transistor applications of CNTs, perfect control of chirality is not necessary.
3. *Directional growth in CNTs*—At this time, an especially challenging step is the controlled directional growth of horizontal CNTs. The placement of catalysts on a vertical surface makes directional vertical growth much simpler than directional horizontal growth. The ability to control the angular divergence of horizontally grown CNTs is not sufficient to meet current integration needs, although some progress has been made in this regard [44].
4. *Achieving low-resistance contacts*—The metal electrode contact with CNTs may cause reflection effects and cause contact resistance. These reflections occur due to inefficient coupling of the electron wavefunction from the electrode into the CNT. A promising close-to-ideal contact has been realized experimentally [27, 45] but the large number of publications reporting large contact resistances indicates a technological challenge in making good contacts. Because of the weak inter-tube coupling between SWCNTs in a bundle [36] and also between shells inside MWCNTs [25, 37], direct connections between all graphene shells and metallic contacts are required. CMP for vertical CNT bundles may be the solution for this requirement [46, 4749, 50].

5. *Achieving defect-free CNTs*—CNTs are very sensitive to adsorbed molecules. It is found that adsorbed molecules on the surface of CNTs affect electrical resistance [38, 48] imposing additional technical challenges to producing CNTs acceptable defect-free stable characteristics.
6. *BEOL compatible CNT growth*—Most high-quality CNTs reported in the literature are grown at temperatures above 600°C, which is not acceptable for the silicon technology. Promising progress is reported that involves the growth of CNTs at temperatures as low as 400°C [27]. However, defect density typically increases as growth temperature is lowered. Furthermore, CNT interconnects are unlikely to replace all copper interconnects. CNT interconnect fabrication technology, therefore, needs to be compatible with Cu/low-κ process technology.

Although CNT interconnects have been separately shown to be promising, there have been few efforts to successfully combine them in realistic circuits. There are still several process and reliability related challenges that need to be addressed before CNT-based devices and interconnects can enter mainstream VLSI processing. This makes it an exciting and open field for research. Problems such as purification, separation of carbon nanotubes, control over nanotube length, chirality and desired alignment, high density growth, low thermal budget and high quality contacts are yet to be fully resolved.

*Table INTC11 Minimum Density of Metallic SWCNTs Needed to Exceed Minimum Cu Wire Conductivity*

Year of Production	2011	2012	2013	2014	2015	2016	2017
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	38	32	27	24	21	18.9	16.9
Cu Effective Resistivity ( $\mu\Omega\text{-cm}$ )	4.48	5.00	5.63	6.00	6.61	6.96	7.46
CNT Minimum Density ( $\text{nm}^{-2}$ )	0.160	0.143	0.127	0.119	0.108	0.103	0.096

Year of Production	2018	2019	2020	2021	2022	2023	2024	2025	2026
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	15	13.4	11.9	10.6	9.5	8.4	7.5	6.7	6
Cu Effective Resistivity ( $\mu\Omega\text{-cm}$ )	8.09	8.81	9.74	10.86	11.71	12.75	14.06	15.02	16.00
CNT Minimum Density ( $\text{nm}^{-2}$ )	0.088	0.081	0.073	0.066	0.061	0.056	0.051	0.048	0.045

### 5.2.6 GRAPHENE NANORIBBONS

Graphene, a monolayer of carbon atoms packed in a hexagonal lattice, is a strictly two-dimensional material [49]. Graphene research has advanced rapidly since its first isolation in 2004, thanks to the expertise previously developed by carbon nanotube researchers. Graphene nanoribbons (GNR) can be considered unrolled CNTs, to which their electronic properties are similar. GNRs can be metallic or semiconducting depending on their geometry [50-52]. High-quality graphene sheets may have mean free paths (MFPs) close to those in CNTs [53], and they can conduct large current densities on the order of magnitude reported for SWCNTs [54]. The major advantage of GNRs over CNTs is their more straightforward fabrication processes.

The electronic properties of GNRs are determined by their width and geometry [52]. Tight-binding approximations predict that GNRs whose edges have a zigzag pattern are metallic (zero bandgap) [52]. GNRs with an armchair pattern, on the other hand, are metallic if the number of carbon atoms across their width is  $3p+2$  where  $p$  is an integer. Armchair GNRs with  $3p$  and  $3p+1$  carbon atoms across their width are semiconducting and their bandgaps are inversely proportional to their widths [52]. All of GNRs measured to date are semiconducting and the bandgap varies inversely proportional to the width [53, 55, 56]. The existence of a gap in the bandstructure of all measured GNRs has been mostly attributed to edge roughness [55, 56]. Also, first principle calculations indicate that the spacing of carbon atoms along the edges of armchair GNRs is 3.5% smaller than the spacing between carbon atoms in 2D graphene [57]. This change in lattice constant opens a small gap in the band structure of  $3p+2$  GNRs [57]. Likewise, a gap appears in the band structure of zigzag GNRs, once the spin degree of freedom is considered in first-principles calculations [57].

The fact that metallic GNRs may be unobtainable does not rule out the potential of GNRs as interconnects [58]. The bandgap in semiconducting GNRs is smaller than 0.1eV, even for the 11 nm interconnect width projected for the end of the ITRS [58]. The Fermi energies in graphene layers are often higher than 0.1eV. When the Fermi energy is a few  $k_B T$

larger than half bandgap, the first conduction band becomes adequately populated [58]. For such GNRs, there would be a negligible difference between the ideal conductances of metallic and semiconducting GNRs.

### ADVANTAGES OF GNRs

GNRs offer several advantages compared to Cu/low- $\kappa$  interconnects:

1. *Higher conductivity*—Like carbon nanotubes, the mean free path of electrons in pure high-quality graphene can be quite large. Mean free paths as large as a few hundred nanometers have been reported in graphene [53]. Substrate-induced disorders are believed to be the dominant source of electron scattering and high mobilities corresponding to mean free paths as large as a few micrometers have been reported in the case of suspended graphene [59]. Conductivity of stacks of non-interacting GNRs with smooth edges and Fermi energies above 0.2 eV has been predicted to outperform those of copper wires, especially at small cross-sectional dimensions and long lengths [58].
2. *Resistance to electromigration*—The strong sp<sup>2</sup> carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for GNRs;  $10^9$  A/cm<sup>2</sup> in contrast to  $10^6$  A/cm<sup>2</sup> in Cu [33]. In practice, however, contacts may limit the maximum current density in GNR interconnects.
3. *Thermal conductivity*—The in-plane thermal conductivity of suspended single layer graphene sheets has been measured to be 5300 W/mK [60]. This value is comparable to the highest values reported for SWCNTs bundles [60].

### GNR INTEGRATION OPTIONS

GNRs can potentially be integrated for on-chip interconnect applications in the following two forms:

1. *Many-layer GNR interconnects*—These can potentially be used to lower interconnect resistance, especially at small interconnect dimensions where size effects severely limit conductivity of Cu wires. In the case of Bernal stacking, graphene layers have an ABAB ordered arrangement [61]. In this case, the layers become electronically coupled and form graphite. Graphite lacks the appealing electronic properties of isolated graphene sheets. It is therefore critical to have electronically decoupled layers in multilayer GNRs. Stacking disorders have been reported for epitaxial graphene grown on C-faced 4H-SiC substrates [61] and CVD grown multi-layer graphene films [62].  
The shift in Fermi energy that naturally occurs because of the charge trapped at the graphene-substrate interface is limited to the few graphene layers at the bottom of GNR stacks due to the screening effect [63]. Methods such as edge functionalization [64] must hence be adopted to shift the Fermi energy of all layers in GNR stacks.
2. *Few-layer GNR interconnects*—A few-layer arrangement of GNRs can be used to reduce the capacitance of the GNR-based interconnects by as much as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This is similar to the few layer arrangement of SWCNTs. The reduction in capacitance helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects in which the delay is dominated by capacitive loading and not resistivity.

### GNR CHALLENGES

There are numerous technical challenges that remain to be addressed before CNTs can be utilized as interconnects. The important challenges facing CNT integration are the following:

1. *Graphene synthesis*—Wafer-level synthesis of high-quality graphene sheets on arbitrary substrates remains a major challenge. While epitaxial graphene grown on SiC substrates has the potential for wafer-level growth, it will not be a suitable option for interconnect applications in which graphene ribbons on dielectric materials are needed. Recently, graphene films have been obtained by using bilayer catalyst films (Co and TiN) and CVD at temperatures around 510°C [65]. In this method, multilayer graphene is created on top of vertical multiwall carbon nanotubes. The graphene film obtained is extremely flat with a thickness determined by the thickness of the Co film [65]. Continuous films of graphene have also been grown by ambient pressure CVD on polycrystalline Ni [62]. After wet-etching the Ni film, the CVD-derived films have been successfully transferred to a diverse set of substrates [62]. A similar approach has been taken [66] where CVD grown graphene films on Ni are transferred to Si substrates; films with sheet resistances as small as 280  $\Omega$  per square and mobilities as high as  $3,700 \text{ cm}^2\text{V}^{-1}\text{S}^{-1}$  have been obtained. Wafer-level methods for graphene preparation still lack the uniformity and grain size needed for large scale integration of graphene devices.

2. *Patterning GNRs with smooth edges*—Resistance of a narrow GNR is quite sensitive to edge quality because electrons interact with the edges frequently when the GNR width becomes comparable to the intrinsic mean free path of non-patterned 2D graphene. Since the intrinsic mean free path in graphene can be as large as several hundred nanometers, the effective mean free path is determined by edge scattering for most interconnect widths of interest. The mean free path associated with edge scattering depends on the edge quality (roughness), GNR width, and the ratio of transverse to longitudinal electron speed. Edge roughness determines the backscattering probability at the edges. In chemically obtained GNRs with relatively smooth edges, a backscattering probability of 0.2 has been reported [67] whereas the data from lithographically patterned GNRs indicate a backscattering probability of 1 [50]. The product of GNR width and the ratio of longitudinal to transverse velocity determines the average length electrons move before interacting with edges [50, 67, 68]. Sub-bands further from the Dirac point have smaller longitudinal to transverse velocity ratios and therefore have shorter mean free paths.
3. *Edge functionalization or doping*—The Fermi energy of graphene layers close to the substrate is shifted from the neutral point because of the charge accumulated at the graphene/substrate interface. However, this effect diminishes exponentially for upper layers because of the screening effect [63]. To utilize all layers within a multilayer GNR, the Fermi energy of upper layers must be shifted either through edge functionalization or doping. Otherwise, the conductance of upper levels would become considerably smaller because of their bandgap. This conductance degradation is more severe for narrower GNRs whose bandgap is larger. Edge-functionalization or doping must be done such that the effective mean free path is not adversely affected.
4. *Achieving low-resistance contacts*—Similar to carbon nanotubes, creating reliable low-resistance contacts to GNRs is challenging. For multilayer GNRs, it is desired that the graphene layers be electronically decoupled to preserve the attractive graphene qualities. Therefore, at the contacts, direct electrical connections to all layers in multilayer GNRs are needed.

## 5.3 CMOS-COMPATIBLE OPTICAL INTERCONNECTS AND I/O

### 5.3.1 INTRODUCTION

Optical solutions have been proposed for on-die interconnects (signaling and clock distribution) and Input/Output (I/O). For on-die interconnect applications, because of pitch, delay and power considerations, optical interconnects are not expected to replace Cu/low- $\kappa$  in the lower layers of the interconnect stack. Instead, the focus is on cost efficient implementations that take advantage of the unique properties of optical architectures. For I/O applications, optical solutions focus on increasing the aggregate bandwidth, bandwidth density (bandwidth per cross sectional distance, typically measured as Gb/s/mm), and/or communication distance while decreasing the power per bit by overcoming the limitations imposed by the high losses of package interconnects and by avoiding or minimizing the need for high power equalization and pre-emphasis. In terms of timeline, optical I/O is generally regarded as the most likely first application of this technology. To facilitate the implementation of this technology, development of CMOS-compatible optical components and processes that utilize existing infrastructure is of paramount importance. Although significant progress continues to be made, this area is not yet sufficiently mature for high-volume low-cost solutions to define an intercept to the existing interconnect roadmap.

### 5.3.2 INTEGRATION OPTIONS

#### Optical architectures for on-die optical interconnects:

Most of the architectures that have been proposed for on-die optical interconnects fall in one of the following two categories:

- *Integrated light-source architectures*: in this case direct-modulated light sources and detectors are integrated on the CPU. The main disadvantage is the large on-die power consumption/heat dissipation, and the significant integration challenges.
- *External light-source architectures*: these implementations use off-die light sources on the package or board, and on-die modulators and detectors. The main advantage is that the laser power is off-die. The main disadvantage is the manufacturing complexity and the high coupling losses to bring the light into the chip.

In both cases above, wavelength-specific filters/modulators can be used to implement multiplexing, which enables multiple independent signals transmitted in each waveguide.

#### Expected advantages

- *Delay*: it is possible to define a critical length above which optical interconnects are faster than their metal-dielectric counterpart. The critical length, which depends on the quality of the optical components, has been assessed to be on the order of millimeters [69, 70].

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- *Skew and Jitter*: low latency and the absence of crosstalk in optical interconnects can potentially result in low skew and jitter clock distribution. However, advanced clock distribution designs implemented in conventional metal-dielectric systems are expected to meet microprocessor needs.

Potential disadvantages: power, cost, integration complexity.

Potential usage in the interconnect hierarchy: long interconnects in upper metal layers, core-core communication.

### Optical architectures for I/O

Most of the proposed implementations can be grouped into two basic architectures [71, 72]:

- *On-CPU optical I/O*: in this case, most or all optical components are integrated into the CPU. Part or all of the communications in and out of the CPU are done through optical signals. The light sources can be on-die or off die, and may or may not be directly modulated.
- *Discrete optical I/O die*: an optical I/O chip receives electrical signals from the CPU (via package traces) and transforms them into optical signals. Equivalently, the optical I/O chip receives optical signals that are transformed into electrical signals that are communicated to the CPU using package traces. The light sources are typically off-die, and may or may not be directly modulated.

The main advantage of integrated optical I/O is that it can potentially save power with respect to discrete optical I/O by avoiding the power penalties associated with electrical I/O. On the other hand, discrete architectures remove many challenging design and integration constraints resulting from integrating optical components on the microprocessor die, but instead increase packaging complexity. The expected advantages of the approach include:

High aggregate bandwidth, low power per bit, long-distance communication, removal or minimization of pre-emphasis and equalization. The disadvantages with this approach included both additional cost and system complexity.

### Challenges

Implementation of optical interconnects for signaling, clock distribution and I/O requires development of a number of optical components. Listed below, the most critical components are briefly described.

*Light sources* can be directly modulated or continuous wave (i.e. non-modulated). In the former case, the light source is turned on/off with an electrical signal; in the latter case, a continuous light source is used in conjunction with optical modulators controlled with electrical signals. From a location perspective, lasers can be off-die (package or board), bonded to a photonics die, or integrated on-die (typically adding III-V capabilities to a CMOS platform). Key parameters are output power, power efficiency, number of lasers in an array, cost, thermal stability, electrical tunability (change in wavelength per change in supply voltage), cooling requirements, and speed for the case of directly-modulated sources. Examples of light sources include: Vertical Cavity Surface Emitting Laser (VCSELs); quantum dot lasers, and edge emitting semiconductor diode lasers. The most widely used wavelengths are 850, 1310 and 1550 nm. Typical requirements are switching rates of 20 Gb/s or higher. Total power requirements depend on the application, but are typically below 1 W. Currently, the key concerns include wavelength stability, reliability at operating conditions and cost of laser arrays.

*Photodetectors* can either be integrated on-die, bonded to a CMOS die, or on-package. Ge-based Metal-Semiconductor-Metal and PIN diode photodetectors have received significant attention since they have the potential to be CMOS compatible [73-78]. Key technical parameters include responsivity, operation voltage, input capacitance, light coupling efficiency, dimensions, and ratio of photocurrent to dark current, light coupling efficiency, dimensions. Detectors that take advantage of plasmons to enhance the coupling of light into the photodetector have been recently proposed [79]. Typical requirements on photodetectors are: responsivity greater than 0.4 A/W; bandwidth higher than 20 Gb/s at less than or equal to 1 V and, stable operation up to 100 °C.

*Modulators and filters* are used in combination with continuous light sources. The purpose of the modulator is to control the flow of light using an electrical signal. A wavelength-dependent filter or modulator can be used to introduce multiplexing, which enables the transmission of multiple signals at differing wavelengths in a single waveguide/fiber. A large variety of CMOS compatible modulators have been proposed in the literature, including ring resonators and Mach Zehnders. Modulators utilize electro-optical effects to control the light output using electrical signals, e.g. free-carrier-effect in Si, electro-absorption effects on III-V materials, electro-optical effects in perovskites and polymers. The key performance parameters include insertion loss, operation voltage, operation frequency, switching power, modulation depth/extinction ratio, and area. Typical requirements are bandwidths higher than 20 Gb/s at 1 V or lower; insertion loss below 3 dB; extinction depth greater than 5 dB; operation up to 100 °C. In the case of resonators, one of the challenges is to keep the light source and the modulator locked at the appropriate wavelength, which may require the use of on-chip local heaters, as well as detection systems and control/feedback circuitry, without introducing a significant power penalty. In the case of Mach Zehnders, the key challenges are the large areas used, high switching power, high insertion loss, manufacturing variations, the need for travelling-wave electrodes and precision resistors matched to the electrodes.

*Waveguides* provide the means for light propagation on the chip with minimum losses. They also need to enable “bends” and “turns”, as well as an efficient coupling of the light into the detectors. A large refractive index contrast between the waveguide and the surrounding materials enables tight turn radii and small pitches. On-die waveguides using common CMOS-compatible materials and processes have been extensively reported. Examples include Si, Si<sub>3</sub>N<sub>4</sub>, or Si<sub>3</sub>O<sub>x</sub>N<sub>y</sub> cores on SiO<sub>2</sub> cladding [78]. Key technical parameters include loss per unit length, refractive index contrast, pitch, and bending radii achievable.

*Waveguide-fiber couplers* are used to transition light from a fiber into an on-die waveguide, and vice versa. There are three main coupling approaches: (i) fiber-waveguide butt coupling, where waveguides and fibers are aligned end-to-end; (ii) grating couplers, where the fiber shines light at an angle on a grating structure that focuses it into a planar waveguide; and (iii) evanescent coupling between specially modified fibers and waveguides. In some cases, mirrors and lens arrays are also utilized to enable the coupling. The key figures of merit are coupling efficiency, cost and package alignment tolerances. Insertion losses in couplers can potentially dominate the optical power budget. The main challenge is the development of solutions that provide low insertion losses that do not require tight packaging alignment, in order to reduce assembly costs. *Laser-waveguide couplers* are used to transition light into an on-die waveguide from a laser or laser array that has been bonded onto a photonics die. There are two primary coupling strategies: evanescent coupling and butt coupling. The development of couplers may require custom packaging solutions, which need to be comprehended for a coupling option to be viable.

### 5.3.3 TOPOLOGICAL INSULATORS

Three dimensional topological insulators (3D-TIs) are a new class of materials with a wide range of potential applications, including spintronics and interconnect. From an interconnect perspective the salient features of the material include: graphene-like 2D surface transport with high mobility and linear bands [80, 81]; spin-polarized carrier motion due to high spin-orbit coupling [82]; immunity to backscattering, surface defects and even high level of alloy impurities [83, 84]. Experimentally measured mobility of  $>10^4$  cm<sup>2</sup>/Vs and carrier concentration  $1.4 \times 10^{12}$  cm<sup>-2</sup> are competitive with graphene [85]. As a result it has been suggested that 3D-TIs have potential as a dissipation-free room temperature interconnect material. However, closer review of the theoretical and experimental results shows that the protection of the surface state exists only for *elastic backscattering*, and only as long as the charge carrier energy does not exceed the bulk bandgap and the thickness of the bulk material is larger than ~5nm [86]. Neither inelastic backscattering nor medium-angle elastic scattering are suppressed on the surface of 3D-TIs. Since the dominant loss mechanism in electrical interconnect is inelastic scattering, electrical transport with topological surface states is not expected to offer a benefit over conventional interconnect, graphene, or CNTs. However, the spin-polarized nature of electron motion on the surface TIs holds promise for applications as native interconnect in spintronics applications and should continue to be studied in that context.

### 5.3.4 SUPERCONDUCTORS

The concept of zero resistance obviously has immediate appeal in attempts to minimize RC delay of interconnect systems. This has attracted some attention to the potential application of superconductors for interconnect systems. Unfortunately, there are several inconvenient realities that make the applications of superconductors much less attractive as interconnects. First, the superconductors need to be cooled to approximately 77K to provide reasonable properties, and such cooling solutions are prohibitively expensive. Second, high temperature superconductors typically require high growth temperatures on epitaxial substrates which are not compatible with CMOS integration. Third, the typical critical current densities of high temperature superconductors are in the 1E5 A/cm<sup>2</sup> range [87], which is similar to operating current densities. Fourth, superconductors have an intrinsic frequency dependent conductivity. At 77K, Cu and YBCO have equivalent surface resistances at 150 GHz. At 10 GHz, YBCO has approximately a two order of magnitude lower surface resistance than Cu [88]. Finally, even if R were to go to zero, signal transmission would then be similar to LC transmission lines for which the signal propagation speed would be  $1/\sqrt{LC}$ .

### 5.3.5 WIRELESS INTERCONNECT

Wireless interconnects in integrated circuits use the substrate or substrate in combination with a dielectric layer that can be placed below the substrate for signal propagation. This provides a parallel channel to conventional interconnect layers, but requires additional areas for circuits and antennas as well as accompanying power consumption. Thick Si substrates with typical doping levels generate high losses and associated signal attenuation. The silicon substrate can be thinned below 100 μm to reduce this attenuation. It is also possible to communicate from an off-chip antenna to on-chip antennas through the silicon substrate backside. The antenna size scales down linearly with the operating frequency which can be as high as 25-50% of the peak cut-off frequency,  $f_T$  for transistors. The extinction coefficient also decreases with the

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operating frequency in the limit when the operating frequency times the permittivity is much larger than the conductivity of the substrate. For 20 Ohm-cm substrates, this transition frequency is around 10 GHz. Eventually the dopant related plasma effects increase the extinction coefficient.

The bandwidth of wireless interconnects is limited by the bandwidth of the circuits that can be realized in a given process technology. The bandwidth is 25–50 % of transistor  $f_T$ . With the present CMOS technology, it should be possible to support a data rate of 100–200 Gbps, which makes wireless interconnects better suited for signals with low to moderate bandwidths. The aggregate bandwidth can be increased by dividing space into cells like what is done for cellular phone communications at the cost of increased circuit area and power consumption. Frequency division multiple access and code division multiple access schemes are additional options to increase the number of I/O lines. However, the hardware and power consumption overheads are usually too high compared to using Cu wires for intra-chip applications. Wireless interconnects are better suited for global signals with fan\_outs 10-100 such as global clock, reset, sleep and other moderate bandwidth signals requiring multiple long metal lines. The area for synchronization at given clock frequency and skew tolerance can be increased by radiating clocks through the back side of an integrated circuit from an off-chip antenna.

Inter-chip wireless data communication within a printed circuit board using the free space between a metal cover and a ground plane on a PC board is also possible. The loss of medium is smaller than that of transmission lines on a PC board. Furthermore, since wired interconnects also need a transmitter and receiver, the power consumption and area overhead for wireless interconnects are more tolerable.

### 5.4 Si CMOS REPLACEMENTS AND INTERCONNECT IMPLICATIONS

A diverse set of emerging switches are being pursued to replace Si CMOS devices. Emerging devices offer various advantages and limitations and the most suitable interconnect technology for each device option may be very different. Novel devices can broadly be categorized as field effect and non-field effect switches. In field effect devices, the voltage applied to the gate modulates the height and/or width of potential barrier. A diverse set of emerging devices is being investigated to augment or replace Si CMOS switches. The range of options being explored varies from field-effect transistors made from novel materials such as Si nanowires, carbon nanotubes, and graphene nanoribbons, to more disruptive devices that are based on new computational state variables such as electron spin. As each of these new device concepts are evaluated in terms of their intrinsic properties, their interconnection aspects must be examined as well. Otherwise, the delay and energy overhead associated with interconnects may wash out the intrinsic advantages of these novel devices. This becomes especially important for some emerging devices in which the boundary between device and interconnect blurs when they are made from the same materials (native device interconnects). Carbon nanotubes, graphene nanoribbons, and silicon nanowires are examples of such materials. Also, non-charge based devices should be able to communicate their state variable in a fast and low-energy fashion, at least locally. Otherwise, the circuit, delay and energy overhead needed for signal conversion will be prohibitive. In this section, the interconnect challenges and opportunities offered by native device interconnects are discussed.

#### *Emerging Field Effect Devices*

**Thermionic FETs:** The majority of field effect devices operate based on thermionic emission in which a potential barrier is modulated by the gate voltage. The emerging devices in this category either use new channel materials with higher mobilities, offer a better electrostatic coupling between the gate and channel, or a combination of both. Such transistors will offer higher  $I_{on}$  (lower output resistances) and lower input parasitic capacitances. Interconnect resistance and capacitance values will hence become more important for such replacement.

**Steep Sub-Threshold FETs:** A major class of emerging FETs do not rely on thermionic emission of carriers and are hence not limited by 60mV/dec subthreshold swings. For instance, in tunneling FETs, the field applied by gate modulates the width of a potential barrier to control the current. Such devices are expected to outperform Si CMOS at low operating voltages where they both tend to have large output resistances. The large output resistance of low-voltage CMOS and emerging devices with steep subthreshold will make interconnect resistance significantly less important. Hence, interconnect technologies or geometries that offer the smallest possible interconnect capacitance will be most suitable for such high resistance devices.

**Nanoelectromechanical Switches:** They operate similar to conventional relays. The output resistances of such switches tend to be small, and they have little or no leakage current. However, the delay is dominated by mechanical movements not by the RC charge up times. Designers have proposed new circuit styles with complex gates in which many devices

may switch in parallel and the mechanical delays switches can be partially masked. From the speed point of view, interconnect resistance and capacitance values will not be important for such circuits. However, from energy standpoint, interconnect capacitance will affect power dissipation. Furthermore, using circuit design styles with large fan-out can result in larger overall interconnect length and wiring density might become a primary driver for interconnect technology optimization.

**Atomic or Molecular Switches** are still at their infancy stage. In general, one can expect very large output resistances and small parasitic capacitances for molecular switches. As such, interconnect technology options with the smallest capacitance will be most suitable for molecular switches and interconnect resistance will be a secondary concern.

**Spin Devices:** Spin FETs and spin MOSFETs use electron spin as an internal switching mechanism. However, from input and output standpoint they resemble other FETs in which the gate voltage controls the current flow from the source to drain. Interconnect implications of such devices will depend on their output resistance and input capacitance.

### **Emerging non-Field Effect Devices**

All field-effect switches are expected to eventually face the same power dissipation limit imposed by thermal noise [89]. To overcome the power barrier, state variables other than electronic charge are being explored to invent new devices that can augment or even replace CMOS nanoelectronics [90-93]. Some examples of novel state variables are electron spin, presence or absence of electron-hole pairs called excitons, and pseudospin in graphene [92, 94].

**All Spin Logic:** An all-spin logic based on ferromagnetic elements/tunneling junctions and bistable nanomagnets has been proposed in [95]. It is proven that this logic technology has the five required capabilities for information processing: concatenability, non-linearity, feedback elimination, gain and a complete set of Boolean operations [95]. In this logic, spin polarized currents are injected into a non-magnetic channels using nanomagnet contacts. The change in spin concentration in the channel toggle the magnetic orientation of other nanomagnets. In this kind of logic or any other technology where input and output are both represented by the spin degree of freedom for electrons or holes, spin information can be communicated via drift and/or diffusion, or in ballistic fashion. The key advantage of such interconnects will be that interconnect capacitance may not charge or discharge with information transfer and these interconnect may potentially dissipate less power as compared to electrical interconnects. However, drift and diffusion based interconnects are generally slow especially if interconnects become long. Furthermore, spin relaxation length is finite and in the order of few micrometers. If interconnects are longer than the spin relaxation lengths the signal length will experience exponential decay.

**Spin Wave Devices:** It has been demonstrated recently that spin waves can be used to transfer information in spin-based logic [96, 97]. A spin wave is a collective oscillation of spins in an ordered spin lattice around the direction of magnetization. The strength of exchange interaction between neighboring spins in the magnetic material determines the upper bound of spin wave velocity in the ferromagnetic material. The spin wave velocity does not exceed  $10^5$  m/s in experimentally studied materials such as Fe and Co (with high Curie temperatures) [97]. For a spin-wave bus implemented with NiFe, the maximum group velocity of the magnetostatic wave propagation mode is  $10^4$  m/s in the GHz frequency range, and it continually decreases at higher frequencies [97]. Thus, spin waves are also slow compared to electrical interconnects.

### **5.4.1 TRANSPORT MECHANISMS FOR SICMOS REPLACEMENTS**

Various computational state variables may potentially be communicated with different transport mechanisms depending on their nature and the medium and material used as interconnects. All FETs including Si CMOS use voltage as information token and conventionally RC interconnects propagate voltaic data through diffusion. The delay for a diffusive interconnect is proportional to  $L^2/D$ , where L is length and D is diffusion constant. The diffusion coefficient for a distributed RC network is  $1/r_{im}c_{im}$  where  $r_{im}$  and  $c_{im}$  are per unit length resistance and capacitance values, respectively. Voltaic signals may also be transmitted through electromagnetic waves through LC networks for which delay is proportional to  $L/c_0$  where  $c_0$  is the speed of light in a dielectric. Such interconnects are often found at the package and board levels and rarely at the top on-chip metal levels used as global interconnects. Ballistic conductors may also provide interconnects with delays linearly proportional to length. In a ballistic conductor, electrons experience little or no scattering and interconnect resistance is dominated by quantum resistance,  $R_Q$ . The delay in a ballistic conductor transmitting voltaic signals is proportional to  $R_Q c_{im} L$ , where  $R_Q$  depends on the number of conduction channels ( $\approx 12.9K\Omega/N_{chan}$ ). The quantum resistance is the result of the mismatch in the number of conduction channels in the quantum conductor and the conventional 3D contacts. In the case of native ballistic interconnects in which there is no

such mismatch between interconnects and devices, the quantum resistance term disappears and the delay becomes proportional to  $R_{on}c_{int}L$ , where  $R_{on}$  is the on resistance of the device.

Non-voltaic information tokens may also be communicated with various transport mechanisms. Those that are associated with carriers such as electron spin, can be communicated through diffusion, drift, or in a ballistic fashion [93]. These transport mechanisms may or may not involve net charge transfer. For instance, if at the transmitter side, electrons with a certain spin orientation are injected and the same number of electrons with opposite spin orientation are removed, no net charge will be added to or removed from the interconnect and hence no voltaic signal will be created. However, a concentration gradient in spin density is created which will diffuse to the other end of the interconnect. Non-local spin valves operate based on this principle. The diffusion coefficient for this kind of interconnect is the diffusion coefficient of electrons within the interconnect and is often considerably smaller than  $1/(r_{int}c_{int})$  of voltaic RC interconnects. If a voltage is applied between a spin driver and the corresponding receiver, electrons will move with an average drift velocity and the delay for such drift-based interconnect becomes proportional to  $L^2/(V\mu)$  where  $\mu$  is mobility and  $V$  is the applied voltage. A representative case is a conventional spin valve. If the interconnect conductor is ballistic, electrons experience little or no scatterings and they move with the Fermi velocity,  $v_f$ . For such interconnects, delay becomes proportional to  $L/v_f$ .

It should be noted that voltaic and spin based diffusive interconnects may have orders of magnitude different speeds because the diffusion coefficients are fundamentally different. In voltaic interconnects, the signal often propagates faster than carriers themselves. Likewise, the propagation velocities for voltaic and spin-based ballistic interconnects can be very different.

Spin information may also be transmitted by means of spin waves without moving electrons. A spin wave is a collection of precession of electron magnetic moment about a magnetic field. Spin waveguides can be made of magnetic films, a wire or a combination of wires made of ferromagnetic films, anti-ferromagnetic materials or ferrite materials. The signal propagation speed of spin wave depends on factors such as the waveguide material and structure, spin-wave frequency and the magnitude and direction of external magnetic field. The delay of spin wave interconnects can be given as  $L/v_{SW}$  where  $v_{SW}$  is the propagation velocity of spin waves in the material.

The power dissipation for non-voltaic interconnects can strongly depend on drivers and receivers. For instance, no energy will be dissipated within a ballistic or diffusion-based spintronic interconnect because the net charge in the interconnect remains constant. Power dissipation is therefore determined by the minimum spin current needed by the receiver, the spin relaxation rate along the interconnect, spin injection efficiency at the driver side, and the electrical resistance of the driving circuit [93]. Figure INTC25 shows a comparison at the 14nm node for the delay versus length for different transport mechanisms.

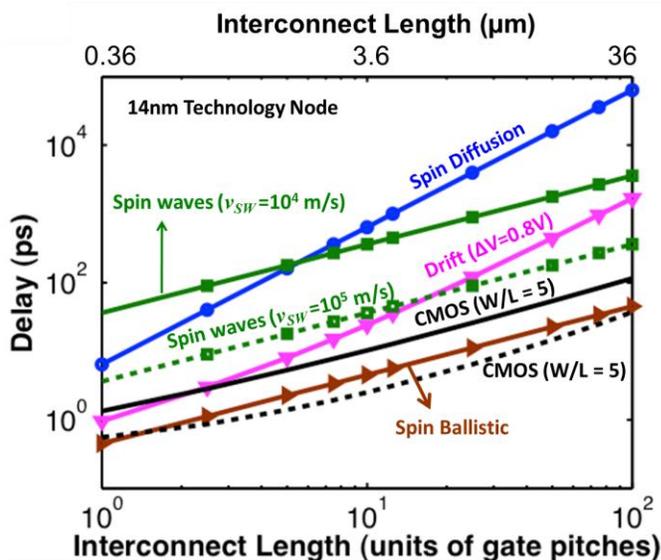


Figure INTC25 Delay versus length for different transport mechanisms.

### 5.4.2 NANOWIRES

Nanowires made from semiconducting materials such as Si and Ge can be locally doped or metallicized to form metal-semiconductor heterostructures. Such structures are especially useful in crossbar architectures in which molecular devices (e.g., diodes) are formed at the intersection of two orthogonal sets of nanowires [98]. Lithographically patterned wires are then used to address individual nanowires that have unique active profiles. The major advantage of crossbar architectures is high packing density, however, they are typically slow. Doped semiconductor nanowires are quite resistive (around hundreds of kilo-Ohms per micron) and can be used only for short lengths. Metallic nanowires such as single crystal NiSi, instead, are considerably better conductors with resistivities around  $9 \mu\Omega\text{-cm}$  [99]. Metallic-semiconducting NiSi-Si heterostructures are created by selectively coating Si nanowires with Ni and annealing them at elevated temperatures ( $\sim 550^\circ\text{C}$ ). The remaining Ni is later etched away, and pure single-crystal NiSi nanowires are obtained. The effective mean free path in single-crystal NiSi nanowires is around 5 nm; because of this, size effects are expected to be modest even in diameters as small as 10 nm [99]. Also, due to their single-crystal nature, NiSi nanowires can conduct current densities as large as  $3 \times 10^8 \text{ A/cm}^2$ .

### 5.4.3 CARBON NANOTUBES

Single-wall carbon nanotubes are quasi 1D materials. At any point in which SWCNTs are interfaced by 3D metallic contacts, extra quantum and contact resistances are introduced. While contact resistance can potentially be lowered by better metal-nanotube interfaces, quantum resistance is a fundamental limit that is unavoidable ( $6.5 \text{ k}\Omega$  for metallic SWNTs). Implementing multiple switches on the same carbon nanotube is an attractive option as it eliminates the extra quantum and contact resistances. In theory, chirality or diameter of a single nanotube can change along its length to form metal-semiconductor junctions. However, it is quite unlikely that this can be done in a controllable fashion as little progress has been made on chirality control. A more practical approach is chemically or electrostatically doping certain regions to form such junctions and connect multiple nanotube switches in a seamless fashion. Chemical doping can degrade the mean free path if the dopants change  $sp^2$  bonds to  $sp^3$ ; dopants that can keep the  $sp^2$  bonding can preserve the large mean free path.

CNT-CNT junctions tend to be highly resistive (many mega Ohms) because electrons have to tunnel between nanotubes. This makes it necessary to use metallic contacts any time a fan-out is needed. Native CNT interconnects are thus useful mainly within logic gates, especially for gates that need multiple switches in series. Examples are multiple-input NAND and NOR gates. Potential performance of such gates, considering possible misalignment of some tubes, has been modeled [100].

### 5.4.4 GRAPHENE NANORIBBONS

GNRs can be considered as unrolled CNTs and have many electronic properties in common with CNTs. The bandgap in a GNR is determined by its width and edge geometry, and can therefore be controlled through proper patterning. This, in principle, provides a big advantage for GNRs over CNTs whose chirality cannot be controlled. A series of semiconductor-metal GNRs can be patterned by varying width along a GNR to form a complex of logic gates with the use of only a few graphene to metal contacts. Wide regions along a GNR have smaller bandgaps that, with the proper choice of Fermi energy, can be made conductive. The choices of widths and lengths for each region should be made properly since the eigenstates in the wide regions can penetrate into the narrow regions and destroy the semiconducting property of the narrow regions. To obtain adequately large bandgaps in GNRs, sub 5 nm widths are needed. This makes patterning nanoribbons a major challenge. Like carbon nanotubes, local doping, both chemically and electrostatically, can be used to form series of semiconductor-metal junctions in GNRs.

Bends and turns can be implemented in GNR circuits. However, if the overall length is short and a GNR operates in the ballistic transport regime, sharp bends and any sudden change in the number of conduction channels along the length of the GNR can reflect electrons and introduce large resistances [101]. This is due to the fact that a ballistic GNR behaves like a waveguide for electron waves. In the diffusive regime, however, GNR behavior is similar to a conventional conductor.

Fan-out in a GNR circuit can be done without the need for metal to graphene contacts, which is another advantage over CNT circuits. This is especially true for the diffusive regime. In the ballistic regime, the wave properties of electrons need to be taken into account, and special layouts may be required to avoid large electron reflections. While GNRs offer more flexibility in terms of layout, there is little routability within a single graphene sheet and other interconnect levels are

needed for making most logic gates. These interconnect levels can be metallic or carbon-based. However, metallic vias are needed to interconnect these levels.

It should be noted that field-effect graphene transistors are not the only device options being pursued. Novel properties of graphene offer opportunities for new device concepts. Examples are devices based on electron spin (spintronics), electron pseudo-spin (valleytronics), and electron wave interference. These new device concepts will offer their own interconnection challenges and opportunities.

### 5.4.5 SPIN-BASED INTERCONNECTS

All devices whose computational state variable is electric charge suffer from the limitations imposed by energy dissipation of charging and discharging capacitances associated with devices and interconnects [102]. Spin is one of the novel state variables being pursued to achieve ultra low-power circuits [103-105]. Spintronics refers to the control and manipulation of the spin degree of freedom of one or a group of electrons, or electron-hole pairs called excitons. Potential advantages of spintronics are non-volatility, increased data processing speed, decreased power consumption, and increased integration density [106]. These potential advantages can be materialized only if spin is used as both input and output for spin-based logic devices [104]. Otherwise, if spin is solely used to control electric current (spin transistor) it will face the same scaling limits as charged based devices [104]. Fast low-power spin-based interconnects are therefore key in developing spin-based circuits which may potentially outperform their conventional counterpart.

Spin signals can be communicated by physical displacement of electrons or excitons carrying the spin information or through spin waves. Carriers can be moved around using electric field (drift) or taking advantage of concentration gradients (diffusion). Excitons have zero net charges and can be moved around by an electric field only if electrons and holes are in separate layers (indirect excitons) e.g., in bi-layer graphene [107]. The use of electric field to move carriers comes with an energy penalty and may result in stand-by power dissipation. Diffusion, on the other hand, can be used for both charged and non-charged carriers. It is a passive phenomenon and can hence be favorable in terms of energy dissipation. Diffusion, however, is a slow process and can limit the speed of diffusion-based interconnects. This low speed must be compensated by a large reduction in power dissipation. Spin relaxation is also an important parameter that limits the length of spin-based interconnects. Spin relaxation length varies in different materials and is typically below a micron. In graphene, spin relaxation lengths as large as 2 micrometers at room temperature have been reported [108], and progress in graphene synthesis is expected to offer higher spin relaxation lengths [108].

It has been demonstrated recently that spin waves can be used to transfer information in spin-based logic [96, 97]. A spin wave is a collective oscillation of spins in an ordered spin lattice around the direction of magnetization. The strength of exchange interaction between neighboring spins in the magnetic material determines the upper bound of spin wave velocity in the ferromagnetic material. The spin wave velocity does not exceed  $10^5$  m/s in experimentally studied materials such as Fe and Co (with high Curie temperatures) [97]. For a spin-wave bus implemented with NiFe, the maximum group velocity of the magnetostatic wave propagation mode is  $10^4$  m/s in the GHz frequency range, and it continually decreases at higher frequencies [97]. Thus, spin waves are also slow compared to electrical interconnects.

## 6 CROSSCUT CHALLENGES

### 6.1 ESH

Globally, chemical regulations continue to evolve with increasing emphasis on evaluation of chemical risks to humans and the environment and restriction of marketing and use of those chemicals deemed most hazardous. By the middle of the decade, an entirely new interconnect materials set may begin to emerge, including non-metallic conductors (likely based on carbon nanomaterials technology) and air-gap dielectrics. Thus, new families of chemicals, materials and process emissions will need to be examined for ESH concerns – especially given the incomplete current definition of the ESH properties of nanomaterials. It is important that all new materials be assessed from an ESH perspective during the basic research and manufacturing process development phases and that the most “green” solutions be chosen which also meets technology requirements. Due to increasing global chemical regulations which may restrict or ban use of a chemical, it is imperative to incorporate ESH assessments in the early in the research and development cycle.

Finally, with such a dramatic shift in interconnect films, there is potential for additive processing. This is a radical shift from decades of lithography-based subtractive processing, but the ESH benefits which would be obtained, along with the process simplification advantages, should be substantial.

The increasing use of planarization presents particular issues both in consumables (e.g., slurries, pads, and brushes), as well as in major chemicals and water use. Efforts should be made to develop planarization processes that will reduce overall water consumption. Water recycling and reclamation for planarization and post-planarization cleans is a potential solution for water use reduction. Advanced CMP slurries may contain nanoparticles that are beginning to be regulated and pose unknown ESH concerns. It is important to understand the environmental fate and impacts of these nanomaterials and how best to minimize exposures to people and the environment.

High GWP (global warming potential) fluorinated greenhouse gases (F-gases) are used extensively in interconnect plasma etch and chamber clean applications. Another high GWP process chemical is  $N_2O$  (used in oxynitride deposition processes). The industry is moving from an era of voluntary greenhouse gas emissions reporting and reduction into a regulatory era. To improve the accuracy of GHG emissions estimates, industry must characterize GHG emissions from interconnect processes. As 450mm equipment sets and processes are developed, emissions characterization should be an essential part of their development. For chamber cleaning, processes that minimize emissions of F-gases have been implemented; note, however, that the residues of carbon-containing low- $\kappa$  films which are removed using fluorinated cleans can produce F-gas emissions (e.g.,  $CF_4$ ,  $C_2F_6$ ) as byproducts. At present, plasma etch processes for dielectrics are all based on F-gases and so F-gas emissions as either byproducts or unreacted starting compounds must be managed. The semiconductor industry's near-term goal has established a goal to reduce normalized F-gas emissions 30% from the 2010 baseline by 2020. To achieve this goal and to ensure that these chemicals remain available for industry use, the industry must continue to reduce process GHG emissions by process optimization, alternative chemistries, and/or abatement. Fluorinated heat transfer fluids also have high global warming potentials, and these materials' emissions must be minimized. With the emergence and expected rapid growth of chip-to-chip interconnects (commonly referred to as 3D technology), a new source of substantial F-gas use has appeared, with processes based on sulfur hexafluoride in development for TSV etch. This new application will place even greater demands on the industry and their efforts to meet the new F-gas reduction goal. It is imperative that emissions from TSV etch processes be characterized so that emission factors can be established. Additionally, TSV etch processes must be developed that minimize F-gas use and emissions while still meeting technology requirements. To meet expected energy conservation goals, equipment (PECVD, dry etch, and CMP) power requirements must be minimized. These goals should include reducing support equipment energy consumption. Plasma processes are both energy-intensive and inefficient in the way they use input chemistries (e.g., often achieving only 10–30% dissociation, by design, in etch processes). Future generation tools will require R&D in low energy-consuming plasma systems. Etchers and CVD tools use point-of-use (POU) chillers and heat exchangers to maintain wafer and chamber temperatures in a vacuum. More efficient heating and cooling control systems (including eliminating simultaneous heating and cooling for temperature control devices) could help decrease energy use and improve control. Greater use of cooling water to remove heat from equipment, rather than dissipating heat into the cleanroom, results in fab energy savings.

Potential solutions for interconnect include additive processing, low ESH impact CMP processes (e.g., slurry recycle or slurry-less CMP), non-F-gas emitting TSV etch, low cost/high efficiency plasma etch emissions abatement, low temperature wafer cleaning, reduced volume process chambers for CVD and ALD, improved ALD process throughput (to reduce resource requirements), vacuum pumping with process-tool-demand-based speed control, reduced dependencies on high temperatures (both internal and external to the processes), and implementation of variable modulation for heating and cooling devices.

## 6.2 CHIP-PACKAGE-INTERACTION (CPI)

In traditional multilevel interconnect schemes there are Al or Cu interconnects which are embedded in conventional dielectric stacks such as  $SiO_2$ , SiN, SiC and/or SiCN. Even with these standard materials in a conventional flow managing the CPI with continual scaling becomes more challenging. Independent of the approach; wirebond, flipchip, C4, advanced scale, or wafer level packaging, stresses are induced by differences in coefficient of thermal expansion (CTE) between the chip and organic substrates or other package materials. Additionally, microcracks and delaminations can be induced during die-prep processes like saw dicing, wafer thinning, and wire bonding and probing. In order to mitigate these induced stresses several countermeasures have been introduced. For example, introduction of polyimide and thick metal layers help to buffer the stresses between the package and the chip. Specific design rules and the use of keep out zones at the chip corners also are effective countermeasures. Further, introduction of crack stop rings at the periphery of the chips edge and sophisticated bond pad construction and optimized placement all contribute to minimize likelihood of cracks and delamination within the system.

In today's most advanced multilevel Cu/low- $\kappa$  interconnect layers, the introduction of mechanically weak low- $\kappa$  and porous ultra low- $\kappa$  (ULK) dielectrics aggravates the critical interaction between on-chip interconnects and the subsequent

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assembly and packaging processes [1-3]. This is a consequence of some very unfavorable properties of the low- $\kappa$  and ULK materials. Low Young's modulus, hardness, reduced cohesion, higher CTE, poor adhesion, increased moisture uptake and reduced thermal conductivity all contribute to degraded chip-package interactions.

From an assembly and packaging perspective the above mentioned low- $\kappa$  and ULK properties are significantly worse compared to the respective properties of traditional interconnect dielectrics, like Si-oxide, Si-nitride or the SiC or SiCN materials. In addition we need to comply with lead-free solders for flip-chip, innovative Cu-pillar approaches and new wafer-level packages and SiP-architectures. Therefore it is necessary to develop and use

- On-chip stress buffers using optimized final passivation schemes & polyimide layer stacks [4].
- New packaging materials with mechanical properties compatible with new low- $\kappa$  and ULK dielectrics
- Laser pre-scribe before saw dicing to reduce saw induced cracks
- Introduction of partly sacrificial seal rings to avoid moisture penetration and crack propagation into the active chip area [5-7].
- Pad-enforcements and / or introduction of mechanical support structures [4].
- Optimized under bump metallization (UBM)
- Gentle or even contact less probing concepts
- Additional low- $\kappa$  / ULK specific design and layout restrictions
- Test structures and test chips sensitive to new CPI issues originating from low- $\kappa$  / ULK materials
- Quick turnaround methods and monitors for early CPI screening of new interconnect materials and integration schemes even before fully integrated BEOL stacks are available for assembly and testing
- Improved test methods for CPI reliability

All the above mentioned developments and optimizations need to be supported by a rather complex thermo-mechanical modeling and simulation of the chip-package-board interaction (CPBI). Typically these FE models to calculate CPBI stresses are set-up in different levels of granularity [8, 9].

- 1) Package-board level addressing the stress between the chip-package, the solder ball connections and the printed circuit board (dimensions of several mm)
- 2) Chip-package level calculating the package stress between the chip, the connecting flip-chip bumps or Cu-pillars and the package substrate, e.g. organic substrate or Si-interposers (dimensions several 100  $\mu\text{m}$ )
- 3) On-chip interconnect level addressing the package related stresses within the Cu/low- $\kappa$  interconnect stack in order to determine crack driving forces, the high stress points and the most likely failure locations (dimensions several  $\mu\text{m}$  or even less).

Obviously this CPBI modeling and simulation is a quite demanding task and needs many new developments and support from the software vendors.

Overall, in order to manufacture successful, innovative, and reliable products in the most advanced technology nodes of today and in the future, much more constructive interaction and collaboration is needed between experts from many different areas of expertise. Teams consisting of designers, FEOL, BEOL, assembly and test engineers must work together with material and tool suppliers in order to successfully navigate the challenges faced by the industry not just from continued scaling but also for the introduction of new 3D architectures. To aid the industry new advanced modeling and simulation will be required to elucidate possible issues early in design phases. Additionally, advanced and novel metrologies and failure analysis will be needed to effectively determine areas of concern early in development cycles. Finally, as in the past, an eye will have to be kept on yield and reliability directly translating to overall system costs and thus ultimate success.

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## 7 APPENDICES

### 7.1 PASSIVE DEVICES

An important challenge for current and future interconnect architectures is the inclusion of precision on-chip passive elements, like high quality capacitors, inductors, resistors and other components into the metallization scheme. This demand is mainly driven by advanced mixed-signal, RF and system-on-a-chip (SoC) applications and is addressed in the standard CMOS platform and foundry technology offerings [1-4, 42, 61-65, 81, 82]. The traditional way to realize passive circuit elements (e.g. capacitors, resistors) on ICs was the integration during front end processing. In this case doped monocrystalline Si substrate, polycrystalline Si and the respective Si-oxides or Si-oxynitrides are used. Because of their close vicinity to the Si substrate, those passive devices fabricated during front end processing suffer increased performance degradation, especially when used at high RF frequencies. Therefore, we see an increasing demand for low loss, low parasitics, but high quality passive devices in the interconnect levels. For interconnect integration the key challenge is to achieve this goal in a modular and cost effective way, without sacrificing the overall interconnect performance and reliability. Basically there are two different approaches for the passive integration. The first approach is the introduction of optional interconnect levels and new materials to accomplish the necessary functions and attributes with the highest performance, the highest quality factors Q and the lowest chip area consumption. The second approach is to realize the passive devices simply by design measures and by using the native properties of existing interconnect levels and materials. This second approach has typically significant cost advantages in the wafer manufacturing process, because no additional process steps are necessary, but suffers in many cases from reduced performance and Q-factors and from increased chip area consumption.

In any case excellent matching properties and the reduction and control of substrate coupling noise and other parasitics are the most important tasks for mixed signal and RF CMOS applications. For the most widely used passive devices, like capacitors, resistors and inductors, the expected future requirements at the different technology nodes of analog, mixed-signal and RF products can be found in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter.

In the following, we will briefly discuss typical applications, requirements and integration challenges of capacitors (MIM and intermetal), inductors and resistors. Published examples of new and innovative approaches to realize passive devices in the interconnect stack will be highlighted as well.

#### 7.1.1 CAPACITORS

*Applications in CMOS, BICMOS and Bipolar chips*

- Decoupling capacitors for MPUs used to reduce the transient currents across the on-chip voltage/ground-interconnects and the chip-to-package interconnects during the switching cycles of the CMOS circuits.
- RF coupling and RF bypass capacitors, in high frequency oscillator and resonator circuits and in matching networks.
- Filter and analog capacitors in high performance mixed-signal products, e.g. A/D or D/A converters.
- Storage capacitors in DRAM and embedded DRAM / logic devices.

*Typical capacitor requirements*

- Small feature size and high charge storage density.
- Low leakage currents and dielectric loss.
- High dielectric breakdown voltage and TDDB reliability.
- High precision of absolute and/or relative capacitance between neighboring capacitors on the same chip.
- High linearity over broad voltage range (low voltage coefficients).
- Small temperature dependence (small temperature coefficients).

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- Low parasitic capacitance.
- Low resistivity of the electrodes and wiring to allow high switching speeds with high Q values, but without excessive heating.

### *Process integration challenges*

#### *a) MIM capacitors*

- Very thin high quality dielectric films with excellent thickness uniformity and control.
- Preferably high k dielectric films in order to reduce the capacitor size. Compare the *Dielectric Potential Solutions* figure for suitable materials.
- Low defect densities for dielectric and metal films (low surface roughness).
- Low deposition temperatures (< 450°C) to be compatible with overall metallization requirements, especially when low-κ intermetal dielectrics are utilized.
- Smart modular integration schemes making optimal use of existing metal levels in order to reduce overall costs, i.e. the number of additional process steps and optional lithography levels.
- Realization of MIM capacitors in the upper metal levels to reduce parasitic substrate coupling and to maintain high Q values. The use of low-κ intermetal dielectrics in the metal levels below should also be beneficial, but may introduce other integration challenges.

#### *b) Intermetal capacitors ('native', MOM, VPP, VNCAP)*

- Aggressive interconnect design rules (narrow lines and spaces, small via height).
- Tight alignment/overlay tolerance between the metal and via levels of the capacitor stack.
- Tight thickness and CD control with minimal line edge roughness of the metal lines.
- Low defect densities for intermetal dielectrics (e.g. porous low-κ) and metal films.
- Low etch and CMP damage in the dielectric films, especially for porous low-κ films.

Successful realizations of MIM capacitors can be found in the literature for Al- based and Cu- based metallizations as well [1-5, 6-8, 18, 19]. Today most MIM capacitors in manufacturing are using silicon oxide, silicon oxynitride or silicon nitride as MIM dielectrics with sufficient material properties, reasonably good RF performance and easy integration into Al- or Cu-based interconnect technologies [47]. Different MIM capacitor architectures, single and stacked approaches, were realized and characterized in a 130 nm multi-level Cu interconnect technology [48]. A very interesting approach of a large area on-chip MIM decoupling capacitor (> 250 nF) with a triple dielectric stack of HfO<sub>2</sub>/Ta<sub>2</sub>O<sub>5</sub>/HfO<sub>2</sub> with TaN electrodes (~ 8 fF/μm<sup>2</sup>) has been demonstrated for a 90 nm SOI microprocessor technology [49, 66]. On-chip MIM power-ground plane capacitor structures with high k dielectrics are expected to significantly improve scaling problems for global interconnects like IR drop, di/dt noise, clock wire latency as well as signal delay and energy per bit for global signal wires [78].

Several papers are published with promising data on the integration of interconnect compatible high k MIM dielectrics (e.g. Al<sub>2</sub>O<sub>3</sub>, Ta<sub>2</sub>O<sub>5</sub>, HfO<sub>2</sub>, Nb<sub>2</sub>O<sub>5</sub>, TiTaO, TiSiO<sub>4</sub>, TaZrO, BST, STO, TiLaO, TiO<sub>2</sub>, Bi<sub>5</sub>Nb<sub>3</sub>O<sub>15</sub>) [3, 20-24, 37, 38, 50-55, 71-74]. The high k MIM dielectrics are deposited either by PVD followed by an appropriate anneal or by CVD and especially Atomic Layer CVD processes keeping the overall temperature budget typically below 400-450°C. However, not all approaches with record breaking capacitance densities may be useful from a leakage current, voltage- & temperature-linearity or dielectric TDDB reliability point of view. Recently laminated (multi-layered) films of different high k MIM dielectrics are proposed in order to overcome these problems [37, 39-41, 50]. By proper work-function tuning of the electrode material (i.e. replacing TaN by Ni) a significant reduction of the leakage current was observed for a MIM capacitor with STO high k dielectric [54].

An innovative 3D damascene MIM capacitor architecture with 17 fF/μm<sup>2</sup> capacitance density was demonstrated by using a PEALD TiN/Ta<sub>2</sub>O<sub>5</sub>/TiN electrode/dielectric/electrode stack embedded in a multilevel Cu metallization with only one added mask compared to the standard process flow [67-69]. In an extended study of this 3D MIM concept combining the Ta<sub>2</sub>O<sub>5</sub> dielectric with other PEALD high k dielectric materials like ZrO<sub>2</sub>, HfO<sub>2</sub>, and Al<sub>2</sub>O<sub>3</sub> even higher capacitance densities up to 30 fF/μm<sup>2</sup> were achieved [69].

A totally different approach of an ultra-thin MIM capacitor stack, making use of the underlying Cu interconnect as bottom electrode (approx. 100 nm total thickness, 10 nm SiN dielectric, 6.3 fF/μm<sup>2</sup>) fitting even between two scaled down Cu

interconnect layers, was demonstrated with promising voltage and temperature linearity and  $> 10$  years of TDDB reliability [70].

The manufacturing of MIM capacitors with high capacitance density, high quality Q, good reliability and low additional cost is a real challenge. Therefore in many applications simply the parasitic or native capacitance of horizontal or vertical parallel plates or comb and finger like structures in different metal levels are used to realize an integrated intermetal capacitor with somewhat reduced area capacitance density [25, 26, 34, 81]. In this approach chip area is traded in versus a reduction in process complexity and manufacturing cost. The big benefit of the intermetal capacitors is that they can be realized and optimized by design and layout measures only without any modification of the wafer manufacturing process. The continued scaling of the on-chip interconnects and the increasing number of interconnect layers in current and future CMOS technology nodes makes the intermetal or natural capacitors more and more competitive, even from a capacitance density per chip area perspective. For the 65nm and 45nm technology nodes native capacitors with good linearity, TDDB robustness and capacitance densities  $> 2 \text{ fF}/\mu\text{m}^2$  and Q-factors  $> 20$  at 1 GHz are reported [75-77], while for the 32nm node capacitance densities even above  $4 \text{ fF}/\mu\text{m}^2$  are predicted [63]. Also for the 32nm node MOM metal finger capacitors with Q-factors  $> 100$  up to 10 GHz frequencies were reported [81]. Based on these promising results, today intermetal capacitors are part of the standard offerings in CMOS platform and foundry technologies for the 65nm node and beyond.

### 7.1.2 INDUCTORS

*Applications of on-chip inductors, especially in RF circuits*

- Impedance matching between different building blocks in today's microwave RF circuits. With increasing frequencies the on-chip inductors will gain even more in importance in the future [9-11].
- RF transceivers
- Filters
- Voltage controlled oscillators (VCO)
- Power amplifiers and low noise amplifiers (LNA)

*Typical inductor requirements*

- High quality factors Q at high inductance. Increasing inductance typically results in reduced quality factors Q.
- High self-resonant frequency fsr.
- Low ohmic losses in the inductor coil (dominant at lower frequencies)
- Low capacitive substrate losses (dominant at high frequencies).
- Low eddy currents generated by inductor-substrate interactions, resulting in an increasing effective resistance at higher frequencies.

*Process integration challenges*

- Making use of thick metal lines to achieve lower coil resistances. Cu metallization is beneficial as compared to traditional Al-interconnects. For spiral inductors built in Cu-damascene technique an improvement of Q by a factor of 2 has been reported as compared to similar Al-coils [12]. However, shunted Al-coils realized in different metal levels may also be feasible.
- Sufficient spatial separation of inductors and substrate, e.g. by putting the coils in the top metal levels or even above the passivation into the polyimide [13-16], helps to reduce capacitive and inductive parasitics and improves the Q-value. Again low- $\kappa$  materials help to reduce the capacitive parasitics and the substrate noise.
- Making use of higher resistive Si-substrates is also improving the parasitic substrate losses, however this approach may not be feasible in every case [10].
- The introduction of metallic shieldings (metal ground planes) in the lowest metal level underneath the inductors can reduce the eddy current losses in the substrate [9-11].

Currently spiral coils realized in single Al- or Cu- metal levels are the most common type of on-chip inductors. However, shunted multilevel spirals and solenoidal types of inductor designs, which are supposed to have lower substrate losses, may be used in the future [12].

The influence of extreme metal thicknesses (5- 22.5  $\mu\text{m}$ ) and innermost turn diameters on Q-factors of spiral inductors [43] as well as the questionable effect of an additional Al-layer on-top of a Cu-based inductor stack [44] is reported.

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A significant improvement of the quality factor was achieved by reducing the substrate coupling in making use of the airgaps in suspended Al-spiral inductors [27] and Al-solenoidal inductors [46]. Using surface-micromachining suspended spiral inductors of 1.38 nH (@ 1GHz) were demonstrated with a quality factor of 70 at a frequency of 6 GHz [28]. However, the thermal isolation of suspended inductors may result in significant self-heating effects which can shift Q and the operation point in RF circuits [56]. Another method for Q-value improvement (30%-70%) is the formation of localized semi-insulating Si-substrate areas under the inductor coils by proton bombardment after device fabrication, i.e. before interconnect, [32] or even after interconnect fabrication [33]. Porous silicon substrate was also reported to improve Q-values and resonant frequencies [45]. Areas with low- $\kappa$  dielectrics partially embedded in the Si-substrate under spiral inductors showed suppressed parasitic capacitances and improved Q-factors [57]. In using SOI substrates excellent inductor Q-values  $\sim 20$  were demonstrated without extra mask and processing steps [34]. Extremely high Q-values  $\sim 40$  were reported for above passivation (above IC) inductors using 5  $\mu\text{m}$  Cu lines in BCB dielectric ( $k \sim 2.7$ ) on top of a multi-layer Cu/oxide interconnect manufactured in a 90nm RF-CMOS platform technology [35].

The successful integration of micro-inductors using magnetic materials was reported also. The introduction of a magnetic ground plane of CoZrTa increased the inductance of a square spiral inductor by 36~50 % [17]. A spiral inductor sandwiched between two layers of ferromagnetic CoNbZr was demonstrated to improve the inductance by 19% and the quality factor by 23% at 2 GHz [29]. Further improvements in inductance and Q was achieved by connecting the two magnetic layers with magnetic vias and a proper inductor layout making use of the uniaxial magnetic anisotropy of a CoZrTa alloy [58]. Another example is the integration of a ferromagnetic core (Cr/Fe<sub>10</sub>Co<sub>90</sub>/Cr) into a solenoidal inductor [30]. At lower frequencies ( $< 0.2$  GHz) up to eight-fold enhancement in inductance and up to seven-fold improvement in quality factor have been achieved by using the ferromagnetic cores. At higher frequencies however, those improvements were significantly degraded by ferromagnetic resonance losses in the ferromagnetic core and by eddy currents.

Crosstalk between adjacent 3-D solenoid on-chip inductors built in 4-layer interconnect stacks was found to be dominated by magnetic coupling and substrate noise and was reduced by arranging a guard ring between the inductor and the Si substrate [79].

Significant reduction in substrate noise is reported for an inductor on an ultra-thin (1.7  $\mu\text{m}$ ) Si-substrate top-chip with a Fe/Ni-permalloy film providing magnetic screening between the top- and bottom chip in 3D-IC system in package approach [36]. Prefabricated RF inductors were transferred from a Si-substrate wafer to a flexible plastic packaging substrate (FR-4) by a wafer-transfer technology and showed significantly improved performance in Q and resonant frequency [59]. A variable on-chip inductor embedded in a wafer-level chip-scale package is proposed by making use of a movable metal plate over a spiral inductor [60]. A basic feasibility study of the variable inductor has been performed. However, the successful implementation of a MEMS actuator for moving the metal plate into the wafer-level package has still to be demonstrated.

Many of these options to build high Q inductors are looking quite interesting from a scientific point of view, but the realization in a manufacturing environment may be very difficult and expensive. Therefore, if high Q inductors are really needed, the most straight forward approach is the utilization of super-fat top metal layers with Cu thicknesses in the range of 2-8  $\mu\text{m}$ . Successful realizations with Q-factors up to 20 have been reported in a 32nm SoC platform technology [81, 82].

### 7.1.3 RESISTORS

*Applications of on-chip thin film resistors, especially in analog and mixed signal circuits*

- Clock and bus terminators
- Precision resistor arrays and networks
- Voltage dividers

*Typical resistor requirements*

- Excellent matching properties
- Precision resistance control
- High voltage linearity (low voltage coefficients)
- Low temperature coefficients (TCR)
- Low 1/f current noise
- High Q values (low parasitics)

*Process integration challenges*

- Moderate and tunable sheet resistance

- Excellent thickness control (deposition uniformity)
- Modular integration scheme
- Good etch selectivity to dielectrics
- Preferably use of standard interconnect materials

So far relatively little literature has been published about the integration of interconnect based thin film resistors. One interesting approach was the multi-functional use of a PVD TaN based MIM capacitor base plate as a precision TaN thin film resistor with varying resistivity based on different film stoichiometries. Low voltage linearity and temperature coefficients and excellent matching properties were reported for the TaN film [8]. Another approach using PVD  $WSi_x$  as metallization based resistor with reasonably good TCR values was also reported [31]. A Ti/Ni(80%)Cr(20%) thin-film resistor with nearly zero TCR for integration into a standard CMOS process was reported [80]. Also a  $TiN_xO_y$  thin film resistor was proposed and successfully integrated in the Al based interconnect scheme of a 0.5  $\mu m$  CMOS technology [83].

## 7.2 DIELECTRIC APPENDIX

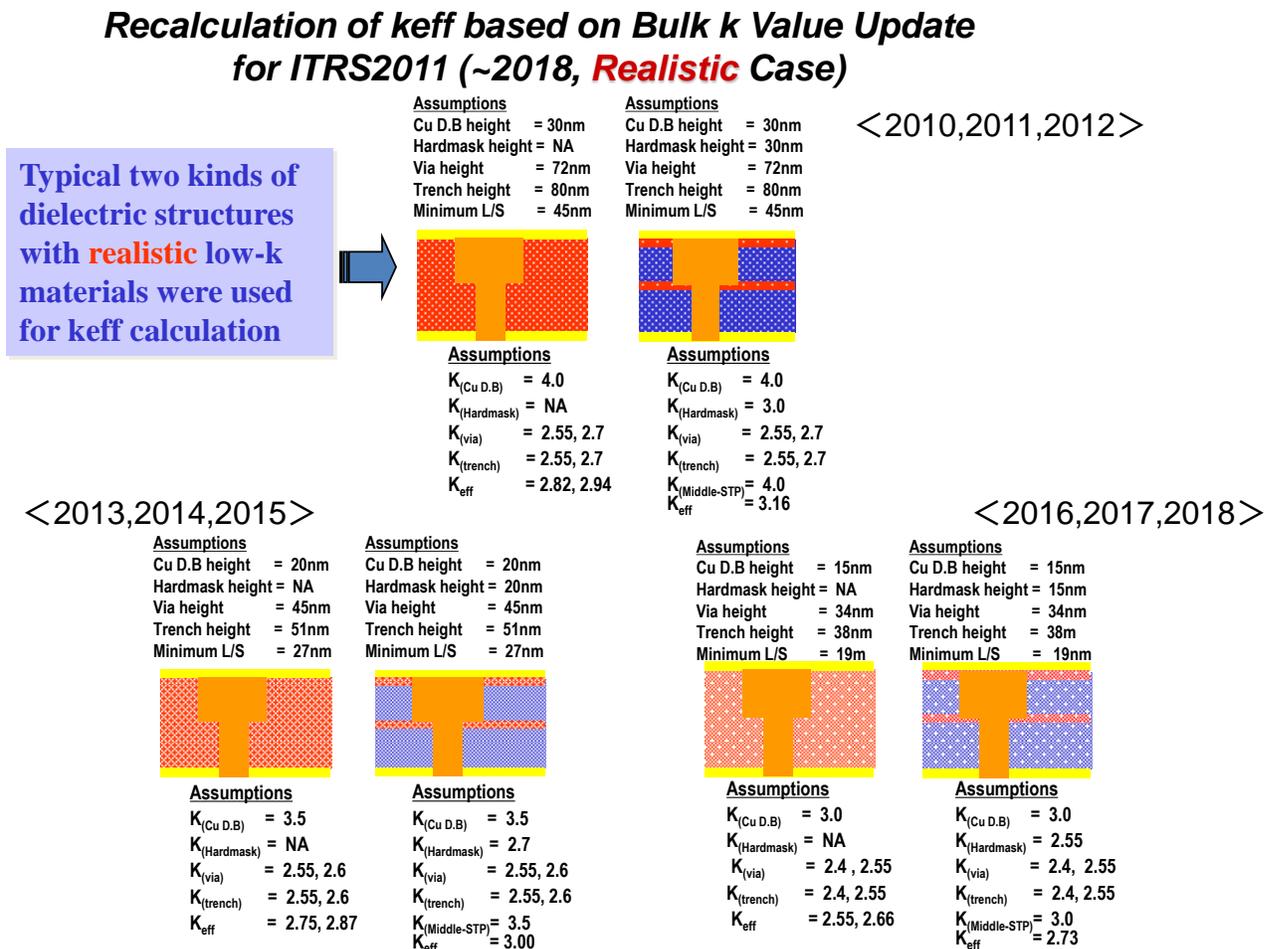


Figure A1 Dielectric Potential Solutions (2010~2018) Realistic Case

## Recalculation of keff based on Bulk k Value Update for ITRS2011 (2019~, **Realistic Case**)

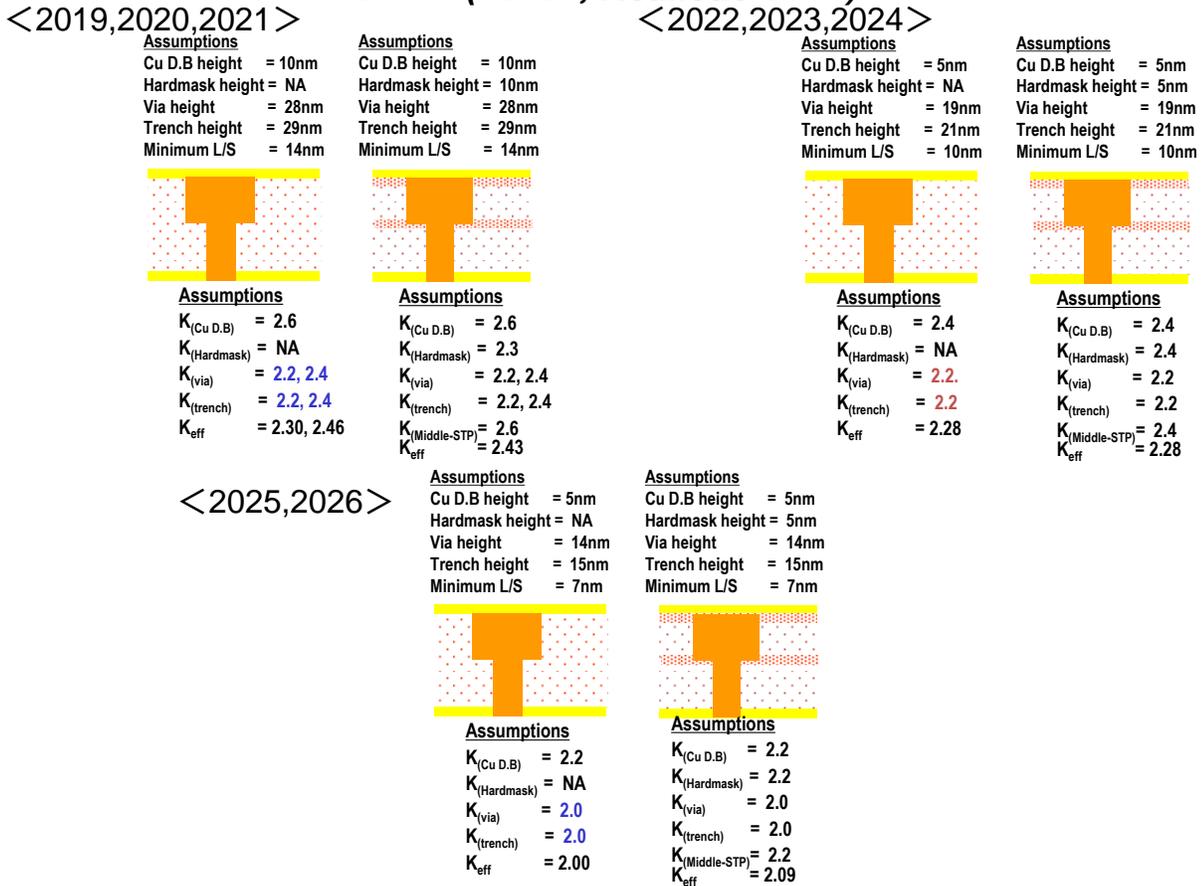


Figure A2 Dielectric Potential Solutions (2019~2027) Realistic Case

### 7.3 INTERCONNECT MODEL ADOPTED FOR RC DELAY EVALUATION APPENDIX

- The model for RC calculation is based on a 2D cross-section of a central wire, surrounded by 2 conductive planes on top and bottom, and by 2 wires on the sides having the same dimensions as the center wire, as reported in the figure. The 2 planes represent the metal layers above and below the layer of the central conductor. All the surrounding conductors are considered grounded for the capacitance calculation. The extension of the planes over the 2 lateral conductors results in limited influence on the capacitance of the central conductor. No Miller effect is considered here.
- The dimensions  $w$ ,  $s$ ,  $h$ ,  $h_v$ ,  $A/R$  and the material parameters  $\kappa_{eff}$  and  $\rho_{eff}$  are taken from the ITRS Roadmap for each technology node.

R per unit length is simply calculated as 
$$\frac{R}{l} = \frac{\rho_{eff}}{h \cdot w}$$

C per unit length is extracted from the 2D model by a static solver simulation as 
$$\frac{C}{l} = \frac{2C_l + 2C_p + C_{fringe}}{l};$$

- inputs for the simulation are dimensions and  $\kappa_{eff}$ .
- $t = w \cdot A/R$  (Cu);  $h_1 = w \cdot A/R$  (Via);  $h_1 = h_2$
- For M1 interconnect  $h_1 = t$  and  $\kappa_{eff} = 4.2$  in  $h_1$  thickness.
- In presence of a range of values in the Roadmap for  $\kappa_{eff}$ , the value used for the simulation is the average between min and max:  $\kappa_{eff} = (\kappa_{eff \max} - \kappa_{eff \min})/2$

The wire width is considered as half pitch:  $w = s = p/2$ .



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*"Via-last" TSV process*—Fabrication of TSVs after (or in the middle of) the Si back-end (BEOL) interconnect process.

*Wafer-to-Wafer (W2W, WtW) bonding*—3D-stacking strategy that uses a wafer on wafer alignment and bonding strategy. Stacked die must be equal in size and wafer stepping pattern.

*Die-to-Wafer (D2W, DtW) bonding*—3D-stacking strategy that uses a die on wafer alignment and bonding strategy. Stacked die can have different sizes and partial population of a wafer is possible.

*Die-to-Die (D2D, DtD) bonding*—3D-stacking strategy that uses a die on die alignment and bonding strategy. Stacked die can have different sizes.

*Face-to-Face (F2F, FtF) bonding*—3D-stacking strategy where the sides of the die or wafers with active devices (=“Face”-side) face each other after bonding.

*“Frontside” TSVs*—TSVs realized starting from the top surface of the wafer (device and interconnect side of the wafer).

*“Backside” TSVs*—TSVs starting from the thinned wafer backside.

*Back-to-Face (B2F, BtF) bonding*—3D-stacking strategy where the backsides of the die or wafers face each other after bonding.

*Outer TSV-Aspect ratio*—Ratio depth of the TSV to the maximum diameter of etch hole in the Si substrate.

*Inner TSV-Aspect ratio*—Ratio depth of the TSV to the maximum diameter of conductive layer of the TSV. (Aspect ratio, excluding the liner thickness)

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