Efficient and Accurate Eye Diagram Prediction for High Speed Signaling

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***Abstract*—This paper introduces an accumulative prediction method to predict the eye diagram for high speed signaling systems. We use the step responses of pull-up and pull-down to extract the worst-case eye diagram, including the eye height and jitter. Furthermore, the method produces the input patterns of the worst-case intersymbol interference. The algorithm handles signals of either symmetric or asymmetric rise/fall time. Experimental results demonstrate the accuracy and efficiency of the proposed method.**

I. Introduction

In high speed signaling system, the distortion, noise, and interference on signal waveforms constrain the system performance [1,2], e.g. bandwidth and power. An eye diagram provides one fundamental and intuitive view to evaluate the quality of the channel. Traditional methods execute the time domain simulation to obtain the eye diagram with a pseudorandom bit sequence (PRBS) as the input stimulus. Due to the limited length of the sequence, the simulated eye size is usually larger than the worst-case.

In [3], Casper et al. developed a peak distortion analysis method to extract the worst-case eye diagram. They derived the worst-case voltage and timing margin from a unit pulse response of the channel and thus avoided the PRBS simulation. They assumed that the pull-up and pull-down responses are symmetric. Hence, unit pulse response is enough to derive the output of all possible input patterns via superposition. In [4], Tsuchiya et al. proposed an analytical formula to estimate the maximum eye-opening voltage. The formula was derived from a piecewise-linear eye model and assumed the receiver side voltage reaches V_{max} when the time $2t_{tof}$ passed after rising, where t_{tof} is the time-of-flight. In [5], Analui et al. presented a method to predict data dependent jitter based on unit pulse response. Analytical formulas were derived for a first-order system and an approximated perturbation technique was applied for general systems. In [6], Zhu et al. simplified the eye prediction based on a bitonic model of the step response.

For various high speed signaling systems, the digital signals may be asymmetric on rise and fall transitions caused by the variations of the pull-up and pull-down drivers [7,8]. An efficient and general method to predict the eye diagram will be very helpful to analyze the system performance.

In this paper, we propose an efficient and accurate accumulative prediction method to predict the signal distortion caused by the intersymbol interference. The method predicts the worst-case eye diagram based on the responses of the pull-up and pull-down transitions. The proposed algorithm handles signals of either asymmetric or symmetric rise/fall time. Furthermore, the computation takes a complexity linear to the length of the transient behavior of the step responses.

The project is partially supported by California MICRO Program. The work of W. Yu was supported by the Basic Research Foundation of Tsinghua National Laboratory for Information Science and Technology (TNList).

The remainder of this paper is organized as follows. In section II, we describe the background regarding the step response and eye diagram. Section III presents the mathematical formulation of the worst-case eye diagram prediction and the accumulative prediction method. Section IV analyzes the complexity and error of the proposed method. The experimental results are shown in Section V. Section VI summarizes our work and briefly discusses future research direction.

II. Preliminaries

We assume that the signaling system is linear time-invariant. The transmitted digital signal is modeled as a linear combination of step responses with shifted times. We analyze the signal's eye diagram based on the superposition of the step responses.

A. Digital Signal Communication and Step Response

The step response is the time domain behavior of the output when the input makes a zero-one transition in a very short time. The step response comprises the characteristics of the system such as the delay, the reflection of the discontinuity, the voltage attenuation and saturation for a transmission line.

We assume that the input is a binary stream of zeros and ones. Thus, input signal, x(t), is a linear combination of a series of alternate zero-one and one-zero transitions, i.e.

$$\begin{aligned} x(t) &= x_r(t - k^r{}_1 T) - x_f(t - k^f{}_1 T) + \dots \\ &+ x_r(t - k^r{}_i T) - x_f(t - k^f{}_i T) + \dots \end{aligned} \tag{1}$$

where $x_r(t)$ is the zero-one transition with a given rise time, $-x_f(t)$ is the one-zero transition with a given fall time, and T is the time interval of each bit. The coefficients k^r_i and k^f_i represent the slot numbers that the ith zero-one and one-zero transitions happen. All coefficients in (1) are non-negative integers and satisfy the inequality

$$k^r_1 < k^f_1 < k^r_2 < k^f_2 < \dots < k^r_i < k^f_i < \dots \tag{2}$$

as we assume that the signal starts from zero.

The output signal y(t) is modeled as a linear combination of step responses

$$\begin{aligned} y(t) &= s_r(t - k^r{}_1 T) - s_f(t - k^f{}_1 T) + \dots \\ &+ s_r(t - k^r{}_i T) - s_f(t - k^f{}_i T) + \dots \end{aligned} \tag{3}$$

$$y(t)\begin{cases} = 0, t \le 0 \\ > 0, t > 0 \end{cases}, s_r(t)\begin{cases} = 0, t \le 0 \\ > 0, t > 0 \end{cases}, s_f(t)\begin{cases} = 0, t \le 0 \\ > 0, t > 0 \end{cases} \tag{4}$$

where $s_r(t)$ is the step response of $x_r(t)$ and $s_f(t)$ is the step response of $x_f(t)$. For simplicity, we shift the time frame of the responses by the time-of-flight from the input to output to simplify the notation. Since

our results depend on the combinations of the step responses only, the shifting does not hamper the validity of the results.

Fig.1 shows the relationship between the digital signal and the step response. The input signal x(t) is the combination of transitions and the output signal y(t) is the combination of step responses.

B. Eye Diagram

The eye diagram is an oscilloscope display in which a digital signal at the receiver side is repetitively sampled to get a good representation. It's created by taking the time domain signal and overlapping the waveform at a time window of certain multiple bit periods, as shown in Fig.2. In general, the following features of the eye diagram are defined

- Eye opening (height, peak to peak): measure of the additive noise in the signal,
- Eye overshoot/undershoot: measure of the peak distortion,
- Eye width: measure of timing jitter effects.

We use *'1' edge* to denote the transmitted bit one, *'1' edge rising* to denote that there's a zero-one transition right before this bit while *'1' edge holding* means the previous bit is also one. The notations for *'0'* are similar. Looking into the eye diagram, we define eight voltage bounds for every time point in the eye diagram, as shown in Fig.2:

- '1' edge rising upper and lower bound, representing the maximum and minimum voltage for zero-one transition, as shown in Fig.2 node 1 and 2;
- '1' edge holding upper and lower bound, representing the maximum and minimum voltage for continuous one bits, as shown in Fig.2 node 3 and 4;
- '0' edge falling upper and lower bound, representing the maximum and minimum voltage for one-zero transition, as shown in Fig.2 node 5 and 6;
- '0' edge holding upper and lower bound, representing the maximum and minimum voltage for continuous zero bits, as shown in Fig.2 node 7 and 8.

The voltage bounds in the overlapping time window reveal the eye's contour and reflect all the valuable features of the eye diagram. Our method predicts the worst-case eye diagram by analyzing these eight voltage bounds.

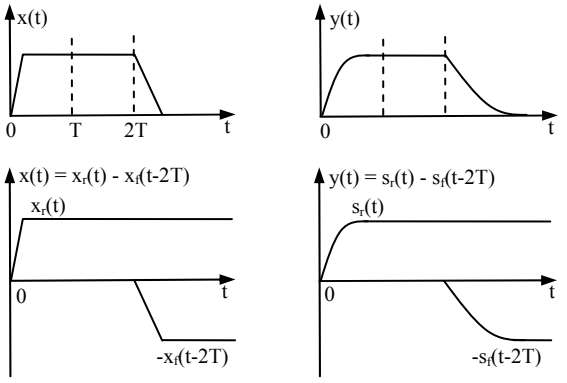


Figure 1. The digital signal and step responses.

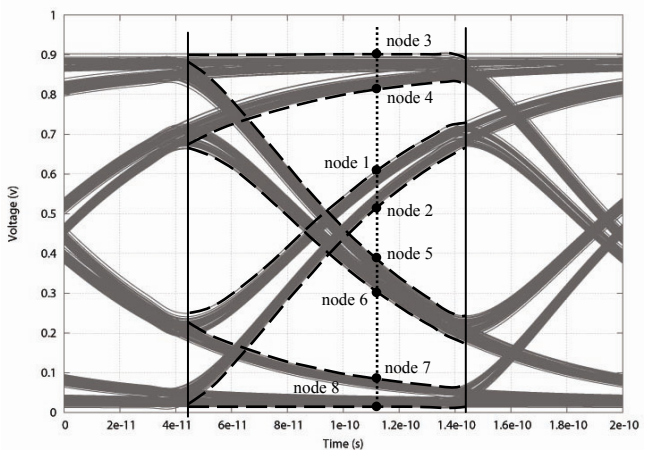


Figure 2. Eye Diagram
Eight voltage bounds for any time point.

III. WORST-CASE EYE DIAGRAM PREDICTION

The accumulative prediction method predicts the worst-case eye diagram based on step responses. The eye opening and timing jitter are extracted for the worst-case eye diagram. The input patterns, which produce the worst-case intersymbol interference, are also generated.

A. Voltage Bounds for Worst-case Eye Diagram

The eye diagram is created by overlapping the signal waveform in the time window of one bit period T in our analysis. The waveform in the eye diagram is given by

$$e(t) = \left\{ y(t + k_i T) \middle| 0 \le t \le T, k_i \in Z^* \right\} \tag{5}$$

We derive the maximum and minimum values of $e(t_o)$ which gives the voltage bounds for the worst-case eye diagram, where t_o is the observing time point $0 \le t_o \le T$. The voltage bounds are expressed by a combination of $s_r(t)$ and $s_f(t)$.

Theorem 1: Given the step responses $s_r(t)$ and $s_f(t)$, the eight voltage bounds are determined by the equations in Table I, $0 \le t_o \le T$.

The coefficients k^o_r and k^o_f represent the transition time for the observing bit, k^r_i and k^f_i represent the transition time for previous bits. All coefficients are positive integers and satisfy the inequality

$$k^o_f < k^o_r < k^f_1 < k^r_1 < k^f_2 < k^r_2 < \ldots < k^f_i < k^r_i < \ldots \tag{6}$$

TABLE I. VOLTAGE BOUNDS EQUATIONS

Voltage bounds		$y(t_o)$
'1' edge rising upper bound	$e_{upper01}(t_o) = \max(y(t_o))$	$s_r(t_o) + \sum_i (-s_f(t_o + k^f_i T) + s_r(t_o + k^r_i T))$
'1' edge rising lower bound	$e_{lower01}(t_o) = \min(y(t_o))$	
'1' edge holding upper bound	$e_{upper11}(t_o) = \max(y(t_o))$	$s_r(t_o + k^o_r T) + \sum_i (-s_f(t_o + k^f_i T) + s_r(t_o + k^r_i T))$
'1' edge holding lower bound	$e_{lower11}(t_o) = \min(y(t_o))$	
'0' edge falling upper bound	$e_{upper10}(t_o) = \max(y(t_o))$	$-s_f(t_o) + s_r(t_o + k^o_r T) + \sum_i (-s_f(t_o + k^f_i T) + s_r(t_o + k^r_i T))$
'0' edge falling lower bound	$e_{lower10}(t_o) = \min(y(t_o))$	
'0' edge holding upper bound	$e_{upper00}(t_o) = \max(y(t_o))$	$-s_f(t_o + k^o_f T) + s_r(t_o + k^o_r T) + \sum_i (-s_f(t_o + k^f_i T) + s_r(t_o + k^r_i T))$
'0' edge holding lower bound	$e_{lower00}(t_o) = \min(y(t_o))$	

Theorem 2: The eight voltage bounds in Table I are the worst-case when step response corresponding to the earliest transition considered in the summation reaches saturation voltage.

We formulate an optimization problem and devise a dynamic programming algorithm to compute the bounds. The formulated problem is as follows

- ***Given****:*
  two arrays A and B
  $A=\{s_r(t_o+T), s_r(t_o+2T), \ldots, s_r(t_o+k_mT)\}$
  $B=\{s_f(t_o+T), s_f(t_o+2T), \ldots, s_f(t_o+k_mT)\}$
  where $s_r(t)$ and $s_f(t)$ have reached saturation voltage at time (t_o+k_mT)
- ***Objective:***
  min/max $\sum_i A[i] - \sum_j B[j]$
- ***Constraints:***
  the starting transition must be selected from array A;
  the ending transition could be selected from array A or B depending on different voltage bounds;
  the transitions must be selected from A and B alternately.

We record all the possible transitions in the arrays. The optimal solution is produced by selecting a set of transitions from the arrays. Dynamic programming is applied to solve the problem. If we assume the optimal solution for A[1,…,m-1] and B[1,…,m-1] is known, the optimal solution for A[1,…,m] and B[1,..,m] is obtained by arithmetical operations and comparisons straightforwardly. Basically, the optimal solution for arrays with the first two elements is obtained trivially.

The detailed algorithm for '1' edge rising lower bound is shown in Fig.3. The optimal solution, called minDeltaV, is the minimum voltage offset and the bound is given by

$$e_{lower01}(t_o) = s_r(t_o) + \text{minDeltaV} \quad (7)$$

For this voltage bound, the ending transition is selected from array B because there's a zero-one transition at the end. The algorithms for other voltage bounds are similar.

Theorem 3: The voltage bounds derived by algorithm volBounds are the exact worst-case of the eye diagram.

Fig.4 and Table II depict an example of computing the voltage offset for '1' edge rising lower bound. In Fig.4, we mark on the step responses $s_r(t)$ and $s_f(t)$ the sampling points starting from the observing time point t_o. In Table II, we illustrate the operation results of executing the algorithm in Fig.3 step by step. The data in the table are the optimal solution if the corresponding transition is selected as the last transition. The data with gray background are the optimal solution for current step. Finally, the optimal solution is -0.14 by selecting B[2], A[3], B[4] and A[5].

```
volBounds_01LowerBound(A, B)
  A_min[1] ← no meaning
  B_min[1] ← -B[1]
  A_min[2] ← -B[1]+A[2]
  B_min[2] ← -B[2]
  minA ← A_min[2]
  minB ← min(B_min[1], B_min[2])
  for i = 3 to k_m
    do A_min[i] ← minB+A[i]
       B_min[i] ← min(minA-B[i], -B[i])
       minA ← min(minA, A_min[i]);
       minB ← min(minB, B_min[i]);
  minDeltaV = minA
  return(minDeltaV)
```

Figure 3. Algorithm for '1' edge rising lower bound.

B. *Worst-case Eye Opening*

The eye opening is the difference between the minimum of the samples related to a logical '1' and the maximum of the samples related to a logical '0', measured at the sampling instant. Usually the eye opening is captured at the symbol transition point. Therefore, we set the observing time point at T to extract the eye opening. The worst-case eye opening is given by

$$V_{eye} = \min(e_{lower01}(T), e_{lower11}(T)) - \max(e_{upper10}(T), e_{upper00}(T)) \quad (8)$$

C. *Worst-case Timing Jitter*

The timing jitter measures the variance in the actual transition time from the ideal transition time. We define the timing jitter as the deviation of transitions crossing the half of saturation voltage. As shown in Fig.5, for an open eye, the timing jitter is given by

$$T_{jitter} = T_{jright} - T_{jleft} \quad (9)$$

The right and left time boundaries are determined by the crossing points of the voltage bounds and the half saturation voltage.

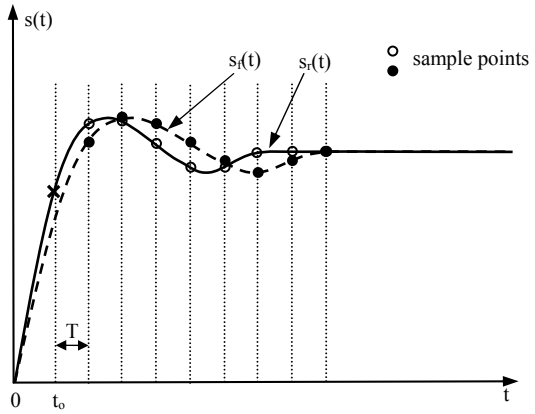


Figure.4 Step responses example.

TABLE II. EXAMPLE: FIND MINIMUM VALUE MINDELTAV

t	t_o+T	t_o+2T	t_o+3T	t_o+4T	t_o+5T	t_o+6T	t_o+7T	t_o+8T
A $s_r(t)$ v	0.96	0.97	0.90	0.85	0.85	0.88	0.89	0.89
B $s_f(t)$ v	0.91	0.98	0.96	0.91	0.86	0.83	0.86	0.89
step 1		0.06						
	-0.91	-0.98						
step 2		0.06	-0.08					
	-0.91	-0.98	-0.96					
step 3		0.06	-0.08	-0.13				
	-0.91	-0.98	-0.96	-0.99				
step 4		0.06	-0.08	-0.13	-0.14			
	-0.91	-0.98	-0.96	-0.99	-0.99			
step 5		0.06	-0.08	-0.13	-0.14	-0.11		
	-0.91	-0.98	-0.96	-0.99	-0.99	-0.97		
step 6		0.06	-0.08	-0.13	-0.14	-0.11	-0.10	
	-0.91	-0.98	-0.96	-0.99	-0.99	-0.97	-1.00	
step 7		0.06	-0.08	-0.13	-0.14	-0.11	-0.10	-0.11
	-0.91	-0.98	-0.96	-0.99	-0.99	-0.97	-1.00	-1.03

$T_{jright} = \max(T_{jr1}, T_{jr2})$ (10)

$T_{jr1} \in (0,T]$ and $T_{jr2} \in (0,T]$

$e_{lower01}(T_{jr1}) = V_{sat}/2$

$e_{upper10}(T_{jr2}) = V_{sat}/2$

$T_{jleft} = \min(T_{jl1}, T_{jl2})$ (11)

$T_{jl1} \in (0,T]$ and $T_{jl2} \in (0,T]$

$e_{lower10}(T_{jl1}) = V_{sat}/2$

$e_{upper01}(T_{jl2}) = V_{sat}/2$

We use binary search on the time region (0,T] to find T_{jr1}, T_{jr2} and T_{jl1}, T_{jl2} efficiently.

D. Worst-case Input Data Pattern

The accumulative prediction method generates the input data patterns of the worst-case intersymbol interference. The method computes the voltage bounds by determining the bit transitions. Thus the input data patterns, which make the bounds happen in the eye diagram, are generated by backtracking the bit transitions.

IV. Analysis of Prediction

In this section, we derive the complexity, the predicted error of the algorithm and the equivalence of the method in [3] when the signal's rise and fall time are symmetric.

A. Prediction Complexity

We assume that the number of sampling time points in the step response is n. In one bit slot, we have an enough amount (T_N) of sampling points for accuracy. Then in the accumulative prediction method, the array size m for each observing time point t_o is given by

$$m = \left\lceil \frac{n}{T_N} \right\rceil \tag{12}$$

The complexity of the dynamic programming algorithm discussed in section III is O(m) because the iterations act on all the array elements and each iteration has constant operations. The total complexity of computing the voltage bounds for all time points in one bit period is given by

$$T_N \times 8 \times O(m) = O(n) \tag{13}$$

The complexity of computing the worst-case eye opening is O(m) for calculating four voltage bounds at time point T. Computing the worst-case timing jitter applies binary search, the complexity is $O(m \lg T_N)$. The complexity of generating the worst-case input data pattern for one voltage bound is O(m) because the pattern is obtained by recording and backtracking the bit transitions.

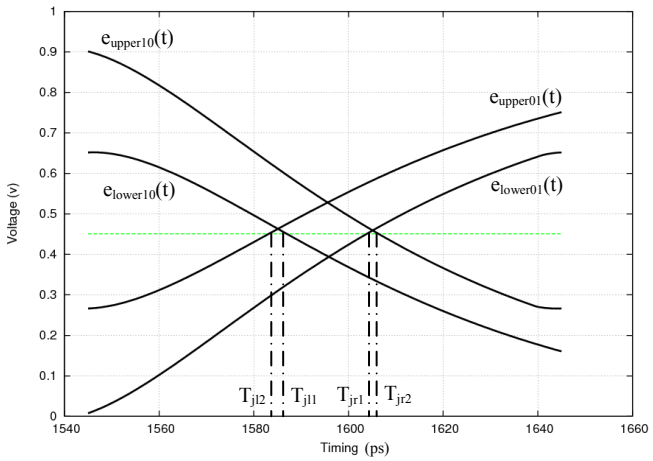


Figure 5. Timing jitter.

B. Prediction Error

The prediction error is caused by two potential error sources. First, inevitable error is introduced by the discrete sampling time points. More sampling time points with smaller time step achieve better accuracy with the cost of complexity. Secondly, the accuracy of the saturation voltage affects the prediction accuracy. The step response waveform fluctuates in a very small range around saturation voltage after certain simulation time. It's hard to obtain the exact saturation voltage value. Further the effective voltage is actually determined by the specific elapsed time in the input bit sequence. The saturation voltage variation introduces the prediction error.

C. Digital Signal with Symmetric and Asymmetric Rise/Fall time

The accumulative prediction method handles signals of either symmetric or asymmetric rise/fall time since the method models zero-one and one-zero transition separately. The peak distortion analysis [3] developed by Casper et al. derived the worst-case voltage and timing margin based on the unit pulse response. They assumed that the pull-up and pull-down responses are symmetric. As shown in Fig.6 bold lines, the rise and fall edges cannot be combined to represent the digital data of asymmetric rise/fall time.

For digital signal with symmetric rise/fall time, the accumulative prediction method is proved to be equivalent to the peak distortion analysis. Both of them have linear complexity.

Theorem 4: the accumulative prediction method is equivalent to the peak distortion analysis for signals with symmetric rise/fall time.

Sketch of proof: according to the formulation, the unit pulse response is represented by

$$p(t) = s_r(t) - s_f(t-T) \tag{14}$$

The step response $s_r(t)$ and $s_f(t)$ are identical for symmetric rise/fall time, i.e. the array A and B are the same in the formulation of the accumulative prediction method. Hence, the feasible solution is rewritten as the combination of pulse response

$$\begin{aligned}
&\sum_i A[i] - \sum_j B[j] \\
&= \sum_i (-s_f(t_o + k^f{}_i T) + s_r(t_o + k^r{}_i T)) \\
&= \sum_i [-s_f(t_o + k^f{}_i T) + s_r(t_o + (k^f{}_i + 1)T) \\
&- s_f(t_o + (k^f{}_i + 1)T) + s_r(t_o + (k^f{}_i + 2)T) + \ldots \\
&- s_f(t_o + (k^r{}_i - 1)T) + s_r(t_o + k^r{}_i T)] \\
&= \sum_i [p(t_o + (k^f{}_i + 1)T) + \ldots + p(t_o + k^r{}_i T)]
\end{aligned} \tag{15}$$

The minimum solution picks all the negative pulse response and the maximum solution picks all the positive pulse response. Therefore, the accumulative prediction method is equivalent to the peak distortion analysis for symmetric rise/fall time signal. ■

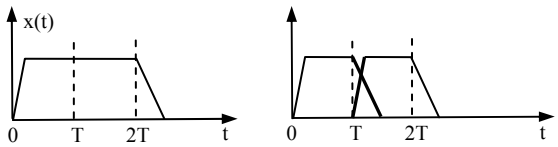


Figure 6. For signal with asymmetric rise/fall time, unit pulse response is not enough to cover all input patterns via superposition.

V. VERIFICATION EXPERIMENTS

We implemented the accumulative prediction method in C program. With a transmission-line case, the accuracy and efficiency of the proposed method is demonstrated.

A. Experiment Setup

Fig.7 displays the structure and parameters of the transmission-line case. The single-end transmission line is on printed circuit board (PCB) with FR4 materials, transmitting signals among processors and memory. The length of the transmission line is 25cm and the characteristic impedance is 50Ω. As shown in Fig.7 (b), a voltage source with Rs=4Ω produces the input signal at the driver side and the voltage V_{dd} is 1V. At the receiver side, a resistor is connected as the termination. We use IBM PowerSPICE [6] to perform the transient simulation and in the simulation, we apply the frequency-dependent RLGC table model which is extracted with IBM CZ2D package [7].

We perform two sets of experiments, one for symmetric rise/fall time and another for asymmetric rise/fall time. For each set of experiments, three simulations are executed

- Run step response simulation and predict the worst-case eye diagram using the accumulative prediction program,
- Run transient simulation with the worst-case input patterns generated by the accumulative prediction program,
- Run transient simulation with a pseudorandom bit sequence (PRBS).

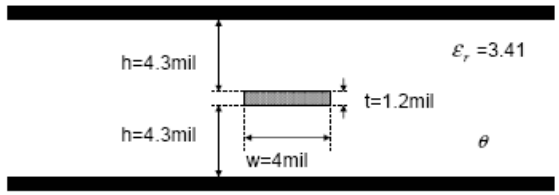
B. Experimental Results

We set the bit period to be 100ps, the rise/fall time 10ps for symmetric signal, and the rise/fall time 10ps/15ps respectively for asymmetric signal. The simulation results for the symmetric signal are shown in table III, IV and V and the results for the asymmetric signal are shown in table VI, VII and VIII. We set 10 cases with various termination impedance, from 32Ω to 68Ω.

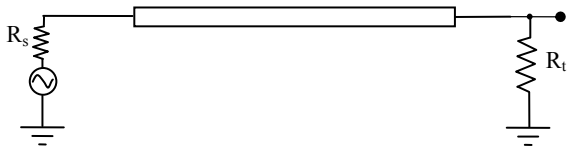
Fig.8 shows the eye opening and timing jitter curves for the symmetric rise/fall time simulations which correspond to the data in table III and IV. Fig.9 shows the eye opening and timing jitter curves for the asymmetric rise/fall time simulations which correspond to the data in table VI and VII.

The experiment demonstrates that the prediction matches the simulation with the worst-case input patterns very well. The simulation using PRBS as stimulus cannot reflect the worst-case of the eye diagram. As the length of the PRBS increases, the simulation achieves better estimation. Fig.10 and Fig.11 display the eye diagrams of different stimulus.

Table V and VIII record the average CPU times for the simulations. The simulation takes less than one minute to generate the step response. The prediction takes no more than one second.



(a) The cross section of the single-end transmission line



(b) The signaling scheme

Figure 7. The single-end transmission line structure.

TABLE III. EYE OPENING, SYMMETRIC RISE/FALL TIME

Rt	Eye Opening (V)			
	100 PRBS	***10000 PRBS***	***Worst-case Input***	***Predict***
32	0.24162999	0.19348612	0.14754779	0.146586
36	0.28892423	0.25287776	0.20618604	0.205273
40	0.33142498	0.30341259	0.26091507	0.260058
44	0.36606853	0.34187927	0.31197535	0.311138
48	0.39882782	0.37755125	0.35955214	0.358757
52	0.42980694	0.41067793	0.38829700	0.387563
56	0.45193290	0.43100600	0.37934625	0.378743
60	0.45400906	0.43434301	0.36499717	0.364447
64	0.44600999	0.42910893	0.34778497	0.347413
68	0.43707650	0.42199397	0.32841799	0.328084
Average relative error	27.47%	17.49%	0	-0.26%

TABLE IV. TIMING JITTER, SYMMETRIC RISE/FALL TIME

Rt	Timing Jitter (ps)			
	100 PRBS	***10000 PRBS***	***Worst-case Input***	***Predict***
32	44.0	44.0	51.3	51.4
36	32.7	32.7	41.4	41.5
40	25.2	25.2	33.6	33.7
44	19.6	19.6	27.0	27.4
48	17.5	17.3	21.9	22.1
52	15.6	14.9	20.1	20.0
56	15.8	16.7	23.3	23.4
60	16.1	19.2	27.2	27.2
64	20.6	21.6	31.1	31.1
68	23.3	24.9	35.0	35.1
Average relative error	-27.03%	-25.17%	0	0.33%

TABLE V. AVERAGE CPU TIME, SYMMETRIC RISE/FALL TIME

100 PRBS	10000 PRBS	Worst-case Input	Step Response	Predict
5.8 s	14 m 55.4 s	2 m 1 s	26.9 s	0.345 s

TABLE VI. EYE OPENING, ASYMMETRIC RISE/FALL TIME

Rt	Eye Opening (V)			
	100 PRBS	*5000 PRBS*	*Worst-case Input*	*Predict*
32	0.24085751	0.19462714	0.14594329	0.144866
36	0.28806198	0.25378747	0.20443388	0.203427
40	0.33045842	0.30383077	0.25906041	0.258093
44	0.36473602	0.34181800	0.30998847	0.309069
48	0.39714371	0.37704639	0.35748097	0.356586
52	0.42778562	0.40976195	0.38611021	0.385301
56	0.44792679	0.42957339	0.37709847	0.376400
60	0.44738613	0.43173967	0.36266126	0.362026
64	0.43849474	0.42617642	0.34534802	0.344920
68	0.42877489	0.41812539	0.32593423	0.325526
Average relative error	27.37%	18.13%	0	-0.30%

TABLE VII. TIMING JITTER, ASYMMETRIC RISE/FALL TIME

Rt	Timing Jitter (ps)			
	100 PRBS	*5000 PRBS*	*Worst-case Input*	*Predict*
32	55.0	55.0	54.9	55.0
36	45.0	45.0	44.9	45.0
40	37.2	37.2	36.9	37.1
44	30.8	30.8	30.6	30.7
48	25.5	25.5	25.4	25.4
52	21.2	21.2	23.3	23.2
56	19.3	20.1	26.7	26.6
60	20.4	22.6	30.6	30.5
64	22.8	25.1	34.4	34.4
68	25.7	27.6	38.5	38.4
Average relative error	-13.8%	-11.30%	0	-0.01%

TABLE VIII. AVERAGE CPU TIME, ASYMMETRIC RISE/FALL TIME

100 PRBS	5000 PRBS	Worst-case Input	Step Response	Predict
5.9 s	5 m 53.2 s	3 m 3 s	54 s	0.344 s

VI. CONCLUSION

In this paper, an efficient and accurate accumulative prediction method is developed to analyze the signal distortion caused by intersymbol interference. The method handles signals with asymmetric rise/fall time with complexity linearly proportional to the length of the step response for its transition to the saturation voltage. The extension of this method to circuit design optimization and noise margin analysis could be explored in the future.

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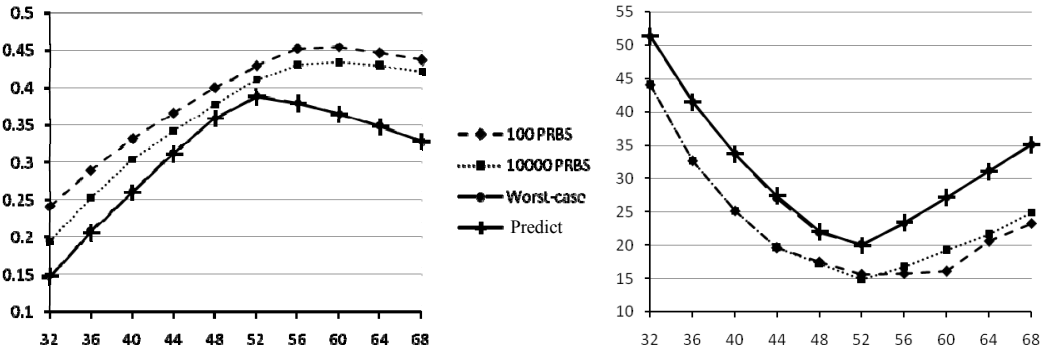
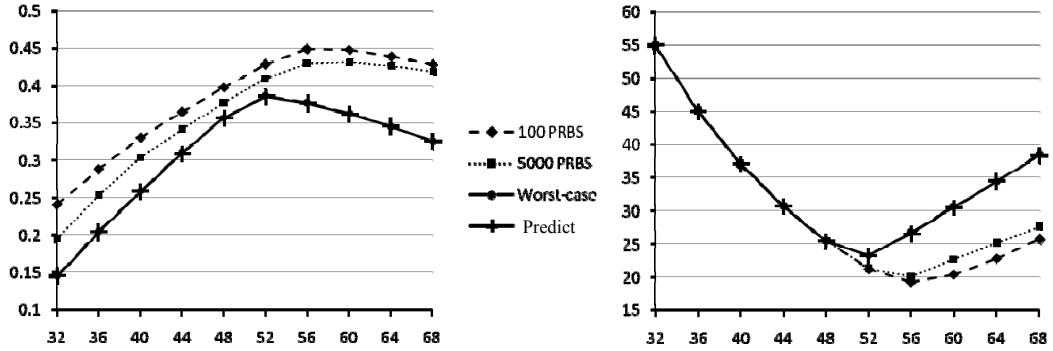


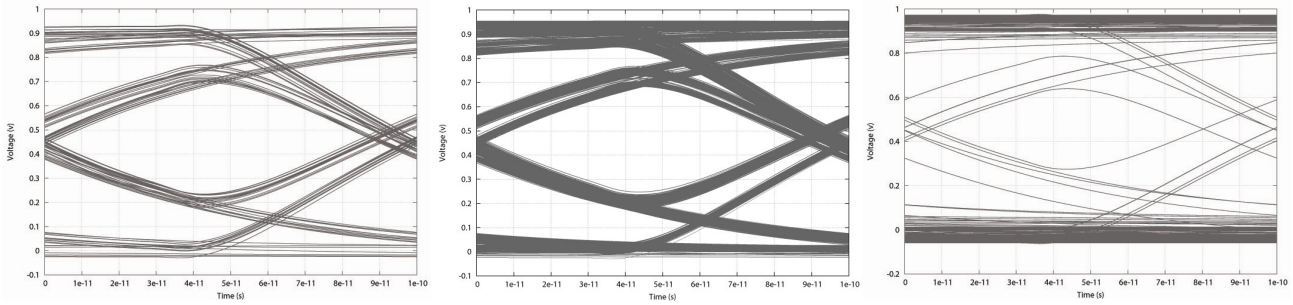
(a) Eye opening (v) vs. Rt (Ω) (b) Timing Jitter (ps) vs. Rt (Ω)

Figure 8. Results for signal with symmetric rise/fall time.



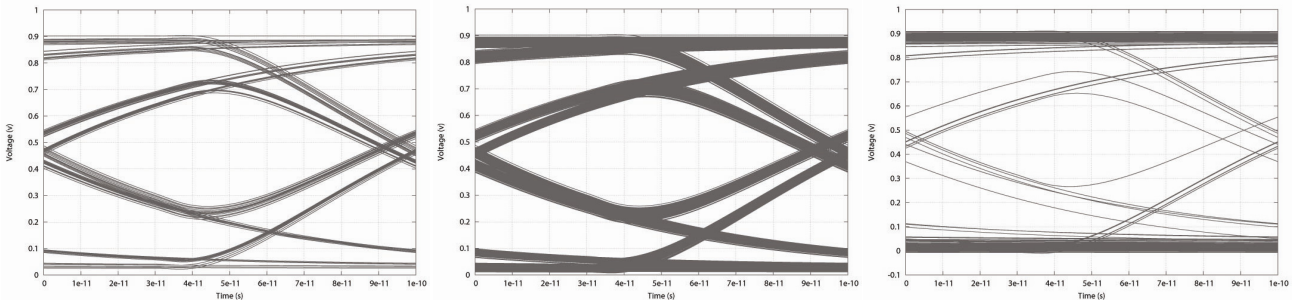
(a) Eye opening (v) vs. Rt (Ω) (b) Timing Jitter (ps) vs. Rt (Ω)

Figure 9. Results for signal with asymmetric rise/fall time.



(a) 100 PRBS (b) 10000 PRBS (c) worst-case input

Figure 10. Eye diagram for signal with symmetric rise/fall time, Rt = 60Ω.



(a) 100 PRBS (b) 5000 PRBS (c) worst-case input

Figure 11. Eye diagram for signal with asymmetric rise/fall time, Rt = 52Ω.