

CSE 141 Discussion

Midterm Review

MIPS Instructions

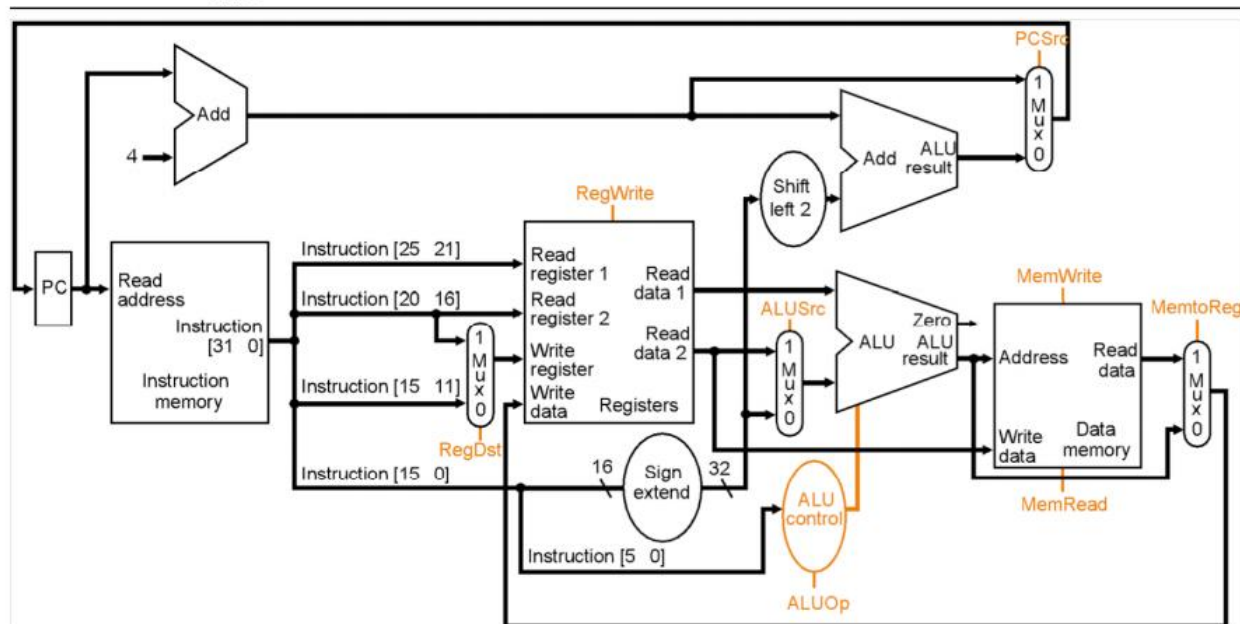
- `sw R4, -100(R16)` (or `sw Rt, Imm(Rs)`)
- What is the register number supplied to the register file's "Write register" input?
 - It's actually R4
 - What???
- I-Type Instruction

Op [31:26]	Rs [25:21]	Rt [20:16]	Imm [15:0]
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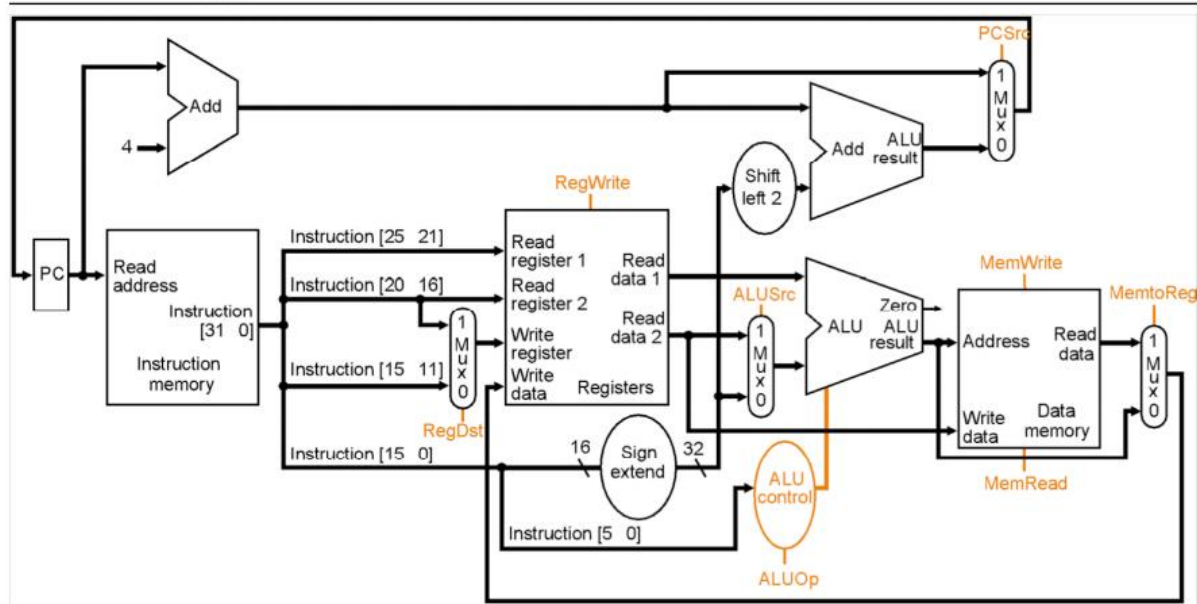
- Figure 4.17 has the write register as either [20:16] or [15:11] depending on the instruction. Since it can't be [15:11] we have only one option

MIPS Instructions

- What are the control signals for the following instruction assuming the architecture below?
 - `addi $r0, $r1, 4`



MIPS Instructions



RegDst	RegWrite	ALUSrc	ALUOp	MemWrite / MemRead	MemtoReg	PCSrc
1	1	0	Add	0	0	1

Performance Question

- Suppose we wanted to add the auto-increment addressing mode to the MIPS ISA – e.g., `lw R1, 1000(R2++)`. This saves an instruction every time we observe a load followed by an increment of the address register. Is this a good idea?
- Consider only performance, and assume that we have to increase cycle time by 10% to accommodate the new instruction,
- That 30% of our instructions are loads,
- That we can apply this change to 50% of all loads,
- And that CPI doesn't change.

Performance Question

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- That 30% of our instructions are loads,
- That we can apply this change to 50% of all loads,
- And that CPI doesn't change.

30% * 50% = 15% fewer instructions

$ET_{new} = (0.85 * IC_{old}) * CPI * (1.1 * CT_{old})$

$ET_{new} = 0.935 * ET_{old}$

Good idea. Speedup = $1/0.935 = 1.069$

Comparing Processors

- Given the following stages (in ps):

IF	ID	EX1	EX2	EX3	MEM1	MEM2	WB
200	150	175	300	225	100	150	75

- What is the single cycle time?
- What is the pipeline cycle time?

Comparing Processors

- Given the following stages (in ps):

IF	ID	EX1	EX2	EX3	MEM1	MEM2	WB
200	150	175	300	225	100	150	75

- What is the single cycle time?

$$200+150+175+300+225+100+150+75 = 1375 \text{ ps}$$

- What is the pipeline cycle time?

$$\max(\text{All Stages}) = 300 \text{ ps}$$

Comparing Processors

- If I split the stages like so:

IF	ID	EX1	EX2	EX3	EX4	MEM 1	MEM 2	WB
200	150	175	150	150	225	100	150	75

- What is the new pipeline cycle time?
- What is the savings to get one instruction through the pipeline vs. before?

Comparing Processors

- If I split the stages like so:

IF	ID	EX1	EX2	EX3	EX4	MEM 1	MEM 2	WB
200	150	175	150	150	225	100	150	75

- What is the new pipeline cycle time?

Max(all stages) = 225 ps

- What is the savings to get one instruction through the pipeline vs. before?

$$8 * 300 - 9 * 225 = 2400 - 2025 = 375 \text{ ps}$$

Pipelining

- What are the dependencies?

1. lw \$r0 0(\$r1)

2. addi \$r1 \$r0 1

3. sw \$r2 0(\$r1)

4. addi \$r0 \$r0 1

5. add \$r0 \$r3 \$r4

6. addi \$r3 \$r3 -1

Pipelining

- What are the dependencies?

```
1. lw $r0 0($r1)
2. addi $r1 $r0 1 # RAW from 1
3. sw $r2 0($r1) # RAW from 2
4. addi $r0 $r0 1 # RAW from 1
5. add $r0 $r3 $r4 # WAW from 4
6. addi $r3 $r3 -1 # WAR from 5
```

- Focus on RAW dependencies for hazards

No Forwarding:

[illegible]

No Forwarding:

[illegible]

No Forwarding:

[illegible]

No Forwarding:

Can we do better with forwarding?

[illegible]

With Forwarding:

Yes - but not as well as we hoped

[illegible]

Branch Prediction

- Know the very simple ones
 - “always taken/not taken” and simple 1-bit predictors .

Example:

```
loop:
bne r0, 100, end
addi r1, r1, 1
addi r0, r0, 1
j loop
end:
```

Branch Prediction

Example:

```
loop:
bne r0, 100, end
addi r1, r1, 1
addi r0, r0, 1
j loop
end:
```

- Always not taken predictor:
 - 99 predicts, 1 mispredict
 - 99% accuracy
- Always taken predictor
 - 1 predict, 99 mispredicts
 - 1% accuracy
- How would a one bit predictor fare?