1) Sequential logic implementation

Consider the following incompletely-specified Moore machine ("X" indicates don't cares).

	$S_1{}^+S_0{}^+$				
S_1S_0	$XY = 00$	01	10	11	F
A	B	C	X	B	0
B	A	B	X	C	X
C	C	A	X	C	1

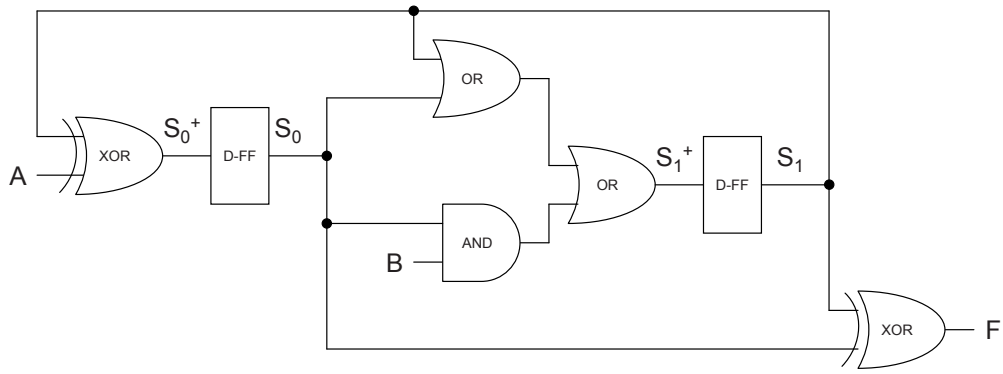
Suppose we use the following state encoding.

State	S_1S_0
A	00
B	11
C	01

Derive the **minimum** two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

$$F =$$
$$S_1{}^+ =$$
$$S_0{}^+ =$$

2) Reverse engineer sequential circuit to finite state machine



a) Fill out the following functions (OK to use $\oplus$ in functions).

$$F =$$
$$S_1+ =$$
$$S_0+ =$$

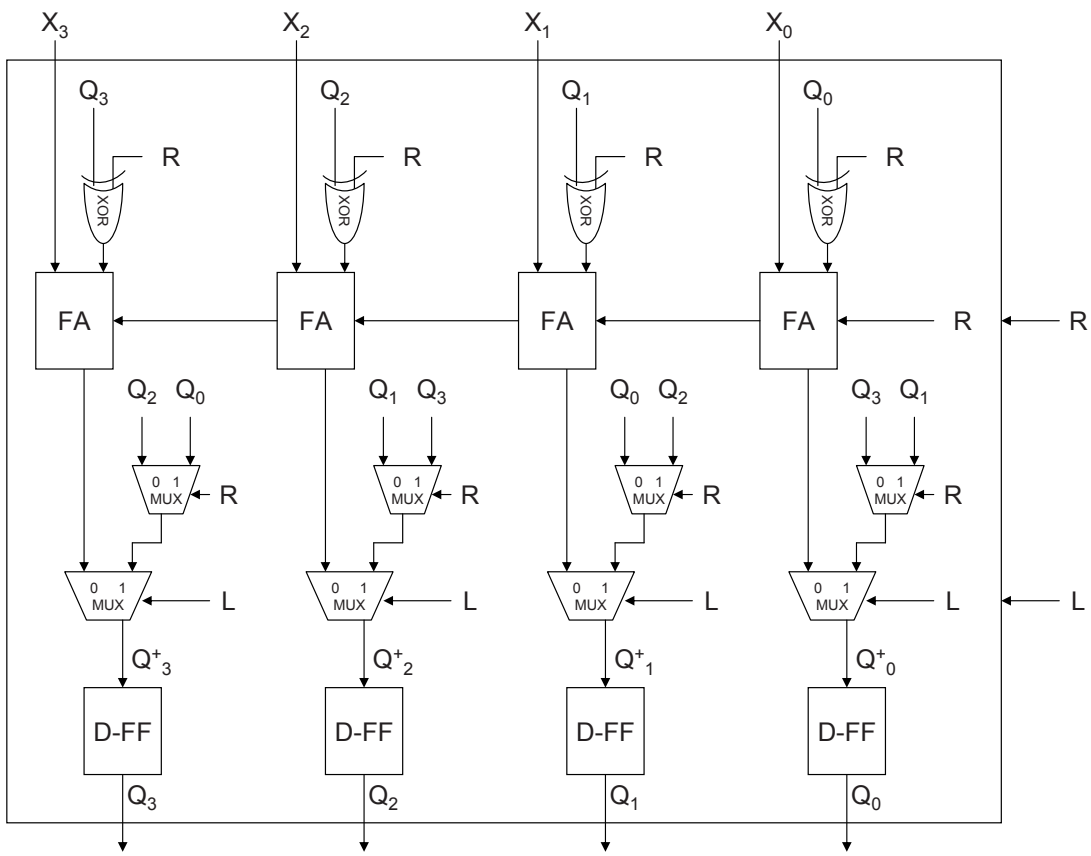
b) Assume initial state is **00**, fill in the following state table. If a state is not reacheable, indicate the appropriate **don't cares** (use "X" to indicate don't cares).

	$S_1{}^+S_0{}^+$				
S_1S_0	$AB = 00$	01	10	11	F
00					
01					
10					
11					

c) With initial state = **00**, what states, if any, are **not** reacheable?

3) Arithmetic/logic and registers

Consider the following diagram. To avoid drawing many messy wires, the **name** of a wire is used in many cases instead. For example, the output of the far right D-FF, Q_0, is connected to the input of the far right XOR gate.



Given the following inputs (L, R, $X_3X_2X_1X_0$) and flip-flop values ($Q_3Q_2Q_1Q_0$), what will be the new flip flop values ($Q_3^+Q_2^+Q_1^+Q_0^+$) ?

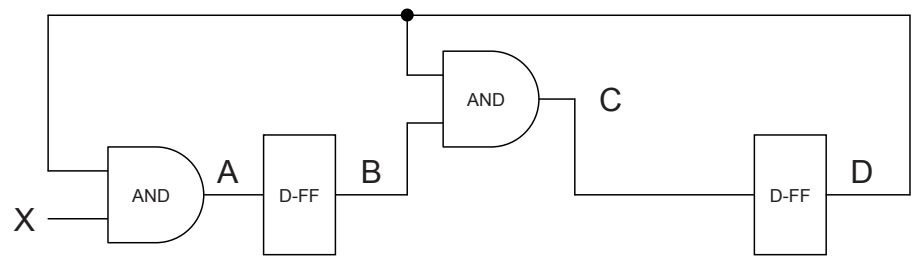
LR	$X_3X_2X_1X_0$	$Q_3Q_2Q_1Q_0$	$Q_3^+Q_2^+Q_1^+Q_0^+$
00	0100	0011	
01	0100	0011	
10	0100	0011	
11	0100	0011	

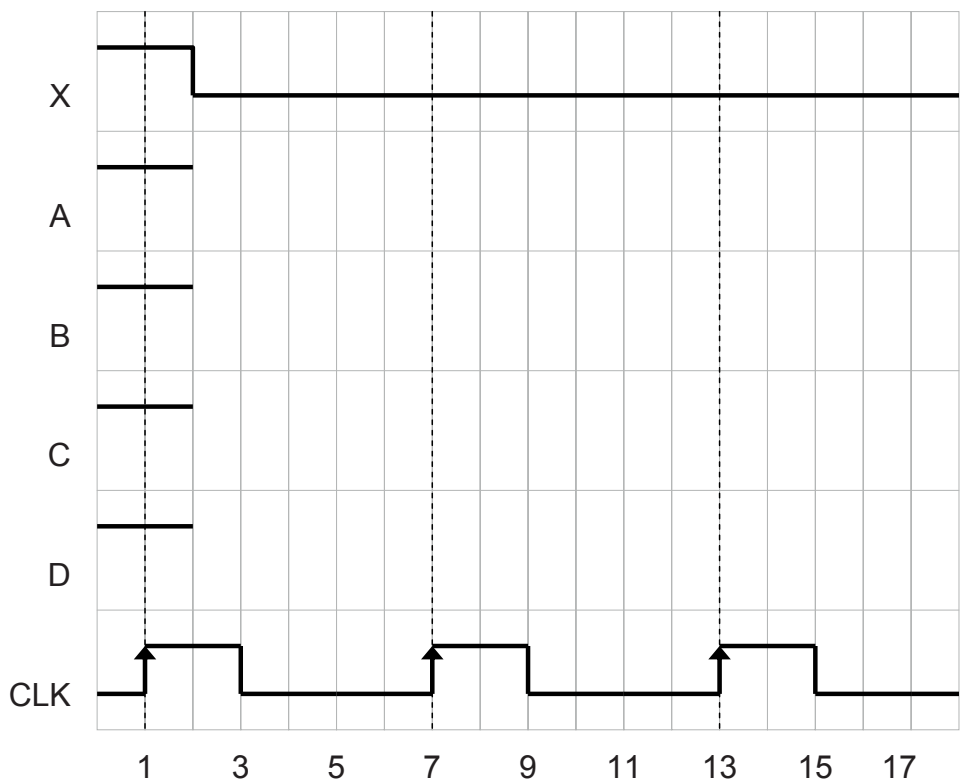
4) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delay for 2-AND is **2 ns**, assume the positive edge-trigged flip-flop delay is $T_{delay_{FF}} = \mathbf{1}$ **ns**, and assume the positive edge-trigged flip-flop setup time is also $T_{setupFF} = \mathbf{1}$ **ns**.

Fill out the rest of the timing diagram for A, B, C, and D.

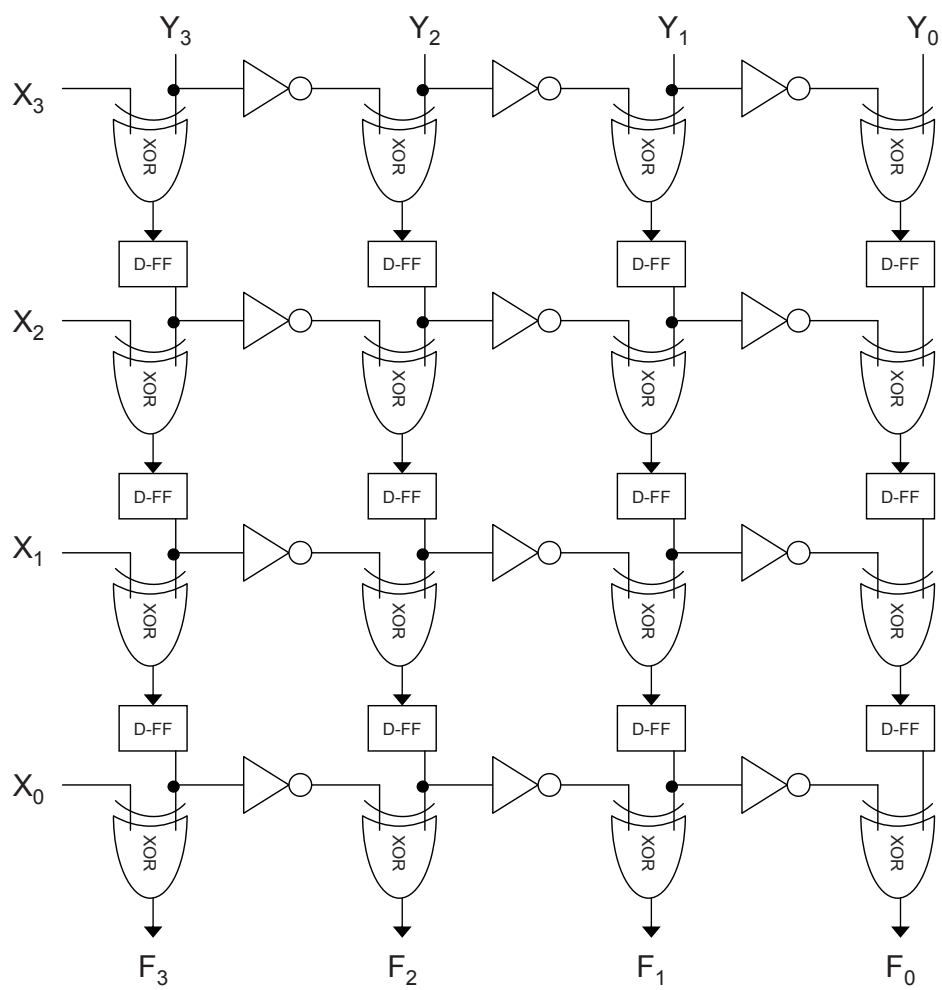




5) Clock period analysis

Consider the following sequential logic diagram where X_3, X_2, X_1, X_0, and Y_3, Y_2, Y_1, Y_0 are **external inputs**, and F_3, F_2, F_1, F_0 are **external outputs**.

Assume the gate delay for 2-XOR is **3 ns**, assume the gate delay for INVERTER is **1 ns**, assume the positive edge-trigged flip-flop delay is $T_{delay_{FF}}$ = **1 ns**, and assume the positive edge-trigged flip-flop setup time is also $T_{setupFF}$ = **1 ns**.

What is the **minimum clock period** that would satisfy these delays? Please explain how you computed the clock period (e.g. give the equation).

Clock period =