

1) Number representation

For each binary vector below, what does it represent if it is interpreted as a Decimal number in conventional binary form (positive only), a Decimal number in 2's complement form (positive and negative), an Octal number, and a Hexadecimal number?

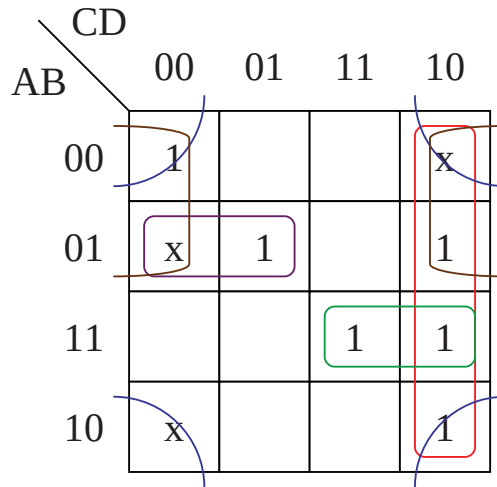
Binary	Decimal		Octal	Hexadecimal
	conventional form	2's complement form		
001111	15	15	17	0F (just "F" also OK)
100000	32	-32	40	20
111111	63	-1	77	3F
100110	38	-26	46	26

2) Two-level logic minimization

$$F(A, B, C, D) = \sum m(0, 5, 6, 10, 14, 15)$$

$$d(A, B, C, D) = \sum m(2, 4, 8)$$

Answer:



a) Identify all the prime and essential prime implicants.

Prime	Essential
— — 10 $C\bar{D}$	
— 0 — 0 $\bar{B}\bar{D}$	
0 — — 0 $\bar{A}\bar{D}$	
111— ABC	X
010— $\bar{A}B\bar{C}$	X

b) Find the minimum two-level logic implementation.

$$F = ABC + \bar{A}B\bar{C} + C\bar{D} + \bar{B}\bar{D} \quad \text{OR}$$

$$F = ABC + \bar{A}B\bar{C} + C\bar{D} + \bar{A}\bar{D} \quad \text{OR}$$

$$F = ABC + \bar{A}B\bar{C} + \bar{B}\bar{D} + \bar{A}\bar{D}$$

3) Multi-level logic minimization

Given following logic equations, minimize the number of literals (e.g. by using common subexpressions, Boolean rules, etc).

$$\begin{aligned}
 H &= \bar{A}BC\bar{E} + \bar{A}BCF \\
 J &= ADE + AD\bar{F} + \bar{B}DE + \bar{B}D\bar{F} + \bar{C}DE + \bar{C}D\bar{F} \\
 K &= \bar{A}BC\bar{E}F + \bar{E}FG + \bar{G} \\
 L &= \bar{A}BC \\
 M &= \bar{E}F
 \end{aligned}$$

Answer:

$$\begin{aligned}
 H &= \bar{A}BC\bar{E} + \bar{A}BCF \\
 &= \bar{A}BC(\bar{E} + F) \\
 &= L(\bar{E} + F) \\
 J &= ADE + AD\bar{F} + \bar{B}DE + \bar{B}D\bar{F} + \bar{C}DE + \bar{C}D\bar{F} \\
 &= AD(E + \bar{F}) + \bar{B}D(E + \bar{F}) + \bar{C}D(E\bar{F}) \\
 &= (AD + \bar{B}D + \bar{C}D)(E + \bar{F}) \\
 &= D(A + \bar{B} + \bar{C})(E + \bar{F}) \\
 &= D\bar{L}\bar{M} \\
 K &= \bar{A}BC\bar{E}F + \bar{E}FG + \bar{G} \\
 &= \bar{A}BC\bar{E}F + \bar{E}F + \bar{G} \\
 &= \bar{E}F + \bar{G} \\
 &= M + \bar{G} \\
 L &= \bar{A}BC \\
 M &= \bar{E}F
 \end{aligned}$$

Final answer with 13 literals

$$\begin{aligned}
 H &= L(\bar{E} + F) \\
 J &= D\bar{L}\bar{M} \\
 K &= M + \bar{G} \\
 L &= \bar{A}BC \\
 M &= \bar{E}F
 \end{aligned}$$

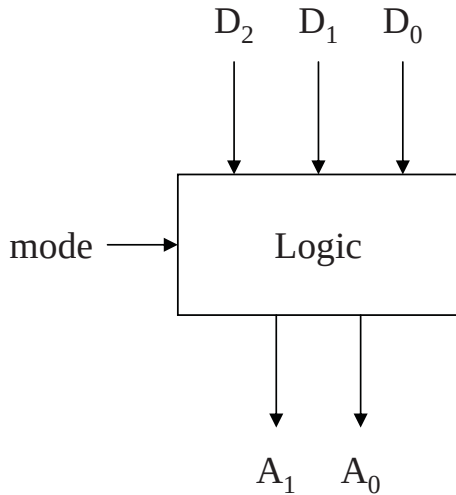
Note that, using De Morgan's law, we can use

$$\begin{aligned}
 \bar{L} &= A + \bar{B} + \bar{C} \\
 \bar{M} &= E + \bar{F}
 \end{aligned}$$

4) Logic design

Specify the truth table (i.e. output = $\{0, 1, x\}$) for the design problem below.

Answer:



mode	D_2	D_1	D_0	A_1	A_0
0	0	0	0	xx	
0	0	0	1	00	
0	0	1	0	01	
0	0	1	1	01	
0	1	0	0	10	
0	1	0	1	10	
0	1	1	0	10	
0	1	1	1	10	
1	0	0	0	00	
1	0	0	1	01	
1	0	1	0	01	
1	0	1	1	10	
1	1	0	0	01	
1	1	0	1	10	
1	1	1	0	10	
1	1	1	1	11	

If $mode = 0$:

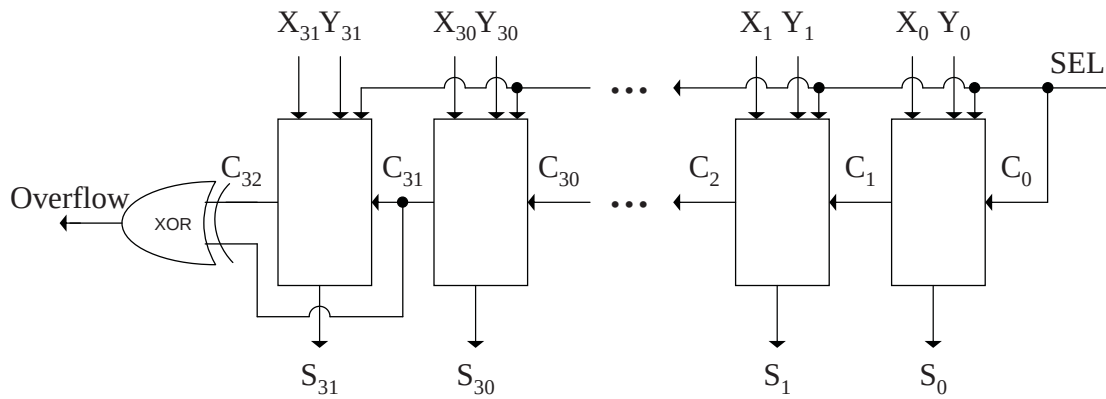
- The outputs A_1A_0 represent the index of the **most significant** input bit D_i that has a value equal to 1. For example, if D_2 is the most significant input bit with value 1, then $A_1A_0 = 10$ (i.e. $A_1 = 1, A_0 = 0$), which is the binary index for 2. If D_1 is the most significant input bit with value 1, then $A_1A_0 = 01$.
- If all inputs have value 0, then the outputs A_1A_0 can be anything.

If $mode = 1$:

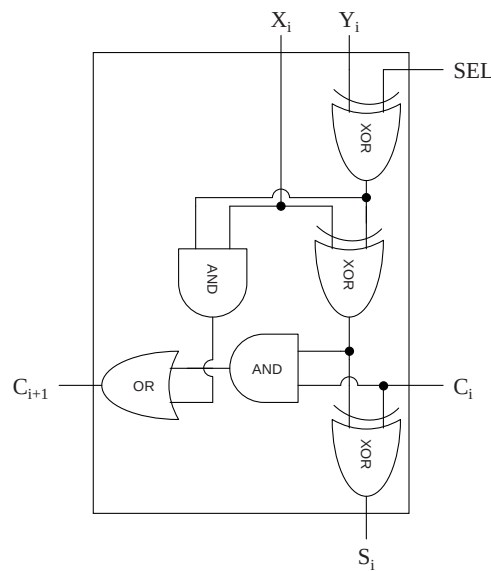
- The outputs A_1A_0 represent the number of input bits (D_2, D_1, D_0) set to "1". For example, if $D_2D_1D_0 = 111$, then $A_1A_0 = 11$ to indicate that there are three 1's.

5) Delay analysis

Consider the 32-bit ripple carry adder/subtractor shown below. Assume **3ns** gate delay for 2-XOR and **1ns** gate delay for 2-AND and 2-OR.



The logic for each bitslice (rectangle box) is as follows:



What are final delays for the following:

$$\begin{aligned} S_1 &= 11 \\ S_{30} &= 69 \\ S_{31} &= 71 \\ \text{Overflow} &= 73 \end{aligned}$$

$$\begin{aligned} C_1 &= 8 \\ C_{30} &= 66 \\ C_{31} &= 68 \end{aligned}$$