

1) Sequential logic implementation

Consider the following incompletely-specified Moore machine (“*” indicates don’t cares).

S_1S_0	$S_1^+S_0^+$		F
	$I = 0$	$I = 1$	
A	A	C	1
B	C	A	0
C	B	*	0

Suppose we use the following state encoding.

State	S_1S_0
A	01
B	11
C	00

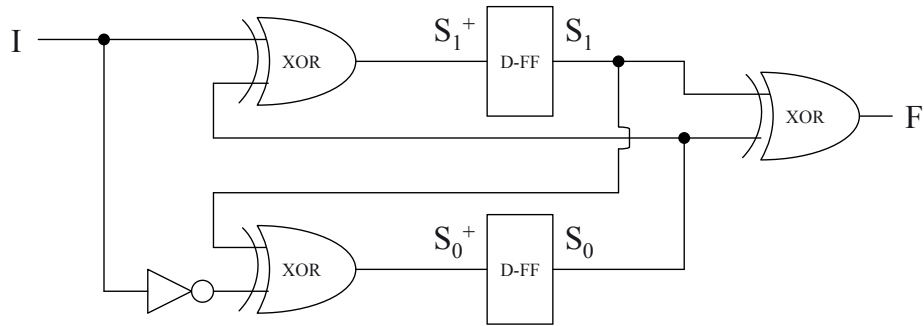
Derive the **minimum** two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

$F = \bar{S}_1S_0$ $S_1^+ = \bar{S}_0$ $S_0^+ = \bar{I}\bar{S}_1 + IS_1$	F		
	S_0	0	1
	S_1	0	1
	1	*	0

S_1^+				
S_1S_0	00	01	11	10
I	00	01	11	10
00	1	0	0	*
01	*	0	0	*

S_0^+				
S_1S_0	00	01	11	10
I	00	01	11	10
00	1	1	0	*
01	*	0	1	*

2) Reverse engineer sequential circuit to finite state machine



a) Fill out the following functions (OK to use $\oplus$ in functions).

$$\begin{aligned} F &= S_1 \oplus S_0 \\ S_1^+ &= I \oplus S_0 \\ S_0^+ &= \bar{I} \oplus S_1 \end{aligned}$$

b) Assume initial state is **11**, fill in the following state table. If a state is not reachable, indicate the appropriate **don't cares** (use "*" to indicate don't cares).

$S_1 S_0$	$S_1^+ S_0^+$		F
	$I = 0$	$I = 1$	
00	01	10	0
01	11	00	1
10	00	11	1
11	10	01	0

c) With initial state = **11**, what states, if any, are **not** reachable?

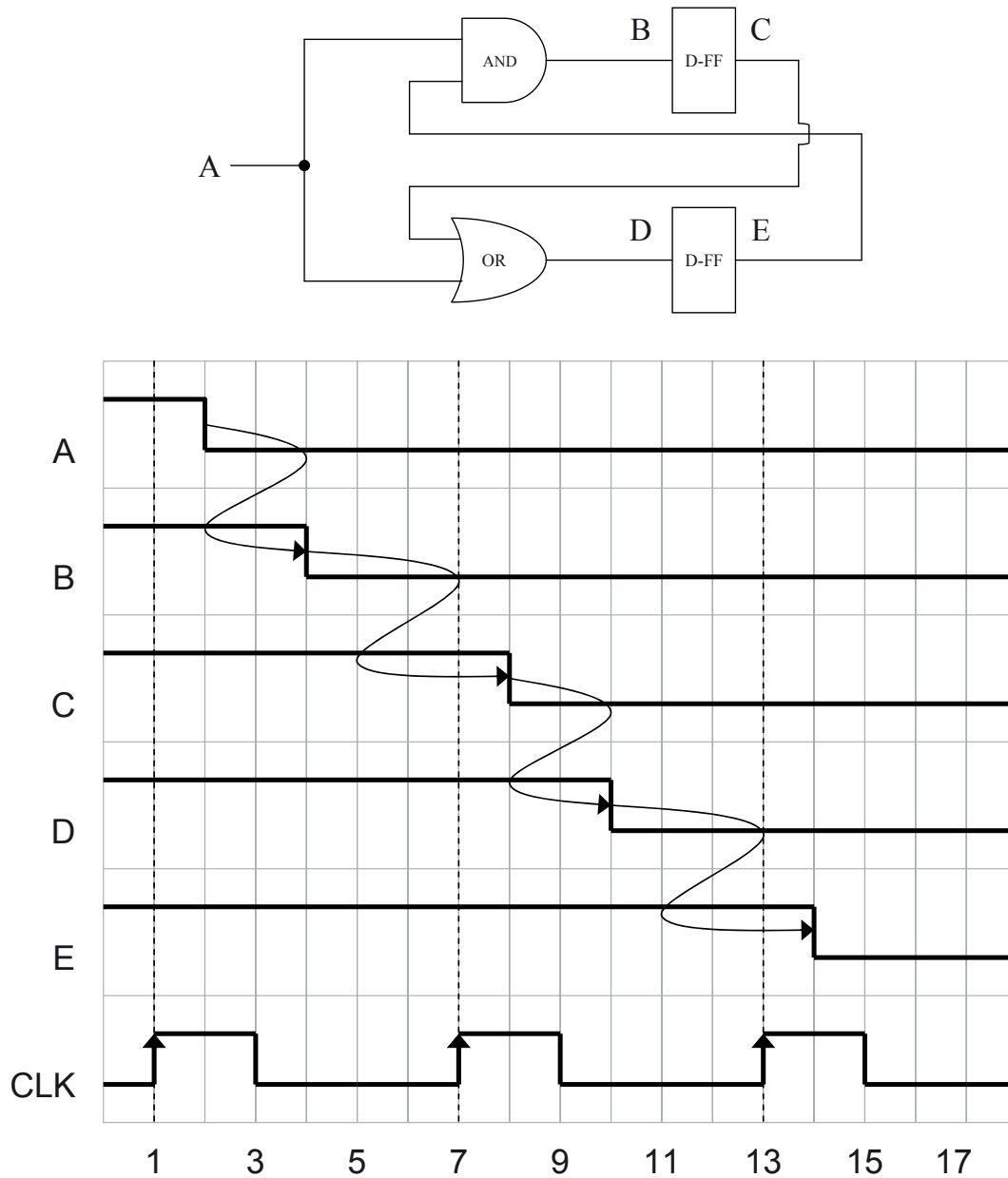
None are unreachable.

3) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delay is **2 ns** for both 2-AND and 2-OR. assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = 1 \text{ ns}$, and assume the positive edge-triggered flip-flop setup time is also $T_{setup_{FF}} = 1 \text{ ns}$.

Fill out the rest of the timing diagram for A , B , C , D , and E .



4) Clock period analysis

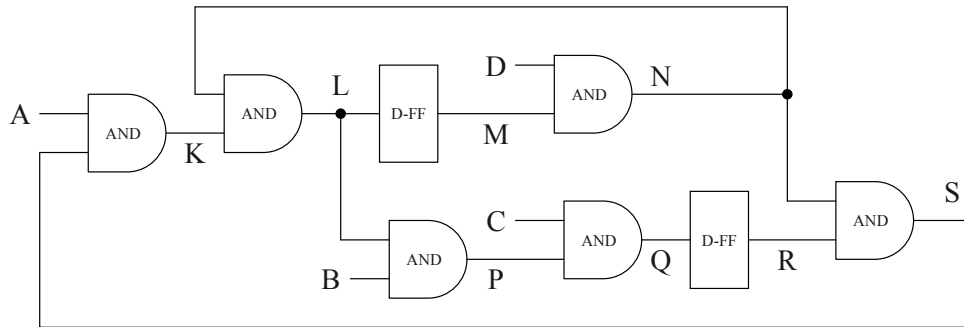
Consider the following sequential logic diagram where A , B , C , and D are **external inputs**.

Assume the gate delay for 2-AND is **2 ns**, assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = \mathbf{1\ ns}$, and assume the positive edge-triggered flip-flop setup time is also $T_{setup_{FF}} = \mathbf{1\ ns}$.

What is the **minimum clock period** that would satisfy these delays? Provide the critical path.

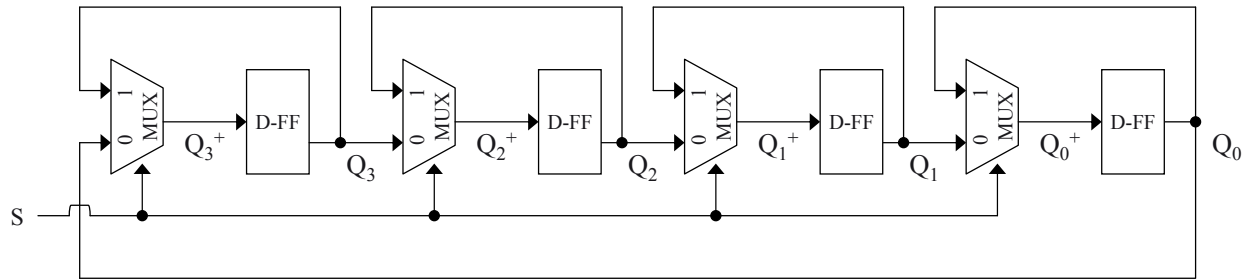
Clock period = 14 ns

Critical path = $M \rightarrow N \rightarrow S \rightarrow K \rightarrow L \rightarrow P \rightarrow Q$



5) Datapath/registers

Consider the following diagram.



Given the values for input S and flip-flop values $(Q_3Q_2Q_1Q_0)$, what will be the new flip flop values $(Q_3^+Q_2^+Q_1^+Q_0^+)$?

S	$Q_3Q_2Q_1Q_0$	$Q_3^+Q_2^+Q_1^+Q_0^+$
0	1011	1101
0	0111	1011
1	1010	1010
1	1100	1100