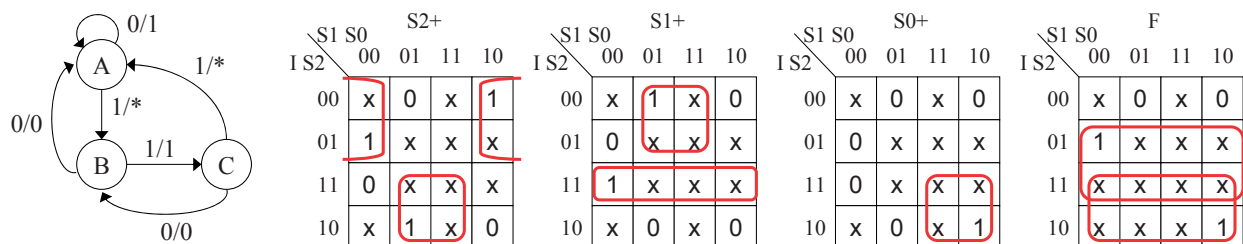


1) Sequential logic implementation

Consider the following incompletely-specified Mealy machine (“*” indicates don’t cares).



Suppose we use the following state encoding. (Assume the name the input variable is I .)

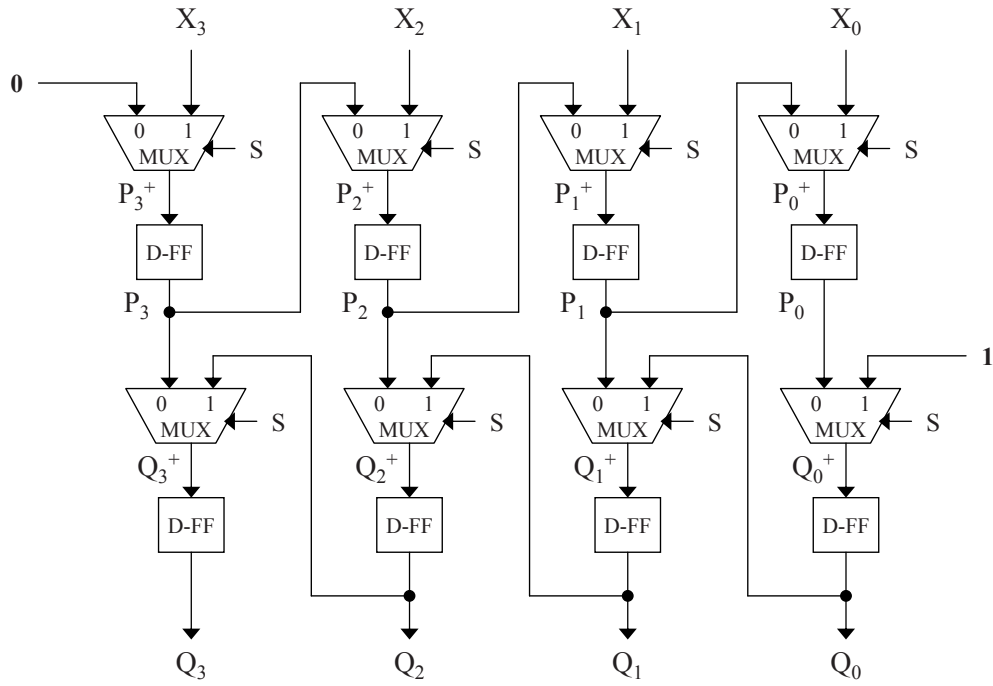
State	$S_2S_1S_0$
A	100
B	010
C	001

Derive the **minimum** two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

$$\begin{aligned}
 F &= I + S_2 \\
 S_2^+ &= \bar{I}\bar{S}_0 + IS_0 = I \oplus S_0 \quad \text{either is OK} \\
 S_1^+ &= \bar{I}S_0 + IS_2 \\
 S_0^+ &= IS_1
 \end{aligned}$$

2) Datapath/registers

Consider the following diagram.



Given the values for control input S , the data inputs $X_3X_2X_1X_0$, and the flip-flop values $P_3P_2P_1P_0$ and $Q_3Q_2Q_1Q_0$, what will be the new flip flop values $P_3^+P_2^+P_1^+P_0^+$ and $Q_3^+Q_2^+Q_1^+Q_0^+$?

Note: All MUXes are controlled by the same control input S , and 0 and 1 mean a constant logic value of “false” (“0”) and “true” (“1”), respectively.

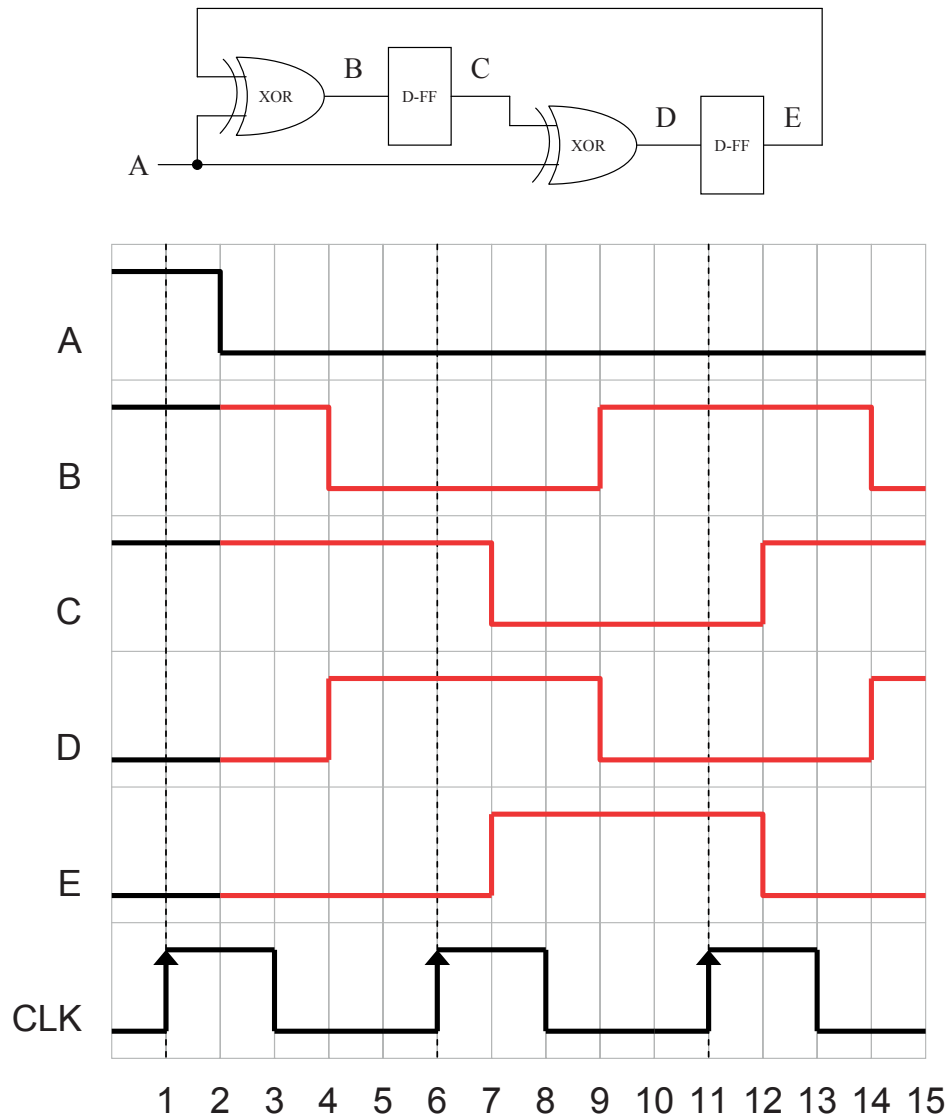
S	$X_3X_2X_1X_0$	$P_3P_2P_1P_0$	$Q_3Q_2Q_1Q_0$	$P_3^+P_2^+P_1^+P_0^+$	$Q_3^+Q_2^+Q_1^+Q_0^+$
0	0000	0100	1111	0010	0100
0	1101	1110	0011	0111	1110
1	0111	1010	1101	0111	1011
1	1000	0000	1011	1000	0111

3) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delay is **2 ns** for both 2-AND and 2-OR. assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = \mathbf{1\ ns}$, and assume the positive edge-triggered flip-flop setup time is also $T_{setup_{FF}} = \mathbf{1\ ns}$.

Fill out the rest of the timing diagram for A , B , C , D , and E .



4) Clock period analysis

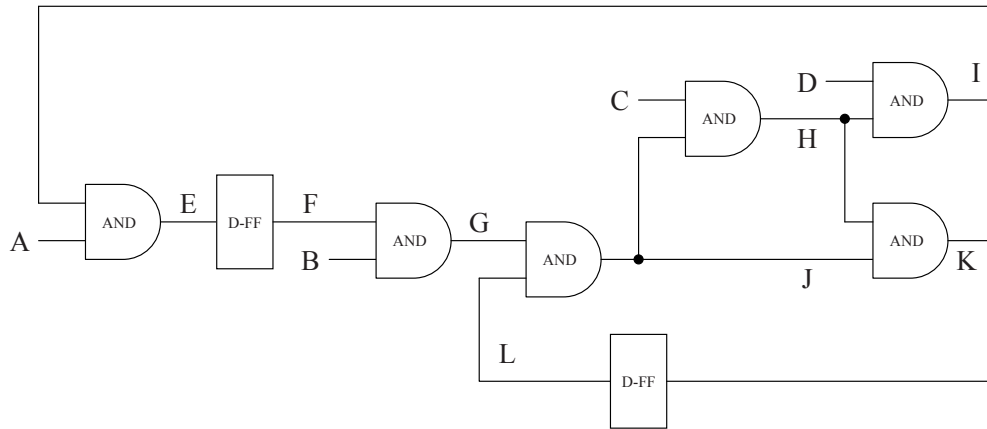
Consider the following sequential logic diagram where A , B , C , and D are **external inputs**.

Assume the gate delay for 2-AND is **2 ns**, assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = \mathbf{1\ ns}$, and assume the positive edge-triggered flip-flop setup time is also $T_{setup_{FF}} = \mathbf{1\ ns}$.

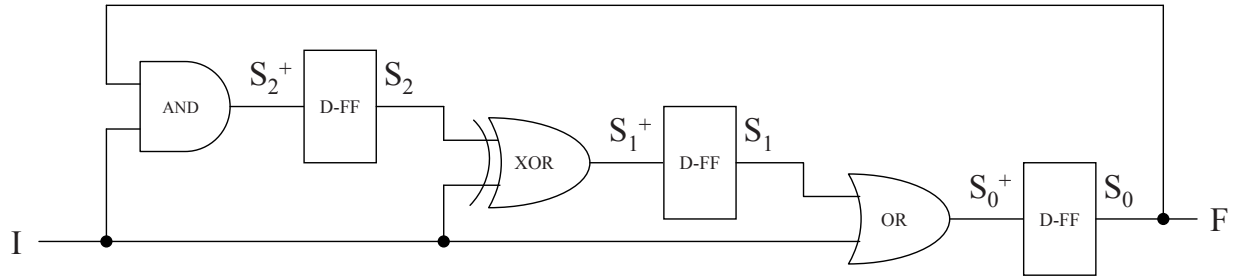
What is the **minimum clock period** that would satisfy these delays? Provide the critical path.

Clock period = 12 ns

Critical path = $F \rightarrow G \rightarrow J \rightarrow H \rightarrow I \rightarrow E$



5) Reverse engineer sequential circuit to finite state machine



a) Fill out the following functions (OK to use $\oplus$ in functions).

$$\begin{aligned} F &= S_0 \\ S_2+ &= IS_0 \\ S_1+ &= I \oplus S_2 \\ S_0+ &= I + S_1 \end{aligned}$$

b) Assume initial state is **000**, fill in the following state table. If a state is not reachable, indicate the appropriate **don't cares** (use "*" to indicate don't cares).

$S_2S_1S_0$	$S_2+S_1+S_0+$		F
	$I = 0$	$I = 1$	
000	000	011	0
001	000	111	1
010	001	011	0
011	001	111	1
100	xxx (010)	xxx (001)	x(0)
101	010	101	1
110	xxx (011)	xxx (001)	x(0)
111	011	101	1

c) With initial state = **000**, what states, if any, are **not** reachable?

100, 110