
1) Number representation

a) Represent these numbers in 6-bit signed 2's complement form or indicate that it is not possible.

-1	111111
-7	111001
63	not possible
-5	111011
34	not possible
-32	100000

b) For each binary vector below, what does it represent in Octal and Hexadecimal?

Binary	Octal	Hexadecimal
101111	57	2F
110000	60	30
011110	36	1E

2) Two-level logic minimization

$$F(A, B, C, D) = \sum m(1, 6, 7, 10, 11, 12, 13)$$

$$d(A, B, C, D) = \sum m(0, 3, 5, 9, 15)$$

		CD			
		00	01	11	10
AB	00	x	1	x	
	01		x	1	1
	11	1	1	x	
	10		x	1	1

a) Identify all the prime and essential prime implicants.

Primes (including Essentials)		Essential Primes Only
—1	D	
000-	$\bar{A}\bar{B}\bar{C}$	
011-	$\bar{A}BC$	X
110-	$AB\bar{C}$	X
101-	$A\bar{B}C$	X

b) Find the minimum two-level logic implementation.

$$F = \bar{A}BC + AB\bar{C} + A\bar{B}C + D$$

3) Multi-level logic minimization

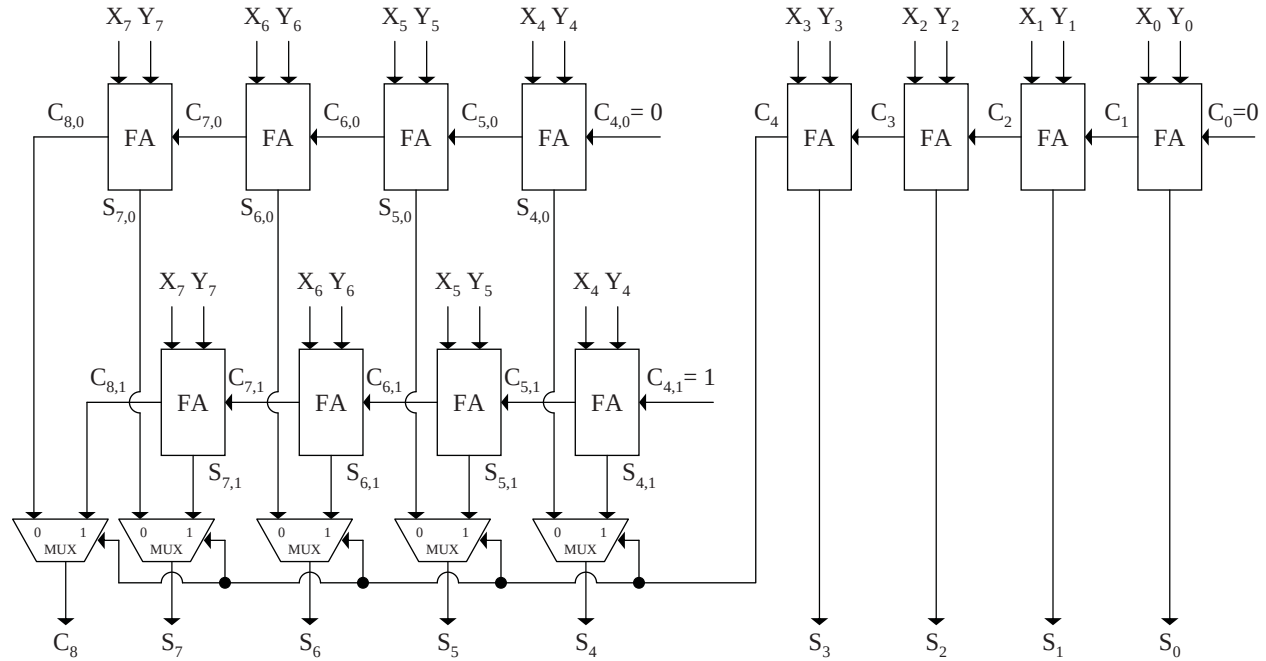
Given following logic equations, minimize the number of literals, e.g. by using common subexpressions, Boolean rules, etc. You can introduce new immediate equations for common sub-expressions if it helps to reduce the number of literals. Put a box around your final answer, and indicate the number of literals in your final answer.

$$\begin{aligned}P &= (\bar{A} + \bar{B} + \bar{C})(D + C + \bar{C}) \\&= (\bar{A} + \bar{B} + \bar{C})(D + 1) \\&= \bar{A} + \bar{B} + \bar{C} \\Q &= ABC\bar{D} + ABC\bar{E} + ABC\bar{F} \\&= ABC(\bar{D} + \bar{E} + \bar{F}) \\&= \bar{P}\bar{R} \\R &= \bar{B}DEF + CDEF + DEF \\&= DEF(\bar{B} + C + 1) \\&= DEF \\S &= A\bar{B}(\bar{A} + B) \\&= 0 \\T &= DEF + (\bar{A} + \bar{B} + \bar{C})(\bar{D} + \bar{E} + \bar{F}) \\&= R + P\bar{R} \\&= R + P \\&= \bar{Q}\end{aligned}$$

9 literals in total.

4) Delay analysis

Consider the following 8-bit Carry Select Adder design that adds the numbers $F = X + Y$. Assume **1ns** gate delay for all gates (i.e., 2-XOR, 2-AND, 2-OR, and 2-input MUX).



What are final delays for the following:

$$S_0 = 2\text{ns}$$

$$S_2 = 6\text{ns}$$

$$S_4 = 10\text{ns}$$

$$S_6 = 10\text{ns}$$

$$C_8 = 10\text{ns}$$

$$S_1 = 4\text{ns}$$

$$S_3 = 8\text{ns}$$

$$S_5 = 10\text{ns}$$

$$S_7 = 10\text{ns}$$

The logic for each bitslice (rectangle box) is as follows:

