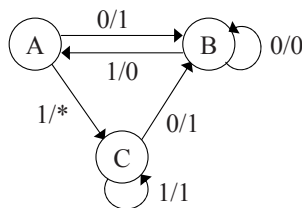


1) Sequential logic implementation

Consider the following incompletely-specified Mealy machine (“*” indicates don’t cares).



Suppose we use the following state encoding. (Assume the name the input variable is I .)

State	$S_1 S_0$
A	00
B	10
C	01

Derive the **minimum** two-level logic for each of the following (you should minimize each logic function separately, no need to worry about sharing logic between logic functions).

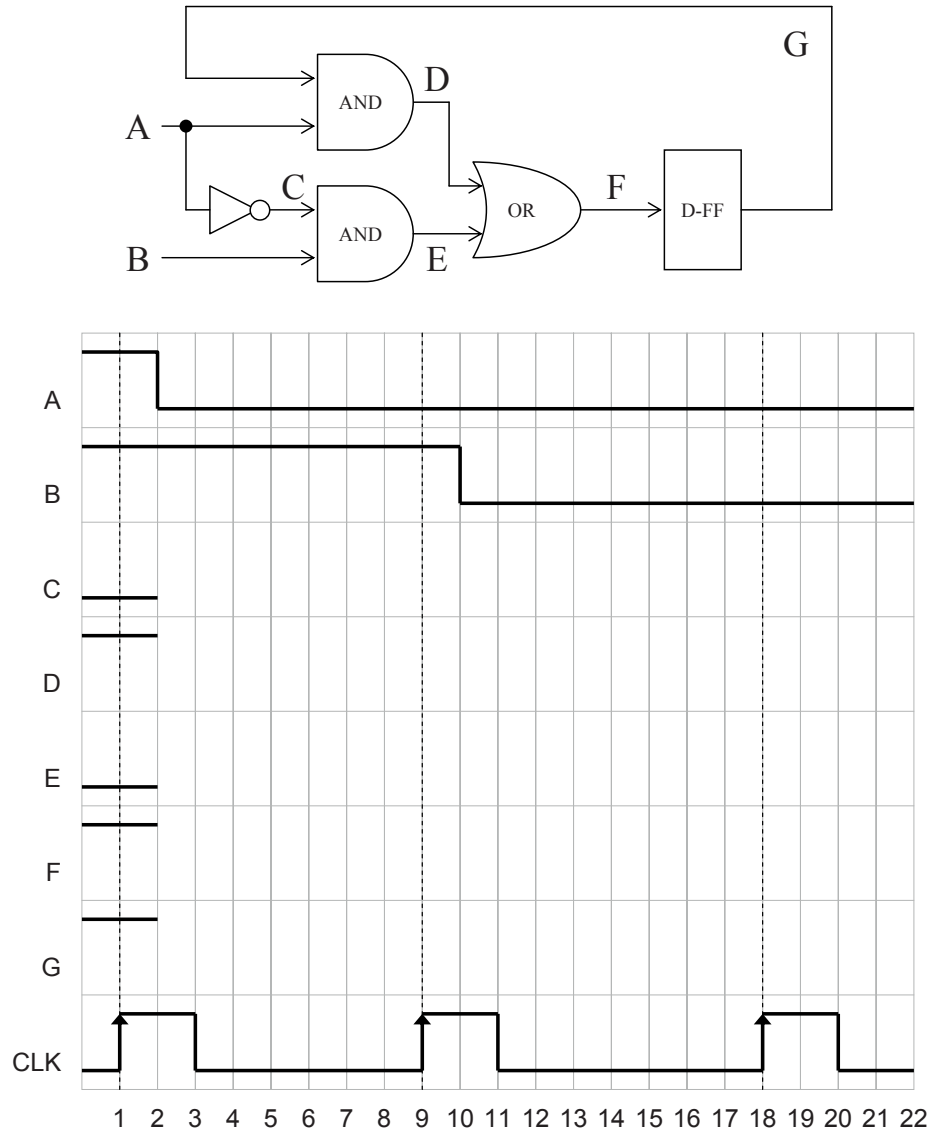
$$\begin{aligned}
 F &= \\
 S_1^+ &= \\
 S_0^+ &=
 \end{aligned}$$

2) Timing analysis

Consider the following sequential logic diagram.

Assume the gate delays are **2 ns** for 2-AND and 2-OR gates and **1 ns** for inverters. Assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = 1 \text{ ns}$, and setup time is also $T_{setup_{FF}} = 1 \text{ ns}$.

Fill out the rest of the timing diagram for A , B , C , D , E , F , and G .



3) Clock period analysis

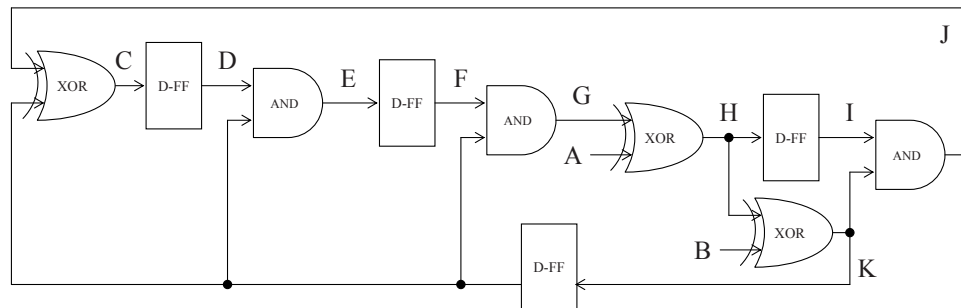
Consider the following sequential logic diagram where A and B are **external inputs**.

Assume the gate delay is **2 ns** for a 2-AND gate and **3 ns** for a 2-XOR gate. assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = 1 \text{ ns}$, and setup time is also $T_{setup_{FF}} = 1 \text{ ns}$.

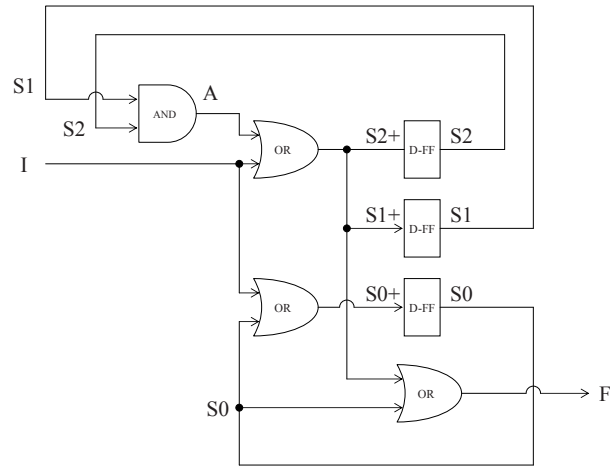
What is the **minimum clock period** that would satisfy these delays? Provide the critical path.

Clock period =

Critical path =



4) Reverse engineer sequential circuit to finite state machine



a) Fill out the following functions.

$$\begin{aligned}
 F &= \\
 S_2+ &= \\
 S_1+ &= \\
 S_0+ &=
 \end{aligned}$$

b) Assume initial state is **000**, draw the state diagram. **Important: Only include reachable states in the diagram.**

c) With initial state = **000**, what states, if any, are **not** reachable?