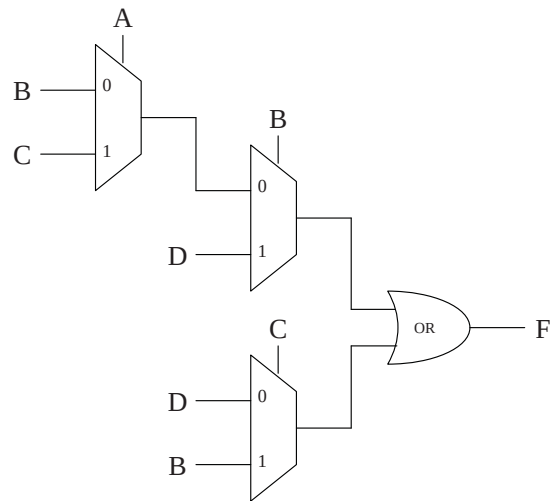


1) Two-level logic minimization

Consider the logic diagram shown below.



a) Please fill out the following K-map for F as a function of A , B , C , and D .

		F				
		CD	00	01	11	10
AB	00		1			
	01		1	1	1	
	11		1	1	1	
	10		1	1	1	

b) For the K-map derived in part (a) for F , specify all the primes and essential primes.

Prime	Essential
1 - - 1 AD	
- 1 - 1 BD	
1 - 1 - AC	X
- 1 1 - BC	X
- - 0 1 $\bar{C}D$	X

c) Find the minimum two-level logic implementation for F .

$$F = AC + BC + \bar{C}D$$

2) Number representation

a) For each binary vector below, what does it represent as an Octal number and a Hexadecimal number?

Binary	Octal	Hexadecimal
00111110	076	3E
10100001	241	A1
00111001	071	39

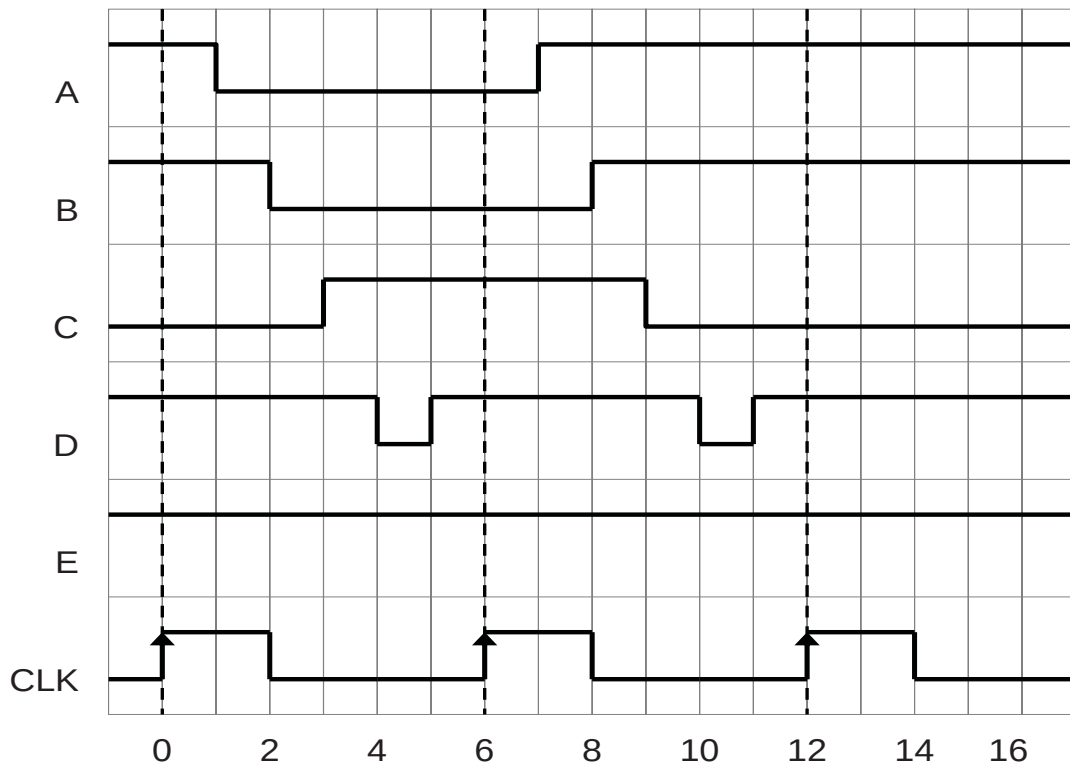
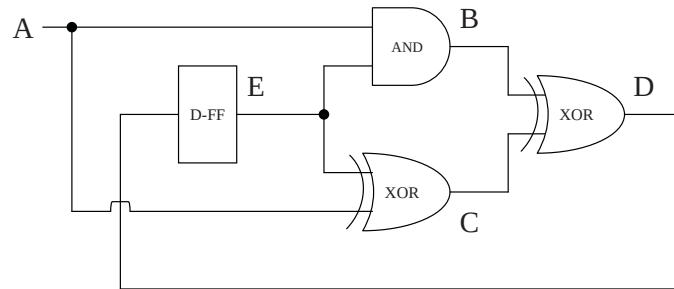
b) Given X and Y below that are 5-bit numbers in 2's complement form, fill in the table of what S should be bit-vector form (**even if the result causes an overflow**). Indicate whether or not there is an *overflow* and what S is as a number (if S results in an overflow, then just put an "x" under the " S as a number" column). (First two rows provide examples.)

X $x_4x_3x_2x_1x_0$	Y $y_4y_3y_2y_1y_0$	$S = X - Y$ $s_4s_3s_2s_1s_0$	Overflow?	S as a number
11101	00011	11010	no	-6
00001	00111	11010	no	-6
11100	11001	00011	no	3
01000	10101	10011	yes	x
10110	00011	10011	no	-13
11000	01011	01101	yes	x

3) Timing analysis

Consider the following sequential logic diagram. Assume the gate delay is **1 ns** for 2-AND and **2 ns** for 2-XOR. Assume the positive edge-triggered flip-flop delay is $T_{delay_{FF}} = \mathbf{1\ ns}$, and Assume the positive edge-triggered flip-flop setup time is also $T_{setup_{FF}} = \mathbf{1\ ns}$.

Fill out the rest of the timing diagram for *B*, *C*, *D*, and *E*.



4) Sequential logic implementation

Consider the following Mealy machine with initial state A . (“ x ” means don’t care.)

$S_2 S_1 S_0$	$S_2^+ S_1^+ S_0^+$		F	
	$I = 0$	$I = 1$	$I = 0$	$I = 1$
A	C	D	0	x
B	A	C	1	1
C	D	C	1	0
D	D	B	x	1

Assume the following state encoding.

State	$S_2 S_1 S_0$
A	000
B	011
C	100
D	010

a) For output F , fill-in K-Map.

		F			
		$S_1 S_0$	00	01	11
$I S_2$	00		x	1	x
	01	1	x	x	x
	11		x	x	x
	10	x	x	1	1

b) Derive the **minimum** two-level logic for the output F .

$$F = \bar{I}S_2 + S_1$$

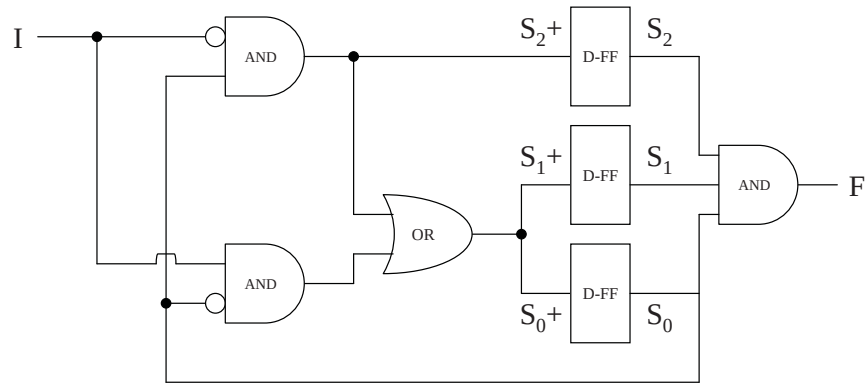
5) Multi-level logic minimization

Given following logic equations, minimize the number of literals, e.g. by using common subexpressions, Boolean rules, etc. You can introduce new immediate equations for common sub-expressions if it helps to reduce the number of literals. Put a box around your final answer, and indicate the number of literals in your final answer.

$$\begin{aligned}M &= \bar{A}Y + \bar{B}Y + \bar{C}Y + \bar{A}Z + \bar{B}Z + \bar{C}Z + ABCD + ABC\bar{D} \\&= (\bar{A} + \bar{B} + \bar{C})(Y + Z) + ABC(D + \bar{D}) \\&= (\bar{A} + \bar{B} + \bar{C})(Y + Z) + ABC \\&= ABC + Y + Z \\&= N + Y + Z \\&= N + \bar{Q} \\N &= A(\bar{A}D + BC)(Z + \bar{Z} + ZC) \\&= (A\bar{A}D + ABC)(1 + ZC) \\&= ABC \\P &= \bar{A}Z + \bar{B}Z + \bar{C}Z \\&= (\bar{A} + \bar{B} + \bar{C})Z \\&= \bar{N}Z \\Q &= \bar{Y}\bar{Z}\bar{W} + \bar{Y}\bar{Z}W + \bar{Y}\bar{Z}\bar{T} + \bar{Y}\bar{Z}T \\&= \bar{Y}\bar{Z}(\bar{W} + W + \bar{T} + T) \\&= \bar{Y}\bar{Z}\end{aligned}$$

Final answer: 9 literals

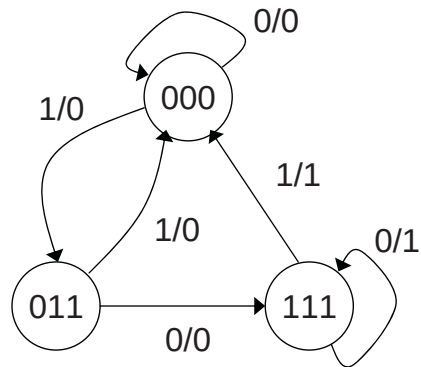
6) Reverse engineer sequential circuit to finite state machine



a) Fill out the following functions.

$$\begin{aligned} F &= S_2 S_1 S_0 \\ S_2^+ &= \bar{I} S_0 \\ S_1^+ &= I \bar{S}_0 + S_2^+ \\ S_0^+ &= S_1^+ \end{aligned}$$

b) Assume initial state is **000**, draw the state diagram. **Important: Only include reachable states in the diagram.**

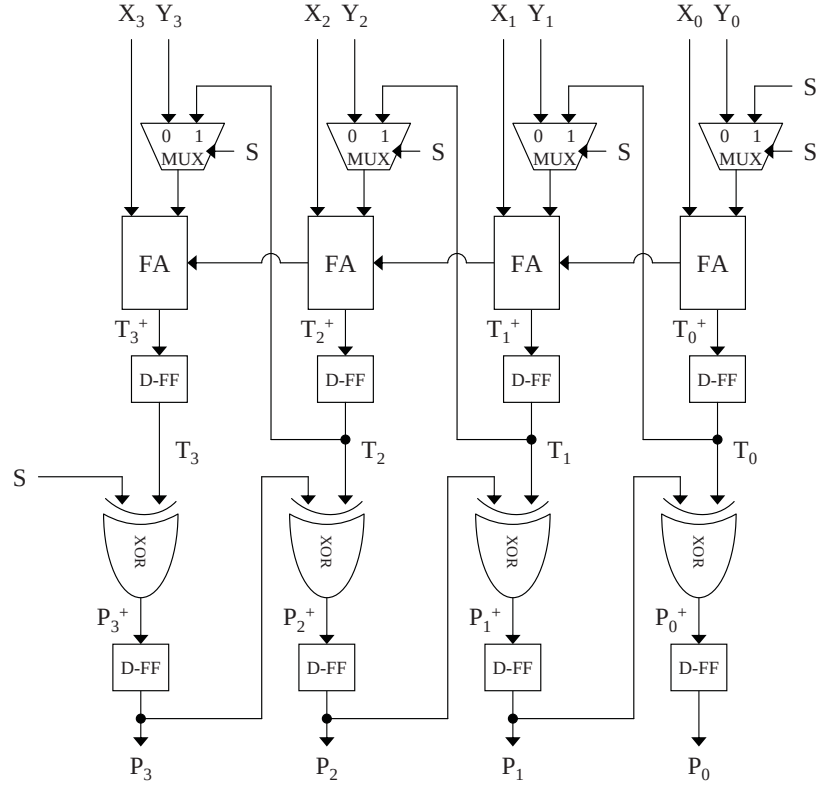


c) With initial state = **000**, what states, if any, are **not** reachable?

001, 010, 100, 101, 110

7) Datapath/registers

Consider the following diagram.



Given the values for control input S , the data inputs $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$, and the flip-flop values $T_3T_2T_1T_0$ and $P_3P_2P_1P_0$, what will be the new flip flop values $T_3^+T_2^+T_1^+T_0^+$ and $P_3^+P_2^+P_1^+P_0^+$?

S	$X_3X_2X_1X_0$	$Y_3Y_2Y_1Y_0$	$T_3T_2T_1T_0$	$P_3P_2P_1P_0$	$T_3^+T_2^+T_1^+T_0^+$	$P_3^+P_2^+P_1^+P_0^+$
0	0111	0011	1111	0000	1010	1111
0	1010	0010	0001	0010	1100	0000
1	1000	1001	0011	1111	1111	1100
1	1100	1001	0000	0000	1101	1000

8) Delay analysis

Consider the following 4×4 “two-dimensional arbiter” with inputs $R_{0,0}, R_{0,1}, R_{0,2}, R_{0,3}, R_{1,0}, R_{1,1}, R_{1,2}, R_{1,3}, \dots, R_{3,0}, R_{3,1}, R_{3,2}, R_{3,3}$ (“requests”) and outputs $G_{0,0}, G_{0,1}, G_{0,2}, G_{0,3}, G_{1,0}, G_{1,1}, G_{1,2}, G_{1,3}, \dots, G_{3,0}, G_{3,1}, G_{3,2}, G_{3,3}$ (“grants”).

$W_{i,0}$ ’s and $N_{0,j}$ ’s are also inputs, and $E_{i,4}$ ’s and $S_{4,j}$ ’s are also outputs.

If $R_{i,j} = 1$ **AND** there is no other grant $G_{p,q} = 1$ such that $p = i$ (same row) and $q < j$ (earlier column), or $p < i$ (earlier row) and $q = j$ (same column), then $G_{i,j} = 1$; otherwise, $G_{i,j} = 0$.

The logic in Fig. 1 is designed so that there is at most one $G_{i,j} = 1$ in any given row or column. In Fig. 1, assume all $N_{i,j} = S_{i-1,j}$ and $W_{i,j} = E_{i,j-1}$, with all $N_{0,j} = 1$ and $W_{i,0} = 1$ (no need to simplify the logic).

Assume **1ns** gate delay for all gates (i.e., 2-AND and INV).

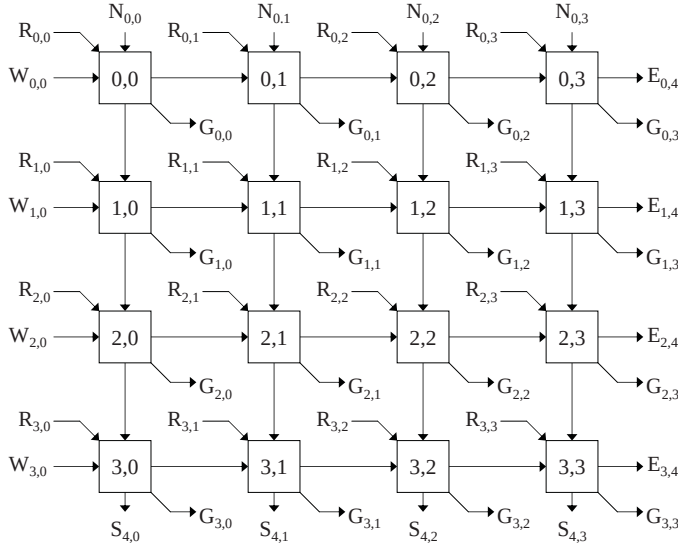


Figure 1: 4×4 two-dimensional arbiter.

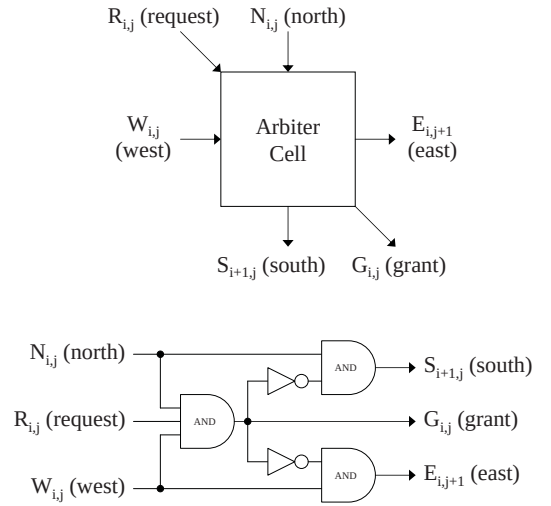


Figure 2: Logic for rectangle box.

a) Which output in Fig. 1 determines the longest delay?

$E_{3,4}$ or $S_{4,3}$

b) What is the longest delay in Fig. 1 (in ns)?

21 ns