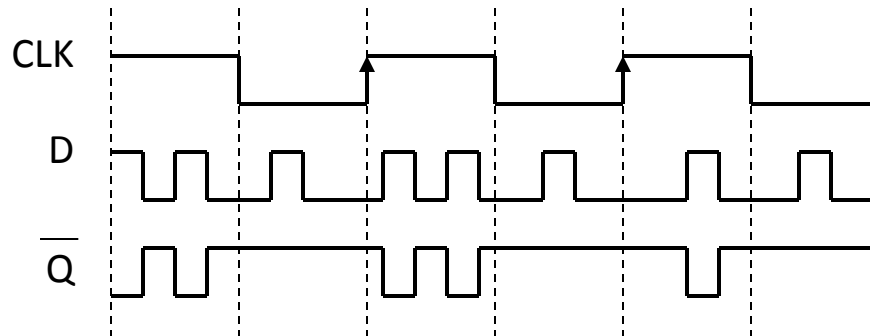
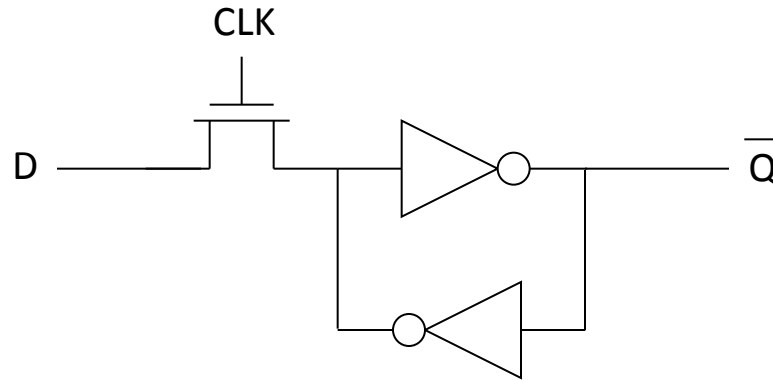


Lecture on Flip-Flops

CSE 140, Fall 11

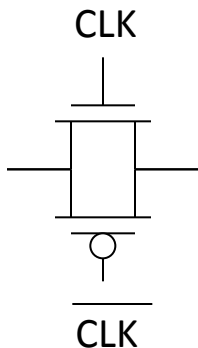
Level-Sensitive Flip-Flop

- Level-sensitive flip-flop (also called a *latch*)
- $\bar{Q}$ changes whenever clock is *high*

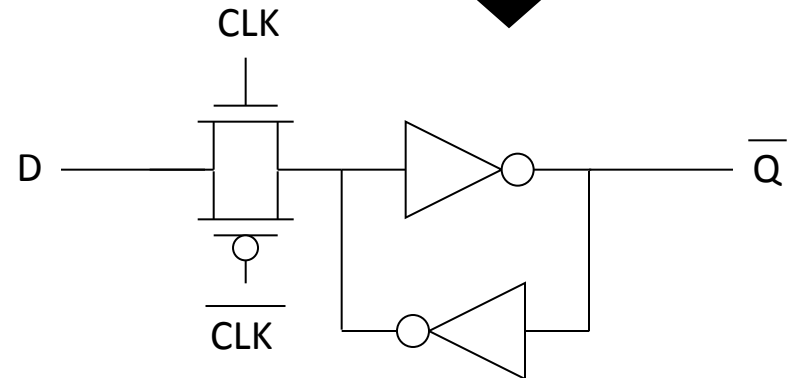
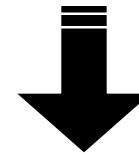
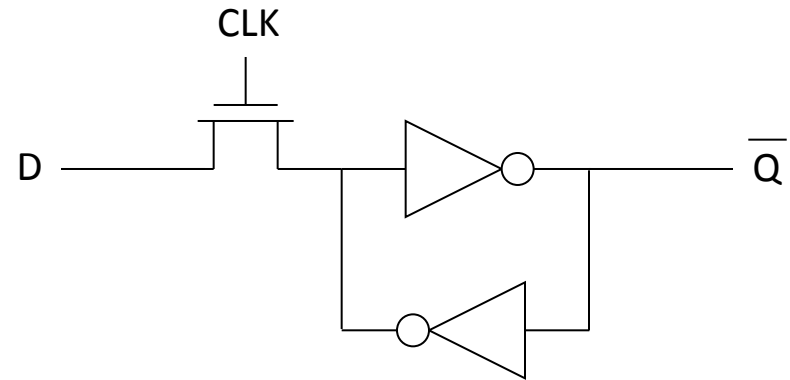


Level-Sensitive Flip-Flop

- NMOS transistor often replaced with *transmission gate*
- *Transmission gate* includes both NMOS and PMOS transistors because NMOS good at passing **0** and PMOS good at passing **1**



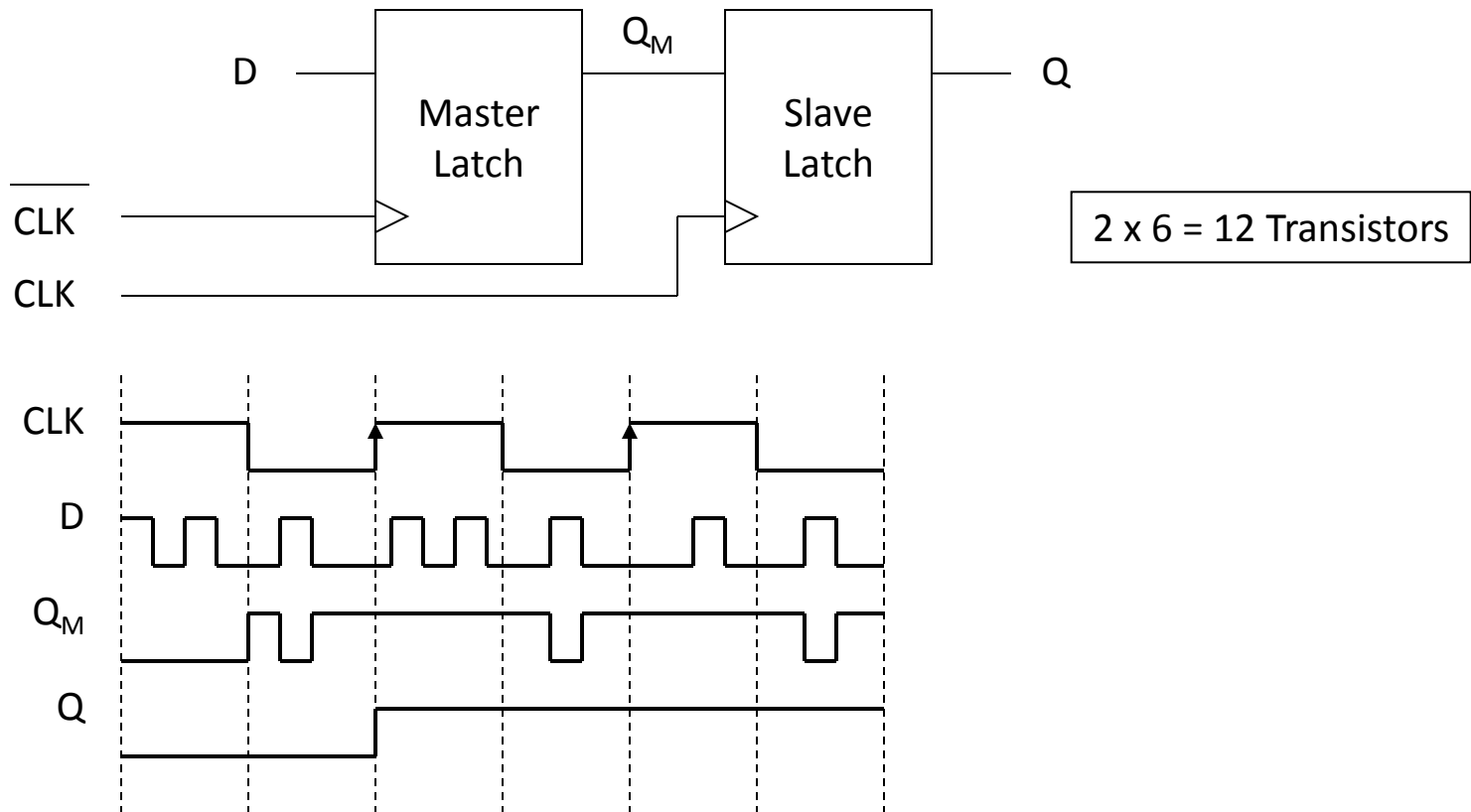
Transmission Gate



6 Transistors

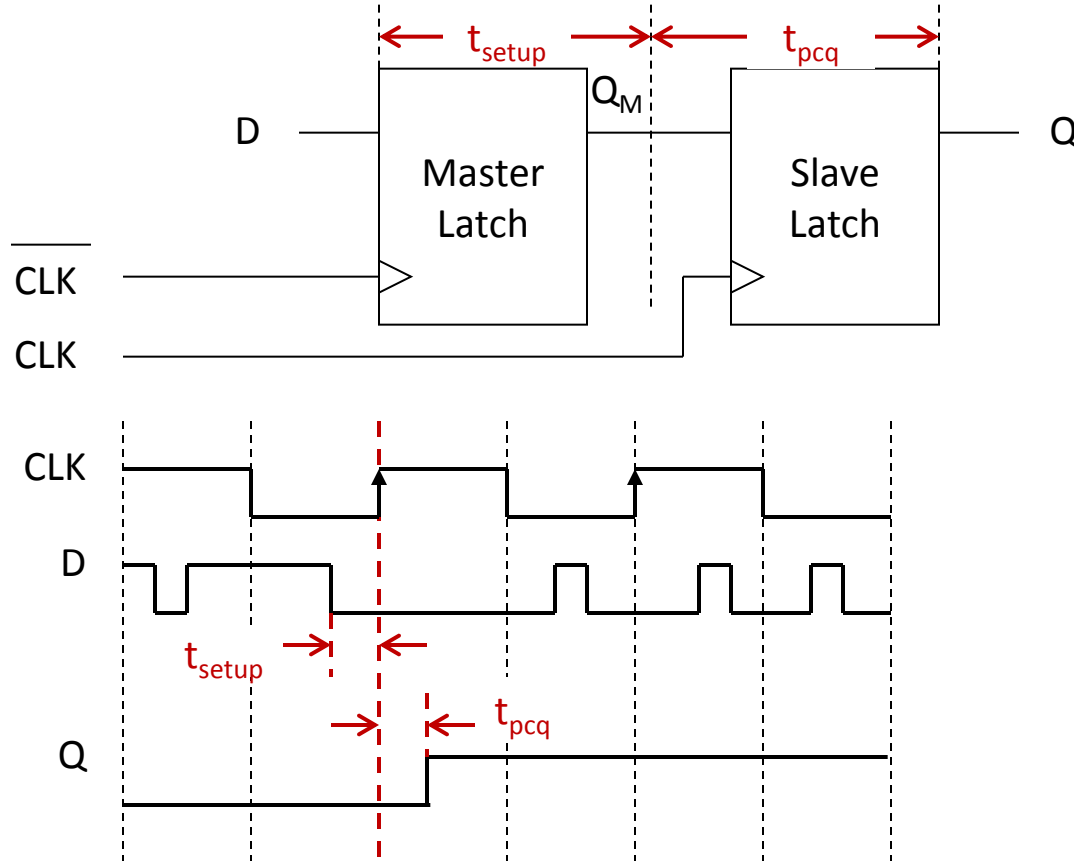
Master-Slave Edge-Triggered Flip-Flop

- Can connect two level-sensitive latches in Master-Slave configuration to form edge-triggered flip-flop
- Master latch *catches* value of D at Q_M when CLK is low
- Slave latch causes Q to change only at rising edge of CLK



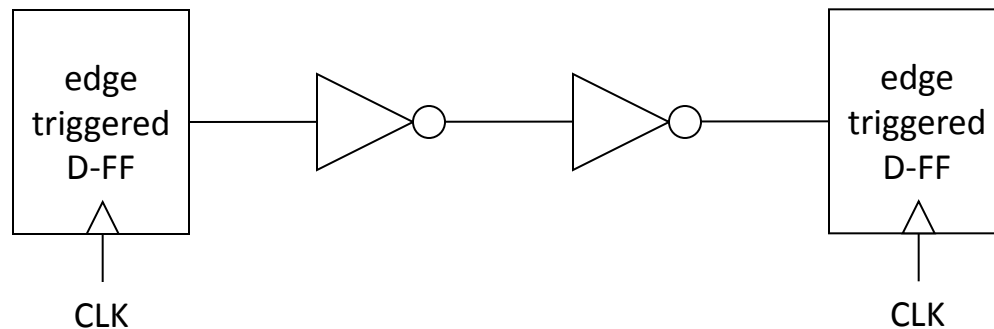
Setup Time & Flip-Flop Propagation Delay

- Setup time: D must be stable some setup time *before* the rising edge of the clock, e.g. $t_{\text{setup}} = 1 \text{ ns}$
- Propagation delay: amount of time *after* the rising edge of the clock before Q completely changes, e.g. $t_{\text{pcq}} = 1 \text{ ns}$



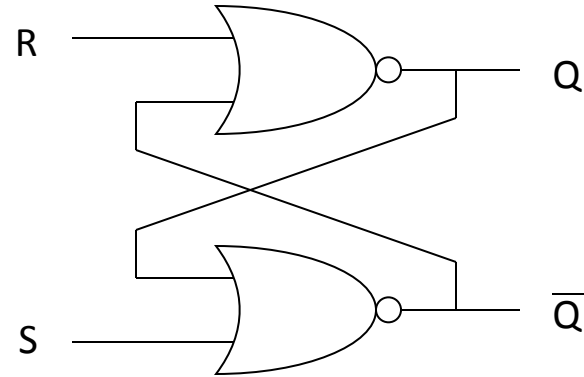
Setup Time & FF Delay

- Suppose $t_{\text{setup}} = 1 \text{ ns}$, $t_{\text{pcq}} = 1 \text{ ns}$, and $t_{\text{inv}} = 1 \text{ ns}$, then clock period is 4 ns (or 250 MHz)



RS-Latch as Cross-Coupled NOR Gates

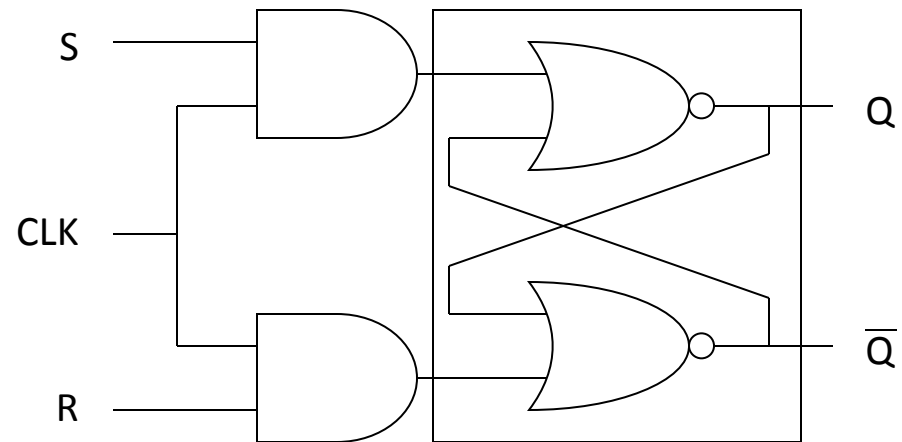
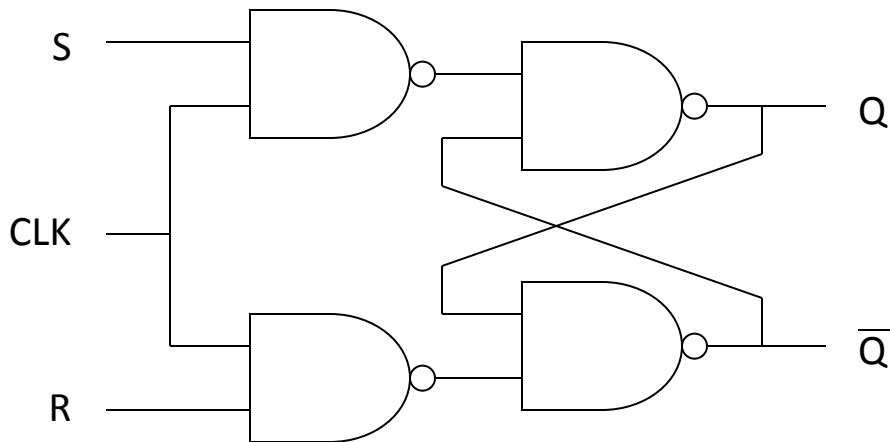
- If $R = 1$, Q resets to 0
- If $S = 1$, Q sets to 1
- If $RS = 00$, no change
- $RS = 11$ is not allowed because leads to oscillation



S R	Q
0 0	No change
0 1	0
1 0	1
1 1	Undefined

Level-Sensitive RS-Latch

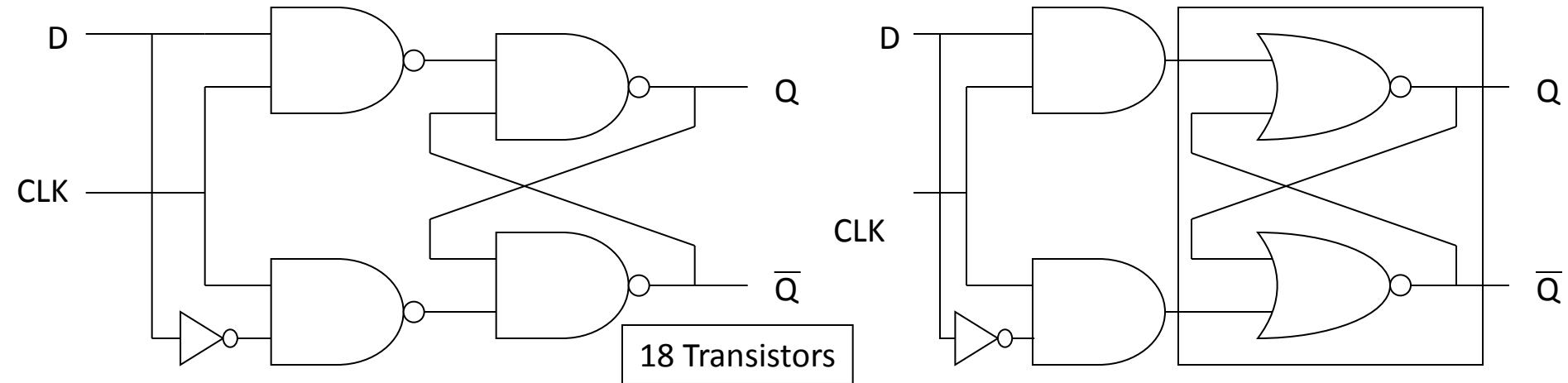
- Q only changes when CLK is high (i.e. level-sensitive)
- When CLK is high, behavior same as RS latch



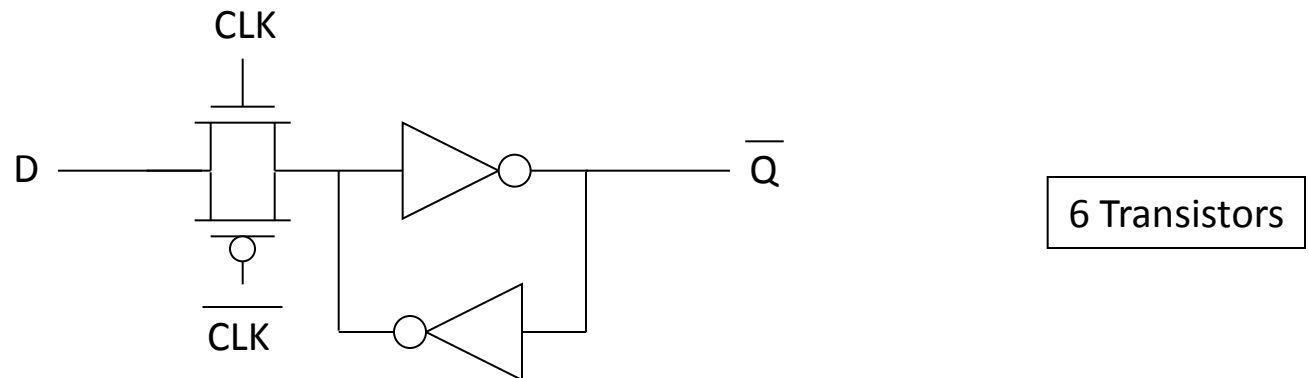
CLK	S R	Q
0	X X	No change
1	0 0	No change
1	0 1	0
1	1 0	1
1	1 1	Undefined

Level-Sensitive D-Latch

- Make level-sensitive D-latch from level-sensitive RS-latch by connecting $S = D$ and $R = \text{not } D$

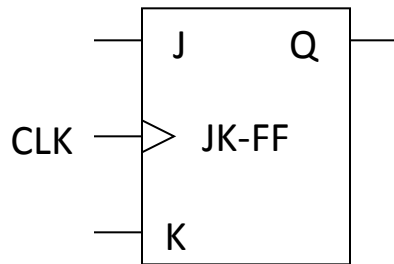
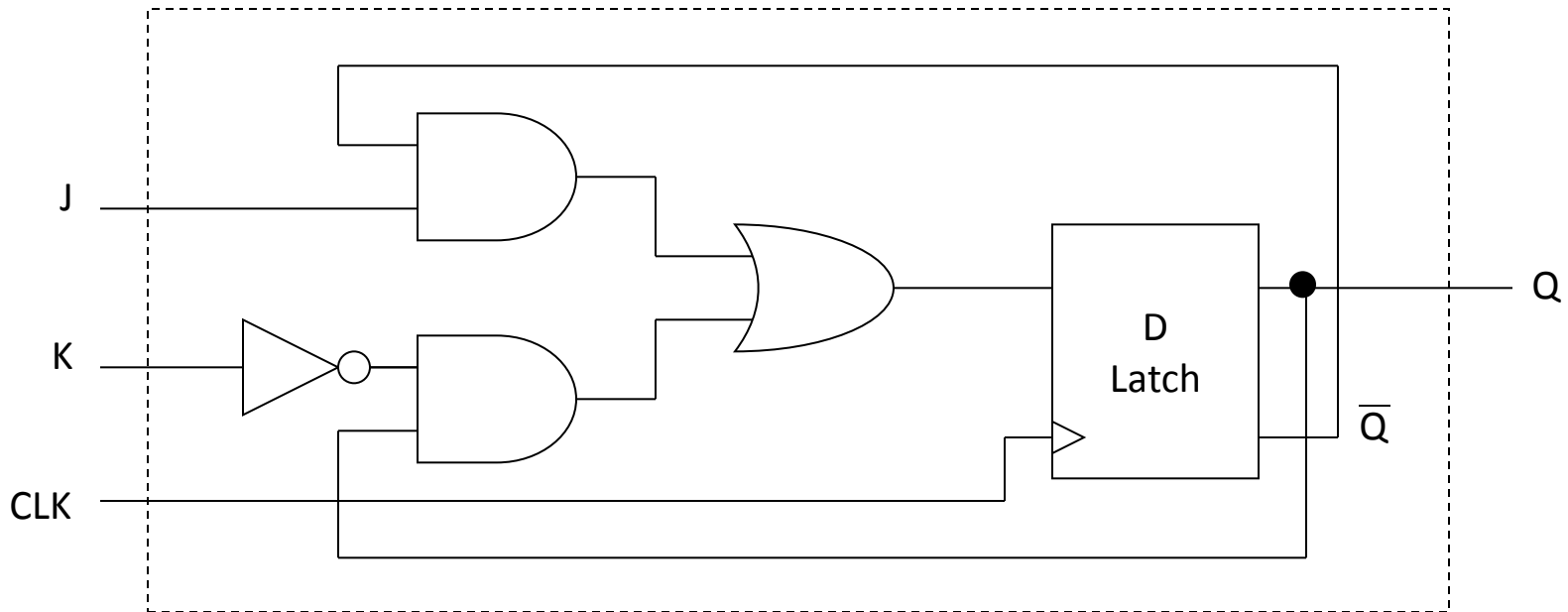


- Compared to transistor version



JK Flip-Flop from D-Latch

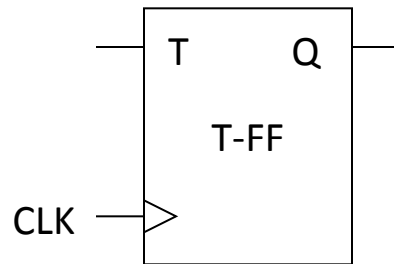
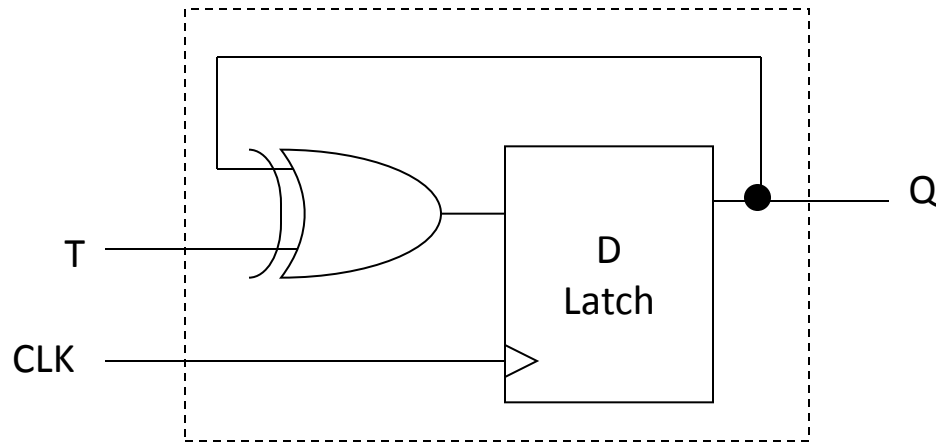
- Same as RS-Latch except it *toggles* on 11



CLK	J K	Q
0	X X	No change
1	0 0	No change
1	0 1	0
1	1 0	1
1	1 1	Toggle

Toggle Flip-Flop from D-Latch

- Toggles stored value if $T = 1$ when CLK is high



CLK	T	Q
0	X	No change
1	0	No change
1	1	Toggle