ModelSim® Reference Manual

Software Version 6.5e
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Chapter 1
Syntax and Conventions

Documentation Conventions

This manual uses the following conventions to define ModelSim™ command syntax.

Table 1-1. Conventions for Command Syntax

<table>
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<th>Syntax notation</th>
<th>Description</th>
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<tr>
<td><code>&lt; &gt;</code></td>
<td>angled brackets surrounding a syntax item indicate a user-defined argument; do not enter the brackets in commands</td>
</tr>
<tr>
<td><code>[ ]</code></td>
<td>square brackets generally indicate an optional item; if the brackets surround several words, all must be entered as a group; the brackets are not entered¹</td>
</tr>
<tr>
<td><code>{ }</code></td>
<td>braces indicate that the enclosed expression contains one or more spaces yet should be treated as a single argument, or that the expression contains square brackets for an index; for either situation, the braces are entered</td>
</tr>
<tr>
<td><code>...</code></td>
<td>an ellipsis indicates items that may appear more than once; the ellipsis itself does not appear in commands</td>
</tr>
<tr>
<td>`</td>
<td>`</td>
</tr>
<tr>
<td>monospaced type</td>
<td>monospaced type is used in command examples</td>
</tr>
<tr>
<td><code>#</code></td>
<td>comments included with commands are preceded by the number sign (#); useful for adding comments to DO files (macros)</td>
</tr>
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</table>

¹. One exception to this rule is when you are using Verilog syntax to designate an array slice. For example,

```
add wave {vector1[4:0]}
```

The square brackets in this case denote an index. The braces prevent the Tcl interpreter from treating the text within the square brackets as a Tcl command.

**Note**

Neither the prompt at the beginning of a line nor the <Enter> key that ends a line is shown in the command examples.
File and Directory Pathnames

Several ModelSim commands have arguments that point to files or directories. For example, the 
-y argument to vlog specifies the Verilog source library directory to search for undefined 
modules. Spaces in file pathnames must be escaped or the entire path must be enclosed in 
quotes. For example:

   vlog top.v -y C:/Documents\ and\ Settings/projects/dut

or

   vlog top.v -y "C:/Documents and Settings/projects/dut"

Design Object Names

Design objects are organized hierarchically. Each of the following objects creates a new level in the hierarchy:

- **VHDL** — component instantiation statement, block statement, and package
- **Verilog** — module instantiation, named fork, named begin, task and function
- **SystemVerilog** — class, package, program, and interface

Object Name Syntax

The syntax for specifying object names in ModelSim is as follows:

```
[<datasetName><datasetSeparator>][<pathSeparator>][<hierarchicalPath>]
<objectName>[[<elementSelection>]]
```

where

- **datasetName** — is the logical name of the WLF file in which the object exists. The currently active simulation is the “sim” dataset. Any loaded WLF file is referred to by the logical name specified when the WLF file was loaded. Refer to the chapter “Recording Simulation Results With Datasets” in the User’s Manual for more information.
- **datasetSeparator** — is the character used to terminate the dataset name. The default is colon ( : ), though a different character (other than backslash ( \ )) may be specified as the dataset separator via the DatasetSeparator variable in the modelsim.ini file. The default is a colon ( : ). This character must be different than the pathSeparator character.
- **pathSeparator** — is the character used to separate hierarchical object names. Normally, a backslash ( / ) is used for VHDL and a period ( . ) is used for Verilog, although other characters (except a backslash ( \ )) may be specified via the PathSeparator variable in the modelsim.ini file. This character must be different than the datasetSeparator. Neither
( . ) nor ( / ) can be used when referring to the contents of a SystemVerilog package or class.

- **hierarchicalPath** — is a set of hierarchical instance names separated by a path separator and ending in a path separator prior to the objectName. For example, /top/proc/clk.

- **objectName** — is the name of an object in a design.

- **elementSelection** — indicates some combination of the following:
  
  - **Array indexing** — Single array elements are specified using either parentheses "()" or square brackets "[]" around a single number.
  
  - **Array slicing** — Slices (or part-selects) of arrays are specified using either parentheses ( () ) or square brackets ( [] ) around a range specification. A range is two numbers separated by one of the following: " to ", " downto ", or a colon ( : ). See *Escaping Brackets and Spaces in Array Slices* for important information about using square brackets in ModelSim commands.

  - **Record field selection** — A record field is specified using a period ( . ) followed by the name of the field.

### SystemVerilog Scope Resolution Operator

SystemVerilog offers the scope resolution operator, double colon ( :: ), for accessing classes within a package and static data within a class. The example below shows various methods of using this operator as well as alternatives using standard hierarchical references.

**Example 1-1. SystemVerilog Scope Resolution Operator Example**

```verilog
package myPackage;
  class packet;
    static int a[0:1] = {1, 2};
    int b[0:1];
    int c;

    function new;
      b[0] = 3;
      b[1] = 4;
      c = a[0];
    endfunction
  endclass
endpackage : myPackage

module top;
  myPackage::packet my = new;
  int myint = my.a[1];
endmodule
```

The following examine examples access data from the class *packet*. 
Syntax and Conventions

File and Directory Pathnames

examine myPackage::packet::a
examine /top/my.a

Both of the above commands return the contents of the static array \textit{a} within class \textit{packet}.

examine myPackage::packet::a(0)
examine /top/my.a(0)

Both of the above commands return the contents of the first element of the static array \textit{a} within class \textit{packet}.

examine /top/my.b

Return the contents of the instance-specific array \textit{b}.

examine /top/my.b(0)

Return the contents of the first element of the instance-specific array \textit{b}.

When referring to the contents of a package or class, you cannot use the standard path separators, a period (.) or a forward slash (/).

Specifying Names

We distinguish between four "types" of object names: simple, relative, fully-rooted, and absolute.

- **Simple name** — does not contain any hierarchy. It is simply the name of an object (e.g., \textit{clk} or \textit{data[3:0]}) in the current context.

- **Relative name** — does not start with a path separator and may or may not include a dataset name or a hierarchical path (e.g., \textit{u1/data} or \textit{view::clk}). A relative name is relative to the current context in the current or specified dataset.

- **Fully-rooted name** — starts with a path separator and includes a hierarchical path to an object (e.g., \textit{/top/u1/clk}). There is a special case of a fully-rooted name where the top-level design unit name can be unspecified (e.g., \textit{/u1/clk}). In this case, the first top-level instance in the design is assumed.

- **Absolute name** — is an exactly specified hierarchical name containing a dataset name and a fully rooted name (e.g., \textit{sim:/top/u1/clk}).

The current dataset is used when accessing objects where a dataset name is not specified as part of the name. The current dataset is determined by the dataset currently selected in the Structure window or by the last dataset specified in an environment.

The current context in the current or specified dataset is used when accessing objects with relative or simple names. The current context is either the current process, if any, or the current instance if there is no current process or the current process is not in the current instance. The situation of the current process not being in the current instance can occur, for example, by
selecting a different instance in the Structure tab or by using the environment to set the current context to a different instance.

Table 1-2 contains examples of various ways of specifying object names.

<table>
<thead>
<tr>
<th>Object Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>specifies the object clk in the current context</td>
</tr>
<tr>
<td>/top/clk</td>
<td>specifies the object clk in the top-level design unit.</td>
</tr>
<tr>
<td>/top/block1/u2/clk</td>
<td>specifies the object clk, two levels down from the top-level design unit</td>
</tr>
<tr>
<td>block1/u2/clk</td>
<td>specifies the object clk, two levels down from the current context</td>
</tr>
<tr>
<td>array_sig[4]</td>
<td>specifies an index of an array object</td>
</tr>
<tr>
<td>{array_sig(1 to 10)}</td>
<td>specifies a slice of an array object in VHDL; see Escaping Brackets and Spaces in Array Slices for more information</td>
</tr>
<tr>
<td>{mysignal[31:0]}</td>
<td>specifies a slice of an array object in Verilog; see Escaping Brackets and Spaces in Array Slices for more information</td>
</tr>
<tr>
<td>record_sig.field</td>
<td>specifies a field of a record</td>
</tr>
</tbody>
</table>

Escaping Brackets and Spaces in Array Slices

Because ModelSim is a Tcl-based tool, you must use curly braces ( {} ) to "escape" square brackets and spaces when specifying array slices. For example:

```
toggle add {data[3:0]}
toggle add {data(3 to 0)}
```

For complete details on Tcl syntax, refer to Tcl Command Syntax.

Further Details

As a Tcl-based tool, ModelSim commands follow Tcl syntax. One problem people encounter with ModelSim commands is the use of square brackets ([ ]) or spaces when specifying array slices. As shown on the previous page, square brackets are used to specify slices of arrays (e.g., data[3:0]). However, in Tcl, square brackets signify command substitution. Consider the following example:

```
set aluinputs [find -in alu/*]
```

ModelSim evaluates the find command first and then sets variable aluinputs to the result of the find command. Obviously you don’t want this type of behavior when specifying an array slice, so you would use curly brace escape characters:
Syntax and Conventions

Wildcard Characters

```text
add wave {/s/abc/data_in[10:1]}
```

You must also use the escape characters if using VHDL syntax with spaces:

```text
add wave {/s/abc/data_in(10 downto 1)}
```

Environment Variables and Pathnames

You can substitute environment variables for pathnames in any argument that requires a pathname. For example:

```text
vlog -v $lib_path/und1
```

Assuming you have defined $lib_path on your system, vlog will locate the source library file `und1` and search it for undefined modules. Refer to Environment Variables for more information.

Name Case Sensitivity

Name case sensitivity is different for VHDL and Verilog. VHDL names are not case sensitive except for extended identifiers in VHDL 1076-1993 or later. In contrast, all Verilog names are case sensitive.

Names in ModelSim commands are case sensitive when matched against case sensitive identifiers, otherwise they are not case sensitive.

Extended Identifiers

The following are supported formats for extended identifiers for any command that takes an identifier.

```text
{\ext ident!\}
```

# Note that trailing space before closing brace is required

```text
\\ext\ ident\!
```

# All non-alpha characters escaped

Wildcard Characters

Wildcard characters can be used in HDL object names in some simulator commands. Table 1-3 shows the conventions for allowable wildcard characters.

<table>
<thead>
<tr>
<th>Character Syntax</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>matches any sequence of characters</td>
</tr>
<tr>
<td>?</td>
<td>matches any single character</td>
</tr>
</tbody>
</table>
A wildcard character does not match a path separator. For example, /dut/* will match /dut/siga and /dut/clk. However, /dut* will not match either of those.

### Using the WildcardFilter Preference Variable

The WildcardFilter preference variable controls which object types are excluded when performing wildcard matches for the following commands:

- add dataflow
- add list
- add memory
- add watch
- add wave
- find
- log

The default behavior is to exclude the following object types:

- VHDL shared variables in packages and design units, constants, generics, and immediate assertions
- Verilog parameters, specparams, memories
- PSL and SystemVerilog assertions, covers, and endpoints
- Signals in cells

Note

Your WildcardFilter settings are persistent from one invocation to the next.
Procedure

Determining the Current WildcardFilter Variable Settings

Enter the following command:

```plaintext
set WildcardFilter
```

which returns a list of currently set arguments for exclusion.

Changing the WildcardFilter Settings from the Command Line

Refer to the list of WildcardFilter arguments in Table 1-4 to determine what you want to exclude from wildcard matches, then enter the following command:

```plaintext
set WildcardFilter "<argument> ..."
```

Note that you must enclose the space-separated list of arguments in quotation marks.

Changing the WildcardFilter Settings back to the Default

Enter the following command:

```plaintext
set WildcardFilter default
```

Changing the WildcardFilter settings from the GUI

1. Choose **Tools > Wildcard Filter** from the main menu.
2. Select the individual Filters you want to exclude from wildcard searches (Table 1-4 describes each option), or select Composite Filters to activate related filters (Table 1-5 describes each composite option).
3. Click OK.

WildcardFilter Argument Descriptions

Table 1-4 provides a list of the WildcardFilter arguments.

**Table 1-4. WildcardFilter Arguments**

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Alias</td>
<td>VHDL Alias</td>
</tr>
<tr>
<td>Architecture</td>
<td>VHDL Architecture</td>
</tr>
<tr>
<td>Assertion</td>
<td>Concurrent SystemVerilog or PSL assertion</td>
</tr>
<tr>
<td>Block</td>
<td>VHDL or Verilog block</td>
</tr>
<tr>
<td>CellInternal</td>
<td>Signals in cells, where a cell is defined as 1) a module within a ‘celldefine 2) a Verilog module found with a library search (using either vlog -v or vlog -y) and compiled with vlog +libcell or 3) a module containing a specify block</td>
</tr>
<tr>
<td>Class</td>
<td>Verilog class</td>
</tr>
</tbody>
</table>
### Table 1-4. WildcardFilter Arguments

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ClassReference</td>
<td>SystemVerilog class reference</td>
</tr>
<tr>
<td>ClockingBlock</td>
<td>Verilog clocking block</td>
</tr>
<tr>
<td>Compare</td>
<td>Waveform comparison signal</td>
</tr>
<tr>
<td>Configuration</td>
<td>Verilog configuration</td>
</tr>
<tr>
<td>Constant</td>
<td>VHDL constant</td>
</tr>
<tr>
<td>Cover</td>
<td>SystemVerilog or PSL cover statements</td>
</tr>
<tr>
<td>Covergroup</td>
<td>SystemVerilog or PSL covergroup</td>
</tr>
<tr>
<td>Coverpoint</td>
<td>Verilog coverpoint</td>
</tr>
<tr>
<td>Cross</td>
<td>Verilog cross</td>
</tr>
<tr>
<td>Endpoint</td>
<td>SystemVerilog assertion objects created for sequences on which the method “ended/triggered” is used. PSL assertion objects created for sequences for which the builtin function “ended()” is used.</td>
</tr>
<tr>
<td>Foreign</td>
<td>VHDL foreign</td>
</tr>
<tr>
<td>Function</td>
<td>Verilog function</td>
</tr>
<tr>
<td>Generate</td>
<td>VHDL generate</td>
</tr>
<tr>
<td>Generic</td>
<td>VHDL generic</td>
</tr>
<tr>
<td>ImmediateAssert</td>
<td>VHDL immediate assertions</td>
</tr>
<tr>
<td>Integer</td>
<td>VHDL integer</td>
</tr>
<tr>
<td>Interface</td>
<td>SystemVerilog interface</td>
</tr>
<tr>
<td>Memory</td>
<td>Verilog memories</td>
</tr>
<tr>
<td>Module</td>
<td>Verilog module</td>
</tr>
<tr>
<td>NamedEvent</td>
<td>Verilog named event</td>
</tr>
<tr>
<td>Net</td>
<td>Verilog net</td>
</tr>
<tr>
<td>Package</td>
<td>VHDL package</td>
</tr>
<tr>
<td>ParamClass</td>
<td>Verilog parameterized class</td>
</tr>
<tr>
<td>Parameter</td>
<td>Verilog parameter</td>
</tr>
<tr>
<td>Port</td>
<td>Verilog port</td>
</tr>
<tr>
<td>Primitive</td>
<td>Verilog primitive</td>
</tr>
<tr>
<td>Process</td>
<td>VHDL process</td>
</tr>
<tr>
<td>Property</td>
<td>Assertion property</td>
</tr>
</tbody>
</table>
### Table 1-4. WildcardFilter Arguments

<table>
<thead>
<tr>
<th>Argument</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Real</td>
<td>Verilog real registers</td>
</tr>
<tr>
<td>Reg</td>
<td>Verilog register</td>
</tr>
<tr>
<td>Root</td>
<td>All objects</td>
</tr>
<tr>
<td>ScExport</td>
<td>SystemC export</td>
</tr>
<tr>
<td>ScHierChannel</td>
<td>SystemC hierarchical channel</td>
</tr>
<tr>
<td>ScMethod</td>
<td>SystemC method</td>
</tr>
<tr>
<td>ScModule</td>
<td>SystemC module</td>
</tr>
<tr>
<td>ScPort</td>
<td>SystemC port</td>
</tr>
<tr>
<td>ScPrimChannel</td>
<td>SystemC primitive channel</td>
</tr>
<tr>
<td>ScThread</td>
<td>SystemC thread</td>
</tr>
<tr>
<td>ScVariable</td>
<td>SystemC variable</td>
</tr>
<tr>
<td>Sequence</td>
<td>SystemVerilog sequence</td>
</tr>
<tr>
<td>Signal</td>
<td>VHDL signal</td>
</tr>
<tr>
<td>SpecParam</td>
<td>Verilog specparam</td>
</tr>
<tr>
<td>Statement</td>
<td>Verilog statement</td>
</tr>
<tr>
<td>Task</td>
<td>Verilog task</td>
</tr>
<tr>
<td>TaThreadMon</td>
<td>Assertion thread monitor object</td>
</tr>
<tr>
<td>Time</td>
<td>Verilog time registers</td>
</tr>
<tr>
<td>TrStream</td>
<td>Transaction stream</td>
</tr>
<tr>
<td>TrStreamArray</td>
<td>Transaction stream array</td>
</tr>
<tr>
<td>Variable</td>
<td>VHDL shared variables in packages and design units.</td>
</tr>
<tr>
<td>VirtualExpr</td>
<td>Virtual expression</td>
</tr>
<tr>
<td>VirtualRegion</td>
<td>Virtual region</td>
</tr>
<tr>
<td>VirtualSignal</td>
<td>Virtual signal</td>
</tr>
<tr>
<td>vlGenerateBlock</td>
<td>Verilog generate block</td>
</tr>
<tr>
<td>vlPackage</td>
<td>Verilog package</td>
</tr>
<tr>
<td>vlProgram</td>
<td>Verilog program</td>
</tr>
<tr>
<td>vITypedef</td>
<td>Verilog typedef</td>
</tr>
</tbody>
</table>
Table 1-5 provides a list of the group aliases of WildcardFilter arguments.

<table>
<thead>
<tr>
<th>Group Argument</th>
<th>Specific arguments included</th>
</tr>
</thead>
<tbody>
<tr>
<td>AllVHDLScopes</td>
<td>Architecture, Block, Generate, Package, Foreign</td>
</tr>
<tr>
<td>AllVHDL</td>
<td>Architecture, Block, Generate, Package, Foreign, Process, Signal, Variable, Constant, Generic, Alias</td>
</tr>
<tr>
<td>AllVerilogScopes</td>
<td>Block, vlGenerateBlock, Module, Task, Function, Statement, Class, Cross, Covergroup, Coverpoint, vlPackage, vlTypedef, ParamClass, ClockingBlock</td>
</tr>
<tr>
<td>AllVerilogVars</td>
<td>Parameter, Reg, Integer, Time, Real, SpecParam, Memory, NamedEvent, ClassReference</td>
</tr>
<tr>
<td>AllVerilog</td>
<td>Block, vlGenerateBlock, Module, Primitive, Task, Function, Statement, Net, Parameter, Reg, Integer, Time, Real, SpecParam, Memory, NamedEvent, Class, Cross, Covergroup, Coverpoint, vlPackage, vlTypedef, ParamClass, ClockingBlock, ClassReference</td>
</tr>
<tr>
<td>VirtualSignals</td>
<td>VirtualSignal, VirtualExpr</td>
</tr>
<tr>
<td>Virtual</td>
<td>VirtualRegion, VirtualSignal, VirtualExpr</td>
</tr>
<tr>
<td>SystemCSignals</td>
<td>ScPrimChannel, ScPort, ScExport</td>
</tr>
<tr>
<td>SystemCProcess</td>
<td>ScModule, ScPrimChannel, ScVariable, ScPort, ScMethod, ScThread</td>
</tr>
<tr>
<td>SystemC</td>
<td>ScModule, ScPrimChannel, ScVariable, ScPort, ScMethod, ScThread, ScExport, ScHierChannel</td>
</tr>
<tr>
<td>TR</td>
<td>TrStream, TrStreamArray</td>
</tr>
<tr>
<td>AllHDLScopes</td>
<td>Architecture, Block, Generate, Package, Foreign, vhGenerateBlock, Module, Task, Function, Statement, Class, Cross, Covergroup, Coverpoint, vlPackage, vlTypedef, ParamClass, ClockingBlock</td>
</tr>
<tr>
<td>AllHDLSignals</td>
<td>Signal, Variable, Constant, Generic, Alias, Net, Parameter, Reg, Integer, Time, Real, SpecParam, Memory, NamedEvent, VirtualSignal, VirtualExpr, ClassReference</td>
</tr>
<tr>
<td>AllVariables</td>
<td>Variable, Constant, Generic, Alias, Parameter, Reg, Integer, Time, Real, SpecParam, Memory, NamedEvent, ClassReference</td>
</tr>
<tr>
<td>AllHDLSignalsVars</td>
<td>Signal, Variable, Constant, Generic, Alias, Net, Parameter, Reg, Integer, Time, Real, SpecParam, Memory, NamedEvent, VirtualSignal, VirtualExpr, ClassReference</td>
</tr>
</tbody>
</table>
ModelSim variables can be referenced in simulator commands by preceding the name of the variable with the dollar sign ($) character. ModelSim uses global variables for simulator state variables, simulator control variables, simulator preference variables, and user-defined variables. Refer to modelsim.ini Variables in the User’s Manual for more information on variables.

The report command returns a list of current settings for either the simulator state or simulator control variables.
Simulation Time Units

You can specify the time unit for delays in all simulator commands that have time arguments. For example:

```
force clk 1 50 ns, 1 100 ns -repeat 1 us
run 2 ms
```

Note that all the time units in a ModelSim command need not be the same.

Unless you specify otherwise as in the examples above, simulation time is always expressed using the resolution units that are specified by the User TimeUnit variable.

By default, the specified time units are assumed to be relative to the current time unless the value is preceded by the character @, which signifies an absolute time specification.

Argument Files

You can load additional arguments into some commands by using argument files, which are specified with the -f argument. The following commands support the -f argument:

```
vlog  vcom  vsim
```

The -f <filename> argument specifies a file that contains additional command line arguments. The following sections outline some syntax rules for argument files.

- **Single Quotes** — allows you to group arbitrary characters so that no character substitution occurs within the quotes, such as environment variable expansion or escaped characters.
  
  ```
  +acc=rn+'\mymodule'
  // does not treat the \ as an escape character
  ```

- **Double Quotes** — allows you to group arbitrary characters so that Tcl-style backslash substitution and environment variable expansion is performed.
  
  ```
  +acc=rn+"\mymodule\$VAR"
  // escapes the path separators (\) and substitutes
  // your value of "$VAR"
  ```

- **Unquoted** — the following are notes on what occurs when some information is not quoted:
  
  - **Tcl backslash substitution** — any unquoted backslash (\) will be treated as an escape character.
    
    ```
    +acc=rn\mymodule
    // the leading \ is considered an escape character
    ```
Command Shortcuts

- Environment variable expansion — any unquoted environment variable, such as $envname, will be expanded. You can also use curly braces in your environment variable, such as ${envname}.

  +acc=rn\$MODULE
  // the leading '\ is considered an escape character and the
  // variable $MODULE is expanded

- Newline Character — you can specify arguments on separate lines in the argument file, with the newline characters treated as space characters. There is no need to put '\ at the end of each line.

- Comments — Comments within the argument files follow these rules:
  - All text in a line beginning with // to its end is treated as a comment.
  - All text bracketed by /* … */ is treated as a comment.

**Command Shortcuts**

- You may abbreviate command syntax, but there’s a catch — the minimum number of characters required to execute a command are those that make it unique. Remember, as we add new commands some of the old shortcuts may not work. For this reason ModelSim does not allow command name abbreviations in macro files. This minimizes your need to update macro files as new commands are added.

- Multiple commands may be entered on one line if they are separated by semi-colons (;). For example:

```
ModelSim> vlog -nodebug=ports level3.v level2.v ; vlog -nodebug top.v
```

The return value of the last function executed is the only one printed to the transcript. This may cause some unexpected behavior in certain circumstances. Consider this example:

```
vsim -c -do "run 20 ; simstats ; quit -f" top
```

You probably expect the simstats results to display in the Transcript window, but they will not, because the last command is quit -f. To see the return values of intermediate commands, you must explicitly print the results. For example:

```
vsim -do "run 20 ; echo [simstats] ; quit -f" -c top
```
Command History Shortcuts

You can review simulator command history or rerun previous commands by using keyboard shortcuts at the ModelSim/VSIM prompt. Table 1-6 contains a list of these shortcuts.

Table 1-6. Keyboard Shortcuts for Command History

<table>
<thead>
<tr>
<th>Shortcut</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>!!</td>
<td>repeats the last command</td>
</tr>
<tr>
<td>!n</td>
<td>repeats command number n; n is the VSIM prompt number (e.g., for this prompt: VSIM 12&gt;, n =12)</td>
</tr>
<tr>
<td>!abc</td>
<td>repeats the most recent command starting with &quot;abc&quot;</td>
</tr>
<tr>
<td>^xyz^ab^</td>
<td>replaces &quot;xyz&quot; in the last command with &quot;ab&quot;</td>
</tr>
<tr>
<td>up and down arrows</td>
<td>scrolls through the command history with the keyboard arrows</td>
</tr>
<tr>
<td>click on prompt</td>
<td>left-click once on a previous ModelSim or VSIM prompt in the transcript to copy the command typed at that prompt to the active cursor</td>
</tr>
<tr>
<td>his or history</td>
<td>shows the last few commands (up to 50 are kept)</td>
</tr>
</tbody>
</table>

Numbering Conventions

Numbers in ModelSim can be expressed in either VHDL or Verilog style. You can use two styles for VHDL numbers and one for Verilog.

VHDL Numbering Conventions

There are two types of VHDL number styles:

VHDL Style 1

[-] [ radix # ] value [ # ]

Table 1-7. VHDL Number Conventions: Style 1

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>indicates a negative number; optional</td>
</tr>
<tr>
<td>radix</td>
<td>can be any base in the range 2 through 16 (2, 8, 10, or 16); by default, numbers are assumed to be decimal; optional</td>
</tr>
<tr>
<td>value</td>
<td>specifies the numeric value, expressed in the specified radix; required</td>
</tr>
<tr>
<td>#</td>
<td>is a delimiter between the radix and the value; the first # sign is required if a radix is used, the second is always optional</td>
</tr>
</tbody>
</table>
A ‘-’ can also be used to designate a "don’t care" element when you search for a signal value or expression in the List or Wave window. If you want the ‘-’ to be read as a "don’t care" element, rather than a negative sign, be sure to enclose the number in double quotes. For instance, you would type "-0110--" as opposed to -0110--. If you don’t include the double quotes, ModelSim will read the ‘-’ as a negative sign. For example:

```
16#FFca23#
2#11111110
-23749
```

**VHDL Style 2**

```plaintext
base "value"
```

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>base</td>
<td>specifies the base; binary: B, octal: O, hex: X; required</td>
</tr>
<tr>
<td>&quot;value&quot;</td>
<td>specifies digits in the appropriate base with optional underscore separators; default is decimal; required</td>
</tr>
</tbody>
</table>

For example:

```plaintext
B"11111110"
X"FFca23"
```

**Searching for VHDL Arrays in the Wave and List Windows**

Searching for signal values in the Wave or List window may not work correctly for VHDL arrays if the target value is in decimal notation. You may get an error that the value is of incompatible type. Since VHDL does not have a radix indicator for decimal, the target value may get misinterpreted as a scalar value. Prefixing the value with the Verilog notation ‘d should eliminate the problem, even if the signal is VHDL.

**Verilog Numbering Conventions**

Verilog numbers are expressed in the style:

```
[ - ] [ size ] [ base ] value
```

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>indicates a negative number; optional</td>
</tr>
<tr>
<td>size</td>
<td>the number of bits in the number; optional</td>
</tr>
<tr>
<td>base</td>
<td>specifies the base; binary: ‘b or ‘B, octal: ‘o or ‘O, decimal: ‘d or ‘D, hex: ‘h or ‘H; optional</td>
</tr>
</tbody>
</table>
A ‘-’ can also be used to designate a "don’t care" element when you search for a signal value or expression in the List or Wave windows. If you want the ‘-’ to be read as a "don’t care" element, rather than a negative sign, be sure to enclose the number in double quotes. For instance, you would type "-0110--" as opposed to 7'b-0110--. If you don’t include the double quotes, ModelSim will read the ‘-’ as a negative sign. For example:

'b1111110  8'b11111110
'Hffca23  21'H1fca23
-23749

**GUI_expression_format**

The GUI_expression_format is an option of several simulator commands that operate within the ModelSim GUI environment. The expressions help you locate and examine objects within the List and Wave windows (expressions may also be used through the Edit > Search menu in both windows). The commands that use the expression format are:

configure, examine, searchlog, virtual function, virtual signal.

**Expression Typing**

GUI expressions are typed. The supported types consist of the following scalar and array types.

**Scalar Types**

The scalar types are as follows: boolean, integer, real, time (64-bit integer), enumeration, and signal state. Signal states are represented by the nine VHDL std_logic states: 'U' 'X' '0' '1' 'Z' 'W' 'L' 'H' and '-'.

Verilog states 0, 1, x, and z are mapped into these states and the Verilog strengths are ignored. Conversion is done automatically when referencing Verilog nets or registers.

**Array Types**

The supported array types are signed and unsigned arrays of signal states. This would correspond to the VHDL std_logic_array type. Verilog registers are automatically converted to these array types. The array type can be treated as either UNSIGNED or SIGNED, as in the IEEE std_logic_arith package. Normally, referencing a signal array causes it to be treated as UNSIGNED by the expression evaluator; to cause it to be treated as SIGNED, use casting as described below. Numeric operations supported on arrays are performed by the expression

---

### Table 1-9. Verilog Number Conventions

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>value</td>
<td>specifies digits in the appropriate base with optional underscore separators; default is decimal; required</td>
</tr>
</tbody>
</table>
evaluator via ModelSim’s built-in numeric_standard (and similar) package routines. The expression evaluator selects the appropriate numeric routine based on SIGNED or UNSIGNED properties of the array arguments and the result.

The enumeration types supported are any VHDL enumerated type. Enumeration literals may be used in the expression as long as some variable of that enumeration type is referenced in the expression. This is useful for sub-expressions of the form:

```
(/memory/state == reading)
```

**Expression Syntax**

GUI expressions generally follow C-language syntax, with both VHDL-specific and Verilog-specific conventions supported. These expressions are not parsed by the Tcl parser, and so do not support general Tcl; parentheses should be used rather than braces. Procedure calls are not supported.

A GUI expression can include the following elements: Tcl macros, constants, array constants, variables, array variables, signal attributes, operators, and casting.

**Tcl Macros**

Macros are useful for pre-defined constants or for entire expressions that have been previously saved. The substitution is done only once, when the expression is first parsed. Macro syntax is:

```
$<name>
```

Substitutes the string value of the Tcl global variable <name>. 
Constants

Table 1-10. Constants Supported for GUI Expressions

<table>
<thead>
<tr>
<th>Type</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>boolean value</td>
<td>true, false, TRUE, FALSE</td>
</tr>
<tr>
<td>integer</td>
<td>[0-9]+</td>
</tr>
<tr>
<td>real number</td>
<td>&lt;int&gt;[/&lt;int&gt;[&lt;exp&gt;]] where the optional [exp] is: (e</td>
</tr>
<tr>
<td>time</td>
<td>integer or real optionally followed by time unit</td>
</tr>
<tr>
<td>enumeration</td>
<td>VHDL user-defined enumeration literal</td>
</tr>
<tr>
<td>single bit constants</td>
<td>expressed as any of the following:</td>
</tr>
<tr>
<td></td>
<td>0 1 x X z U H L W 'U' 'X' '0' '1' 'Z' 'W' 'L' 'H' '-' 1'b0 1'b1</td>
</tr>
</tbody>
</table>

Array Constants, Expressed in Any of the Following Formats

Table 1-11. Array Constants Supported for GUI Expressions

<table>
<thead>
<tr>
<th>Type</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>VHDL # notation</td>
<td>&lt;int&gt;#&lt;alphanum&gt;[#]</td>
</tr>
<tr>
<td></td>
<td>Example: 16#abc123#</td>
</tr>
<tr>
<td>VHDL bitstring</td>
<td>&quot;(U</td>
</tr>
<tr>
<td></td>
<td>Example: &quot;11010X11&quot;</td>
</tr>
<tr>
<td>Verilog notation</td>
<td>[-][&lt;int&gt;]'(b</td>
</tr>
<tr>
<td></td>
<td>(where &lt;alphanum&gt; includes 0-9, a-f, A-F, and '-')</td>
</tr>
<tr>
<td></td>
<td>Example: 12'hc91 (This is the preferred notation because it removes the ambiguity about the number of bits.)</td>
</tr>
<tr>
<td>Based notation</td>
<td>0x..., 0X..., 0o..., 0O..., 0b..., 0B...</td>
</tr>
<tr>
<td></td>
<td>ModelSim automatically zero fills unspecified upper bits.</td>
</tr>
</tbody>
</table>

Variables

Table 1-12. Variables Supported for GUI Expressions

<table>
<thead>
<tr>
<th>Variable</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name of a signal</td>
<td>The name may be a simple name, a VHDL or Verilog style extended identifier, or a VHDL or Verilog style path. The signal must be one of the following types: -- VHDL signal of type INTEGER, REAL, or TIME -- VHDL signal of type std_logic or bit -- VHDL signal of type user-defined enumeration -- Verilog net, Verilog register, Verilog integer, or Verilog real</td>
</tr>
</tbody>
</table>
Syntax and Conventions

GUI_expression_format

Array variables

Table 1-13. Array Variables Supported for GUI Expresssions

<table>
<thead>
<tr>
<th>Variable</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name of a signal</td>
<td>-- VHDL signals of type bit_vector or std_logic_vector</td>
</tr>
<tr>
<td></td>
<td>-- Verilog register</td>
</tr>
<tr>
<td></td>
<td>-- Verilog net array</td>
</tr>
<tr>
<td></td>
<td>A subrange or index may be specified in either VHDL or Verilog</td>
</tr>
<tr>
<td></td>
<td>syntax. Examples: mysignal(1 to 5), mysignal[1:5], mysignal (4),</td>
</tr>
<tr>
<td></td>
<td>mysignal [4]</td>
</tr>
</tbody>
</table>

Signal attributes

<name>’event
<name>’rising
<name>’falling
<name>’delayed()
<name>’hasX

The ’delayed attribute lets you assign a delay to a VHDL signal. To assign a delay to a signal in Verilog, use “#” notation in a sub-expression (e.g., #-10 /top/signalA).

The hasX attribute lets you search for signals, nets, or registers that contains an X (unknown) value.

See Examples of Expression Syntax below for further details on ’delayed and ’hasX.
## Operators

### Table 1-14. Operators Supported for GUI Expressions

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&amp;&amp;</td>
<td>boolean and</td>
<td>sll/SLL</td>
<td>shift left logical</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>boolean or</td>
</tr>
<tr>
<td>!</td>
<td>boolean not</td>
<td>srl/SRL</td>
<td>shift right logical</td>
</tr>
<tr>
<td>==</td>
<td>equal</td>
<td>sra/SRA</td>
<td>shift right arithmetic</td>
</tr>
<tr>
<td>!=</td>
<td>not equal</td>
<td>ror/ROR</td>
<td>rotate right</td>
</tr>
<tr>
<td>===</td>
<td>exact equal¹</td>
<td>rol/ROL</td>
<td>rotate left</td>
</tr>
<tr>
<td>!==</td>
<td>exact not equal¹</td>
<td>+</td>
<td>arithmetic add</td>
</tr>
<tr>
<td>&lt;</td>
<td>less than</td>
<td>-</td>
<td>arithmetic subtract</td>
</tr>
<tr>
<td>&lt;=</td>
<td>less than or equal</td>
<td>*</td>
<td>arithmetic multiply</td>
</tr>
<tr>
<td>&gt;</td>
<td>greater than</td>
<td>/</td>
<td>arithmetic divide</td>
</tr>
<tr>
<td>&gt;=</td>
<td>greater than or equal</td>
<td>mod/MOD</td>
<td>arithmetic modulus</td>
</tr>
<tr>
<td>not/NOT/~</td>
<td>unary bitwise inversion</td>
<td>rem/REM</td>
<td>arithmetic remainder</td>
</tr>
<tr>
<td>and/AND</td>
<td>bitwise and</td>
<td>^&lt;vector_expr&gt;</td>
<td>OR reduction</td>
</tr>
<tr>
<td>nand/NAND</td>
<td>bitwise nand</td>
<td>^&lt;vector_expr&gt;</td>
<td>XOR reduction</td>
</tr>
<tr>
<td>or/OR/</td>
<td>bitwise or</td>
<td></td>
<td></td>
</tr>
<tr>
<td>nor/NOR</td>
<td>bitwise nor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>xor/XOR</td>
<td>bitwise xor</td>
<td></td>
<td></td>
</tr>
<tr>
<td>xnor/XNOR</td>
<td>bitwise xnor</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. This operator is allowed to be compatible with other simulators.

### Note

Arithmetic operators use the std_logic_arith package.
Casting

Table 1-15. Casting Conversions Supported for GUI Expressions

<table>
<thead>
<tr>
<th>Casting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(bool)</td>
<td>convert to boolean</td>
</tr>
<tr>
<td>(boolean)</td>
<td>convert to boolean</td>
</tr>
<tr>
<td>(int)</td>
<td>convert to integer</td>
</tr>
<tr>
<td>(integer)</td>
<td>convert to integer</td>
</tr>
<tr>
<td>(real)</td>
<td>convert to real</td>
</tr>
<tr>
<td>(time)</td>
<td>convert to 64-bit integer</td>
</tr>
<tr>
<td>(std_logic)</td>
<td>convert to 9-state signal value</td>
</tr>
<tr>
<td>(signed)</td>
<td>convert to signed vector</td>
</tr>
<tr>
<td>(unsigned)</td>
<td>convert to unsigned vector</td>
</tr>
<tr>
<td>(std_logic_vector)</td>
<td>convert to unsigned vector</td>
</tr>
</tbody>
</table>

Examples of Expression Syntax

/top/bus & $bit_mask

This expression takes the bitwise AND function of signal /top/bus and the array constant contained in the global Tcl variable bit_mask.

clk'event && (/top/xyz == 16'hffae)

This expression evaluates to a boolean true when signal clk changes and signal /top/xyz is equal to hex ffae; otherwise is false.

clk'rising && (mystate == reading) && (/top/u3/addr == 32'habcd1234)

Evaluates to a boolean true when signal clk just changed from low to high and signal mystate is the enumeration reading and signal /top/u3/addr is equal to the specified 32-bit hex constant; otherwise is false.

(/top/u3/addr and 32'hff000000) == 32'hac000000

Evaluates to a boolean true when the upper 8 bits of the 32-bit signal /top/u3/addr equals hex ac.

/top/signalA'delayed(10ns)

This expression returns /top/signalA delayed by 10 ns.

/top/signalA'delayed(10 ns) && /top/signalB

This expression takes the logical AND of a delayed /top/signalA with /top/signalB.
virtual function { (#-10 /top/signalA) && /top/signalB}
mySignalB_AND_DelayedSignalA

This evaluates /top/signalA at 10 simulation time steps before the current time, and takes the logical AND of the result with the current value of /top/signalB. The '#' notation uses positive numbers for looking into the future, and negative numbers for delay. This notation does not support the use of time units.

((NOW > 23 us) && (NOW < 54 us)) && clk’rising && (mode == writing)

Evaluates to a boolean true when WLF file time is between 23 and 54 microseconds, clk just changed from low to high, and signal mode is enumeration writing.

searchlog -expr {dbus'hasX} {0 ns} dbus

Searches for an 'X' in dbus. This is equivalent to the expression: {dbus(0) == 'x' || dbus(1) == 'x'}. This makes it possible to search for X values without having to write a type specific literal.

Signal and Subelement Naming Conventions

ModelSim supports naming conventions for VHDL and Verilog signal pathnames, VHDL array indexing, Verilog bit selection, VHDL subrange specification, and Verilog part selection.

Examples in Verilog and VHDL syntax:

top.chip.vlogsig
/top/chip/vhdlsig
vlogsig[3]
vhdlsig(9)
vlogsig[5:2]
vhdlsig[5 downto 2]

Grouping and Precedence

Operator precedence generally follows that of the C language, but we recommend liberal use of parentheses.

Concatenation of Signals or Subelements

Elements in the concatenation that are arrays are expanded so that each element in the array becomes a top-level element of the concatenation. But for elements in the concatenation that are records, the entire record becomes one top-level element in the result. To specify that the records be broken down so that their subelements become top-level elements in the concatenation, use the `concat_flatten` directive. Currently we do not support leaving full arrays as elements in the result. (Please let us know if you need that option.)
If the elements being concatenated are of incompatible base types, a VHDL-style record will be created. The record object can be expanded in the Objects and Wave windows just like an array of compatible type elements.

**Concatenation Syntax for VHDL**

```
<signalOrSliceName1> & <signalOrSliceName2> & ...
```

**Concatenation Syntax for Verilog**

```
&{<signalOrSliceName1>, <signalOrSliceName2>, ... }
&{<count>{<signalOrSliceName1>}, <signalOrSliceName2>, ... }
```

Note that the concatenation syntax begins with "&{" rather than just "{". Repetition multipliers are supported, as illustrated in the second line. The repetition element itself may be an arbitrary concatenation subexpression.

**Concatenation Directives**

A concatenation directive (as illustrated below) can be used to constrain the resulting array range of a concatenation or influence how compound objects are treated. By default, the concatenation will be created with a descending index range from \((n-1)\) downto 0, where \(n\) is the number of elements in the array.

```
(concat_range 31:0)<concatenationExpr> # Verilog syntax
(concat_range (31:0))<concatenationExpr> # Also Verilog syntax
(concat_range (31 downto 0))<concatenationExpr> # VHDL syntax
```

The **concat_range** directive completely specifies the index range.

```
(concat_ascending) <concatenationExpr>
```

The **concat_ascending** directive specifies that the index start at zero and increment upwards.

```
(concat_flatten) <concatenationExpr>
```

The **concat_flatten** directive flattens the signal structure hierarchy.

```
(concat_noflatten) <concatenationExpr>
```

The concat_noflatten directive groups signals together without merging them into one big array. The signals become elements of a record and retain their original names. When expanded, the new signal looks just like a group of signals. The directive can be used hierarchically with no limits on depth.

```
(concat_sort_wild_ascending) <concatenationExpr>
```

The **concat_sort_wild_ascending** directive gathers signals by name in ascending order (the default is descending).
Syntax and Conventions

**GUI_expression_format**

ModelSim Reference Manual, v6.5e

### Examples of Concatenation

\( \&\{ \text{"mybusbasename*"} \} \)

Gathers all signals in the current context whose names begin with "mybusbasename", sorts those names in descending order, and creates a bus with index range \((n-1)\) downto 0, where \(n\) is the number of matching signals found. (Note that it currently does not derive the index name from the tail of the one-bit signal name.)

\((\text{concat}_\text{range} \ 13:4)\&\{ \text{"mybusbasename*"} \}\)

Specifies the index range to be 13 downto 4, with the signals gathered by name in descending order.

\((\text{concat}_\text{ascending})\&\{ \text{"mybusbasename*"} \}\)

Specifies an ascending range of 0 to \(n\)-1, with the signals gathered by name in descending order.

\((\text{concat}_\text{ascending})\ (\text{concat}_\text{sort_wild_ascending})\&\{\text{"mybusbasename*"}\})\)

Specifies an ascending range of 0 to \(n\)-1, with the signals gathered by name in ascending order.

\((\text{concat}_\text{reverse})(\text{bus1} \ & \ \text{bus2})\)

Specifies that the bits of bus1 and bus2 be reversed in the output virtual signal.

### Record Field Members

Arbitrarily-nested arrays and records are supported, but operators will only operate on one field at a time. That is, the expression \(\{a == b\}\) where \(a\) and \(b\) are records with multiple fields, is not supported. This would have to be expressed as:

\(\{(a.f1 == b.f1) \ && \ (a.f2 == b.f2) \ \ldots\}\)

Examples:

vhdlSig.field1
vhdlSig.field1.subfield1
vhdlSig.(5).field3
vhdlSig.field4(3 downto 0)

### Searching for Binary Signal Values in the GUI

When you use the GUI to search for signal values displayed in 4-state binary radix, you should be aware of how ModelSim maps between binary radix and std_logic. The issue arises because
there is no “un-initialized” value in binary, while there is in std_logic. So, ModelSim relies on mapping tables to determine whether a match occurs between the displayed binary signal value and the underlying std_logic value.

This matching algorithm applies only to searching using the GUI. It does not apply to VHDL or Verilog test benches.

For comparing VHDL std_logic/std_ulogic objects, ModelSim uses the table shown below. An entry of “0” in the table is “no match”; an entry of “1” is a “match”; an entry of “2” is a match only if you set the Tcl variable `STDLOGIC_X_MatchesAnything` to 1. Note that $X$ will match a $U$, and - will match anything.

<table>
<thead>
<tr>
<th>Search Entry</th>
<th>Matches as follows:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>U</td>
</tr>
<tr>
<td>U</td>
<td>1</td>
</tr>
<tr>
<td>X</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Z</td>
<td>0</td>
</tr>
<tr>
<td>W</td>
<td>0</td>
</tr>
<tr>
<td>L</td>
<td>0</td>
</tr>
<tr>
<td>H</td>
<td>0</td>
</tr>
<tr>
<td>-</td>
<td>1</td>
</tr>
</tbody>
</table>

For comparing Verilog net values, ModelSim uses the table shown below. An entry of “2” is a match only if you set the Tcl variable “VLOG_X_MatchesAnything” to 1.

<table>
<thead>
<tr>
<th>Search Entry</th>
<th>Matches as follows:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Z</td>
<td>0</td>
</tr>
<tr>
<td>X</td>
<td>2</td>
</tr>
</tbody>
</table>
This chapter describes ModelSim commands that you can enter either on the command line of the Main window or in a macro file. Some commands are automatically entered on the command line when you use the graphical user interface.

Note that, in addition to the simulation commands listed in this chapter, you can also use the Tcl commands described in the Tcl man pages (use the Main window menu selection: Help > Tcl Man Pages).

Table 2-1 provides a brief description of each ModelSim command. For more information on command details, arguments, and examples, click the link in the Command name column.

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>abort</td>
<td>halts the execution of a macro file interrupted by a breakpoint or error</td>
</tr>
<tr>
<td>add dataflow</td>
<td>adds the specified object to the Dataflow window</td>
</tr>
<tr>
<td>add list</td>
<td>lists VHDL signals and variables, and Verilog nets and registers, and their values in the List window</td>
</tr>
<tr>
<td>add log</td>
<td>also known as the log command; see log</td>
</tr>
<tr>
<td>add memory</td>
<td>opens the specified memory in the MDI frame of the Main window</td>
</tr>
<tr>
<td>add watch</td>
<td>adds signals or variables to the Watch window</td>
</tr>
<tr>
<td>add wave</td>
<td>adds VHDL signals and variables, and Verilog nets and registers to the Wave window</td>
</tr>
<tr>
<td>add_cmdhelp</td>
<td>adds an entry to the command-line help; use the help command to display the help text</td>
</tr>
<tr>
<td>alias</td>
<td>creates a new Tcl procedure that evaluates the specified commands</td>
</tr>
<tr>
<td>batch_mode</td>
<td>returns a 1 if ModelSim is operating in batch mode, otherwise returns a 0</td>
</tr>
<tr>
<td>bd</td>
<td>deletes a breakpoint</td>
</tr>
<tr>
<td>bookmark add wave</td>
<td>adds a bookmark to the specified Wave window</td>
</tr>
<tr>
<td>bookmark delete wave</td>
<td>deletes bookmarks from the specified Wave window</td>
</tr>
<tr>
<td>bookmark goto wave</td>
<td>zooms and scrolls a Wave window using the specified bookmark</td>
</tr>
</tbody>
</table>
### Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>bookmark list wave</td>
<td>displays a list of available bookmarks</td>
</tr>
<tr>
<td>bp</td>
<td>sets a breakpoint</td>
</tr>
<tr>
<td>change</td>
<td>modifies the value of a VHDL variable or Verilog register variable</td>
</tr>
<tr>
<td>configure</td>
<td>invokes the List or Wave widget configure command for the current default List or Wave window</td>
</tr>
<tr>
<td>dataset alias</td>
<td>assigns an additional name to a dataset</td>
</tr>
<tr>
<td>dataset clear</td>
<td>clears the current simulation WLF file</td>
</tr>
<tr>
<td>dataset close</td>
<td>closes a dataset</td>
</tr>
<tr>
<td>dataset config</td>
<td>configures WLF file settings after dataset is open</td>
</tr>
<tr>
<td>dataset info</td>
<td>reports information about the specified dataset</td>
</tr>
<tr>
<td>dataset list</td>
<td>lists the open dataset(s)</td>
</tr>
<tr>
<td>dataset open</td>
<td>opens a dataset and references it by a logical name</td>
</tr>
<tr>
<td>dataset rename</td>
<td>changes the logical name of an opened dataset</td>
</tr>
<tr>
<td>dataset restart</td>
<td>unloads specified or current dataset</td>
</tr>
<tr>
<td>dataset save</td>
<td>saves data from the current WLF file to a specified file</td>
</tr>
<tr>
<td>dataset snapshot</td>
<td>saves data from the current WLF file at a specified interval</td>
</tr>
<tr>
<td>delete</td>
<td>removes objects from either the List or Wave window</td>
</tr>
<tr>
<td>describe</td>
<td>displays information about the specified HDL object</td>
</tr>
<tr>
<td>disablebp</td>
<td>turns off breakpoints and when commands</td>
</tr>
<tr>
<td>do</td>
<td>executes commands contained in a macro file</td>
</tr>
<tr>
<td>drivers</td>
<td>displays in the Main window the current value and scheduled future values for all the drivers of a specified VHDL signal or Verilog net</td>
</tr>
<tr>
<td>dumplog64</td>
<td>dumps the contents of the <code>vsim.wlf</code> file in a readable format</td>
</tr>
<tr>
<td>echo</td>
<td>displays a specified message in the Main window</td>
</tr>
<tr>
<td>edit</td>
<td>invokes the editor specified by the EDITOR environment variable</td>
</tr>
<tr>
<td>enablebp</td>
<td>turns on breakpoints and when commands turned off by the disablebp command</td>
</tr>
<tr>
<td>environment</td>
<td>displays or changes the current dataset and region environment</td>
</tr>
<tr>
<td>examine</td>
<td>examines one or more objects, and displays current values (or the values at a specified previous time) in the Main window</td>
</tr>
</tbody>
</table>
### Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>exit</td>
<td>exits the simulator and the ModelSim application</td>
</tr>
<tr>
<td>find</td>
<td>displays the full pathnames of all objects in the design whose names match the name specification you provide</td>
</tr>
<tr>
<td>find infiles</td>
<td>searches the specified files and prints to the Transcript window those lines from the files that match the specified pattern.</td>
</tr>
<tr>
<td>find insource</td>
<td>searches all source files related to the current design and prints to the Transcript window those lines from the files that match the specified pattern.</td>
</tr>
<tr>
<td>formatTime</td>
<td>global format control for all time values displayed in the GUI</td>
</tr>
<tr>
<td>force</td>
<td>applies stimulus to VHDL signals and Verilog nets</td>
</tr>
<tr>
<td>help</td>
<td>displays in the Main window a brief description and syntax for the specified command</td>
</tr>
<tr>
<td>history</td>
<td>lists the commands executed during the current session</td>
</tr>
<tr>
<td>layout</td>
<td>allows you to perform operations on GUI layouts</td>
</tr>
<tr>
<td>log</td>
<td>creates a wave log format (WLF) file containing simulation data for all objects whose names match the provided specifications</td>
</tr>
<tr>
<td>lshift</td>
<td>takes a Tcl list as an argument and shifts it in-place one place to the left, eliminating the left-most element</td>
</tr>
<tr>
<td>lsublist</td>
<td>returns a sublist of the specified Tcl list that matches the specified Tcl glob pattern</td>
</tr>
<tr>
<td>mem compare</td>
<td>compares the selected memory to a reference memory or file</td>
</tr>
<tr>
<td>mem display</td>
<td>displays the memory contents of a selected instance to the screen</td>
</tr>
<tr>
<td>mem list</td>
<td>displays a flattened list of all memory instances in the current or specified context after a design has been elaborated</td>
</tr>
<tr>
<td>mem load</td>
<td>updates the simulation memory contents of a specified instance</td>
</tr>
<tr>
<td>mem save</td>
<td>saves the contents of a memory instance to a file in any of the supported formats: Verilog binary, Verilog hex, and MTI memory pattern data</td>
</tr>
<tr>
<td>mem search</td>
<td>finds and prints to the screen the first occurring match of a specified memory pattern in the specified memory instance</td>
</tr>
<tr>
<td>messages clearfilter</td>
<td>removes any filter you have set in the Message Viewer</td>
</tr>
<tr>
<td>messages setfilter</td>
<td>performs the same action as the Message Viewer Filter Dialog Box, lets you determine which messages are shown in the Message Viewer</td>
</tr>
</tbody>
</table>
Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>modelsim</td>
<td>starts the ModelSim GUI without prompting you to load a design; valid only for Windows platforms</td>
</tr>
<tr>
<td>noforce</td>
<td>removes the effect of any active force commands on the selected object</td>
</tr>
<tr>
<td>nolog</td>
<td>suspends writing of data to the WLF file for the specified signals</td>
</tr>
<tr>
<td>notepad</td>
<td>opens a simple text editor</td>
</tr>
<tr>
<td>noview</td>
<td>closes a window or set of windows in the ModelSim GUI</td>
</tr>
<tr>
<td>nowhen</td>
<td>deactivates selected when commands</td>
</tr>
<tr>
<td>onbreak</td>
<td>specifies command(s) to be executed when running a macro that encounters a breakpoint in the source code; in effect only during a run command</td>
</tr>
<tr>
<td>onElabError</td>
<td>specifies one or more commands to be executed when an error is encountered during elaboration; in effect only during a vsim command</td>
</tr>
<tr>
<td>onerror</td>
<td>specifies one or more commands to be executed when a Tcl command in a dofile encounters an error; not dependent on a run command</td>
</tr>
<tr>
<td>onfinish</td>
<td>controls simulator behavior when encountering $finish or sc_stop() in the design code</td>
</tr>
<tr>
<td>pause</td>
<td>interrupts the execution of a macro</td>
</tr>
<tr>
<td>precision</td>
<td>determines how real numbers display in the GUI</td>
</tr>
<tr>
<td>printenv</td>
<td>echoes to the Main window the current names and values of all environment variables</td>
</tr>
<tr>
<td>process report</td>
<td>creates textual report of all processes displayed in the Process window</td>
</tr>
<tr>
<td>project</td>
<td>performs common operations on new projects</td>
</tr>
<tr>
<td>pwd</td>
<td>displays the current directory path in the Main window</td>
</tr>
<tr>
<td>quietly</td>
<td>turns off transcript echoing for the specified command</td>
</tr>
<tr>
<td>quit</td>
<td>exits the simulator</td>
</tr>
<tr>
<td>radix</td>
<td>specifies the default radix to be used</td>
</tr>
<tr>
<td>radix define</td>
<td>creates or modifies a user-defined radix</td>
</tr>
<tr>
<td>radix names</td>
<td>returns a list of currently defined radix names</td>
</tr>
<tr>
<td>radix list</td>
<td>returns the complete definition of a radix</td>
</tr>
</tbody>
</table>
### Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>radix delete</td>
<td>removes the radix definition from the named radix</td>
</tr>
<tr>
<td>report</td>
<td>displays the value of all simulator control variables, or the value of any simulator state variables relevant to the current simulation</td>
</tr>
<tr>
<td>restart</td>
<td>reloads the current dataset if the current dataset is not the active simulation (&quot;sim&quot;) and resets the simulation time to zero, in effect acting just like a restart of a simulation</td>
</tr>
<tr>
<td>resume</td>
<td>continues execution of a macro file after a pause command or a breakpoint</td>
</tr>
<tr>
<td>run</td>
<td>advances the simulation by the specified number of timesteps</td>
</tr>
<tr>
<td>runStatus</td>
<td>returns the current state of your simulation after issuing a run or step command</td>
</tr>
<tr>
<td>searchlog</td>
<td>searches one or more of the currently open logfiles for a specified condition</td>
</tr>
<tr>
<td>see</td>
<td>displays the specified number of source file lines around the current execution line</td>
</tr>
<tr>
<td>setenv</td>
<td>sets an environment variable</td>
</tr>
<tr>
<td>shift</td>
<td>shifts macro parameter values down one place</td>
</tr>
<tr>
<td>show</td>
<td>lists objects and subregions visible from the current environment</td>
</tr>
<tr>
<td>simstats</td>
<td>reports performance-related statistics about active simulations</td>
</tr>
<tr>
<td>status</td>
<td>lists all currently interrupted macros</td>
</tr>
<tr>
<td>step</td>
<td>steps to the next HDL statement</td>
</tr>
<tr>
<td>stop</td>
<td>stops simulation in batch files; used with the when command</td>
</tr>
<tr>
<td>suppress</td>
<td>prevents the specified message(s) from displaying</td>
</tr>
<tr>
<td>tb</td>
<td>displays a stack trace for the current process in the Transcript window</td>
</tr>
<tr>
<td>Time</td>
<td>performs various numerical comparisons, operations, and conversions on simulation time values</td>
</tr>
<tr>
<td>transcript</td>
<td>controls echoing of commands executed in a macro file; also works at top level in batch mode</td>
</tr>
<tr>
<td>transcript file</td>
<td>sets or queries the pathname for the transcript file</td>
</tr>
<tr>
<td>tssi2mti</td>
<td>converts a vector file in Technology Standard Events Format (TSSI) into a sequence of force and run commands</td>
</tr>
<tr>
<td>ui_VVMode</td>
<td>specifies behavior when encountering user interface registration calls used by verification packages, such as AVM or OVM</td>
</tr>
</tbody>
</table>
### Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsetenv</td>
<td>deletes an environment variable</td>
</tr>
<tr>
<td>vcd add</td>
<td>adds the specified objects to the VCD file</td>
</tr>
<tr>
<td>vcd checkpoint</td>
<td>dumps the current values of all VCD variables to the VCD file</td>
</tr>
<tr>
<td>vcd comment</td>
<td>inserts the specified comment in the VCD file</td>
</tr>
<tr>
<td>vcd dumpports</td>
<td>creates a VCD file that captures port driver data</td>
</tr>
<tr>
<td>vcd dumpportsall</td>
<td>creates a checkpoint in the VCD file that shows the current values of all selected ports</td>
</tr>
<tr>
<td>vcd dumpportsflush</td>
<td>flushes the VCD buffer to the VCD file</td>
</tr>
<tr>
<td>vcd dumpportslimit</td>
<td>specifies the maximum size of the VCD file</td>
</tr>
<tr>
<td>vcd dumpportsoff</td>
<td>turns off VCD dumping and records all dumped port values as x</td>
</tr>
<tr>
<td>vcd dumpportson</td>
<td>turns on VCD dumping and records the current values of all selected ports</td>
</tr>
<tr>
<td>vcd file</td>
<td>specifies the filename and state mapping for the VCD file created by a vcd add command</td>
</tr>
<tr>
<td>vcd files</td>
<td>specifies filenames and state mapping for the VCD files created by the vcd add command; supports multiple VCD files</td>
</tr>
<tr>
<td>vcd flush</td>
<td>flushes the contents of the VCD file buffer to the VCD file</td>
</tr>
<tr>
<td>vcd limit</td>
<td>specifies the maximum size of the VCD file</td>
</tr>
<tr>
<td>vcd off</td>
<td>turns off VCD dumping and records all VCD variable values as x</td>
</tr>
<tr>
<td>vcd on</td>
<td>turns on VCD dumping and records the current values of all VCD variables</td>
</tr>
<tr>
<td>vcd2wlf</td>
<td>translates VCD files into WLF files</td>
</tr>
<tr>
<td>vcom</td>
<td>compiles VHDL design units</td>
</tr>
<tr>
<td>vdel</td>
<td>deletes a design unit from a specified library</td>
</tr>
<tr>
<td>vdir</td>
<td>lists the contents of a design library</td>
</tr>
<tr>
<td>vencrypt</td>
<td>encrypts Verilog code contained within encryption envelopes</td>
</tr>
<tr>
<td>verror</td>
<td>prints a detailed description of a message number</td>
</tr>
<tr>
<td>vgencomp</td>
<td>writes the equivalent VHDL component declaration for a Verilog module to standard output</td>
</tr>
<tr>
<td>view</td>
<td>opens a ModelSim window and brings it to the front of the display</td>
</tr>
<tr>
<td>virtual count</td>
<td>counts the number of currently defined virtuals that were not read in using a macro file</td>
</tr>
</tbody>
</table>
### Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>virtual define</td>
<td>prints the definition of a virtual signal or function in the form of a command that can be used to re-create the object</td>
</tr>
<tr>
<td>virtual delete</td>
<td>removes the matching virtuals</td>
</tr>
<tr>
<td>virtual describe</td>
<td>prints a complete description of the data type of one or more virtual signals</td>
</tr>
<tr>
<td>virtual expand</td>
<td>produces a list of all the non-virtual objects contained in the virtual signal(s)</td>
</tr>
<tr>
<td>virtual function</td>
<td>creates a new signal that consists of logical operations on existing signals and simulation time</td>
</tr>
<tr>
<td>virtual hide</td>
<td>causes the specified real or virtual signals to not be displayed in the Objects window</td>
</tr>
<tr>
<td>virtual log</td>
<td>causes the sim-mode dependent signals of the specified virtual signals to be logged by the simulator</td>
</tr>
<tr>
<td>virtual nohide</td>
<td>redisplays a virtual previously hidden with virtual hide</td>
</tr>
<tr>
<td>virtual nolog</td>
<td>stops the logging of the specified virtual signals</td>
</tr>
<tr>
<td>virtual region</td>
<td>creates a new user-defined design hierarchy region</td>
</tr>
<tr>
<td>virtual save</td>
<td>saves the definitions of virtuals to a file</td>
</tr>
<tr>
<td>virtual show</td>
<td>lists the full path names of all the virtuals explicitly defined</td>
</tr>
<tr>
<td>virtual signal</td>
<td>creates a new signal that consists of concatenations of signals and subelements</td>
</tr>
<tr>
<td>virtual type</td>
<td>creates a new enumerated type</td>
</tr>
<tr>
<td>vlib</td>
<td>creates a design library</td>
</tr>
<tr>
<td>vlog</td>
<td>compiles Verilog design units and SystemVerilog extensions</td>
</tr>
<tr>
<td>vmake</td>
<td>creates a makefile that can be used to reconstruct the specified library</td>
</tr>
<tr>
<td>vmap</td>
<td>defines a mapping between a logical library name and a directory</td>
</tr>
<tr>
<td>vsim</td>
<td>loads a new design into the simulator</td>
</tr>
<tr>
<td>vsim&lt;info&gt;</td>
<td>returns information about the current vsim executable</td>
</tr>
<tr>
<td>vsim_break</td>
<td>stop the current simulation before completion</td>
</tr>
<tr>
<td>vsource</td>
<td>specifies an alternative file to use for the current source file</td>
</tr>
<tr>
<td>wave</td>
<td>commands for manipulating cursors, for zooming, and for adjusting the wave display view in the Wave window</td>
</tr>
</tbody>
</table>
Table 2-1. Supported Commands (cont.)

<table>
<thead>
<tr>
<th>Command name</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>when</td>
<td>instructs ModelSim to perform actions when the specified conditions are met</td>
</tr>
<tr>
<td>where</td>
<td>displays information about the system environment</td>
</tr>
<tr>
<td>wlf2log</td>
<td>translates a ModelSim WLF file to a QuickSim II logfile</td>
</tr>
<tr>
<td>wlf2vcd</td>
<td>translates a ModelSim WLF file to a VCD file</td>
</tr>
<tr>
<td>wlfman</td>
<td>outputs information about or a new WLF file from an existing WLF file</td>
</tr>
<tr>
<td>wlfrecover</td>
<td>attempts to repair an incomplete WLF file</td>
</tr>
<tr>
<td>write format</td>
<td>records the names and display options in a file of the objects currently being displayed in the List or Wave window</td>
</tr>
<tr>
<td>write list</td>
<td>records the contents of the List window in a list output file</td>
</tr>
<tr>
<td>write preferences</td>
<td>saves the current GUI preference settings to a Tcl preference file</td>
</tr>
<tr>
<td>write report</td>
<td>prints a summary of the design being simulated</td>
</tr>
<tr>
<td>write timing</td>
<td>prints timing information about the specified instance</td>
</tr>
<tr>
<td>write transcript</td>
<td>writes the contents of the Main window transcript to the specified file</td>
</tr>
<tr>
<td>write tssi</td>
<td>records the contents of the List window in a “TSSI format” file</td>
</tr>
<tr>
<td>write wave</td>
<td>records the contents of the Wave window in PostScript format</td>
</tr>
</tbody>
</table>
abort

This command halts the execution of a macro file interrupted by a breakpoint or error.

When macros are nested, you may choose to abort the last macro only, abort a specified number of nesting levels, or abort all macros. You can specify this command within a macro to return early.

Syntax

abort [<n> | all]

Arguments

• <n>
  (optional) The number of nested macro levels to abort. Specified as an integer greater than 0, where the default value is 1.

• all
  (optional) Instructs the tool to abort all levels of nested macros.

Related Topics

• onbreak
• onElabError
• onerror
add dataflow

This command adds the specified process, signal, net, or register to the Dataflow window. Wildcards are allowed.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

add dataflow <object> ... [-connect <source_net> <destination_net>] 

Arguments

- <object> ...
  (required unless specifying -connect) Specifies a process, signal, net, or register to add to the Dataflow window. Wildcards are allowed. Multiple objects are specified as a space separated list. Refer to the section “Wildcard Characters” for wildcard usage as it pertains to the add commands. Must be specified as the first argument to the add dataflow command.

- -connect <source_net> <destination_net>
  (optional) Computes and displays in the Dataflow window all paths between two nets.
  <source_net> — The net that originates the path search.
  <destination_net> — The net that terminates the path search.

- -in
  (optional) Specifies to add ports of mode IN.

- -inout
  (optional) Specifies to add ports of mode INOUT.

- -out
  (optional) Specifies to add ports of mode OUT.

- -ports
  (optional) Specifies to add all ports. This switch has the same effect as specifying -in, -out, and -inout together.

- -internal
  (optional) Specifies to add internal (non-port) objects.

- -nofilter
  (optional) Specifies that the WildcardFilter Tcl preference variable be ignored when finding signals or nets.

The WildcardFilter Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.
-recursive

( optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

You can specify -r as an alias to this switch.

**Examples**

- Add all objects in the design to the dataflow window.
  ```
  add dataflow -r /*
  ```

- Add all objects in the region to the dataflow window.
  ```
  add dataflow *
  ```

**Related Topics**

- Automatically Tracing All Paths Between Two Nets
- Dataflow Window
- Using the WildcardFilter Preference Variable
add list

This command adds the following objects and their values to the List window:

- VHDL signals and variables
- Verilog nets and registers
- User-defined buses

If you do not specify a port mode, such as -in or -out, this command displays all objects in the selected region with names matching the object name specification.

See “Wildcard Characters” for wildcard usage as it pertains to the add commands.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax


Arguments

- <object> ...
  (required when <object_name> { sig ... } is not specified.) Specifies the name of the object to be listed. Multiple objects are entered as a space separated list. Wildcards are allowed. Refer to the section “Wildcard Characters” for wildcard usage as it pertains to the add commands. Must be specified as the first argument to the add list command.

  Note that the WildcardFilter Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.

  You can add variables as long as they are preceded by the process name. For example:

  add list myproc/int1

  You must specify the <object> argument as the first argument to the add list command.

- <object_name> { sig ... }
  (required when <object> is not specified) Creates a user-defined bus with the specified object name containing the specified signals (sig) concatenated within the user-defined bus. Arguments, must be enclosed in braces ({}). Must be specified as the second argument to the add list command.

  sig — A space-separated list of signals, enclosed in braces ({}), that are included in the user-defined bus. The signals may be either scalars or various sized arrays as long as they have the same element enumeration type.

  For example:

  add list {mybus {a b y}}
-allowconstants
  (optional) *For use with wildcard searches.* Specifies that constants matching the wildcard search should be added to the List window.

  This command does not add constants by default because they do not change.

-<level>
  (optional) Restricts a recursive search, as specified with -recursive, to a certain level of hierarchy.

  <level> — an integer greater than or equal to zero.

  For example, if you specify **-depth 1**, the command descends only one level in the hierarchy.

-in
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode IN if they match the *object* specification.

-inout
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode INOUT if they match the *object* specification.

-out
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode OUT if they match the *object* specification.

-ports
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include all ports. This switch has the same effect as specifying **-in**, **-out**, and **-inout** together.

-internal
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include internal objects (non-port objects) if they match the *object* specification. VHDL variables are not selected.

-label <name>
  (optional) Specifies an alternative signal name to be displayed as a column heading in the listing.

  <name> — Specifies the label to be used at the top of the column. You must enclose <name> in braces ( {{ }} ) if it includes any spaces.

  This alternative name is not valid in a force or examine command.

-nodelta
  (optional) Specifies that the delta column not be displayed when adding signals to the List window. Identical to configure list -delta none.
**Commands**

**add list**

- `<radix_type>`
  (optional) Specifies the radix type for the objects that follow in the command. Valid entries (or any unique abbreviations) are: binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

  If no radix is specified for an enumerated type, the default radix is used. You can change the default radix for the current simulation using the `radix` command. You can change the default radix permanently by editing the `DefaultRadix` variable in the `modelsim.ini` file.

  If you specify a radix for an array of a VHDL enumerated type, ModelSim converts each signal value to 1, 0, Z, or X.

- `-radix <type>`
  (optional) Specifies a user-defined radix. The `-radix <type>` switch can be used in place of the `-<radix_type>` switch. For example, `-radix hexadecimal` is the same as `-hex`.

    `<type>` — binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

- `-radixenumnumeric`
  (optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

- `-radixenumsymbolic`
  (optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the `-radixenumnumeric` option.

- `-recursive`
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

  You can use the `-depth` argument to specify how far down the hierarchy to descend. You can use "-r" as an alias to this switch.

- `-trigger | -notrigger`
  (optional) Specifies whether objects should be updated in the List window when the objects change value.

    -trigger — (default) Update objects in the List Window when their values change.
    -notrigger — Do not update objects in the List Window when their values change.

- `-width <integer>`
  (optional) Formats the column width.

    `<integer>` — A positive integer specifying the column width in characters.

**Examples**

- List all objects in the design.

  ```
  add list -r /*
  ```

- List all objects in the region.
add list *

• List all input ports in the region.

add list -in *

• Display a List window containing three columns headed a, sig, and array_sig(9 to 23).

add list a -label sig /top/lower/sig {array_sig(9 to 23)}

• List clk, a, b, c, and d only when clk changes.

add list clk -notrigger a b c d

• Lists clk, a, b, c, and d every 100 ns.

config list -strobeperiod {100 ns} -strobestart {0 ns} -usestrobe 1
add list -notrigger clk a b c d

• Creates a user-defined bus named "mybus" consisting of three signals; the bus is displayed in hex.

add list -hex {mybus {msb {opcode(8 downto 1)} data}}

• Lists the object vec1 using symbolic values, lists vec2 in hexadecimal, and lists vec3 and vec4 in decimal.

add list vec1 -hex vec2 -dec vec3 vec4

Related Topics

• add wave
• log
• Extended Identifiers
• Using the WildcardFilter Preference Variable
add memory

This command displays the contents and sets the address and data radix of the specified memory in the MDI frame of the Main window.

See “Wildcard Characters” for wildcard usage as it pertains to the add commands.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

```
add memory [-addressradix {decimal | hex}] [-dataradix <type>]
  [-radixenumnumeric | -radixenumsymbolic] [-wordsperline <num>] <object_name> ...
```

Arguments

- **-addressradix {decimal | hex}**
  (optional) Specifies the address radix for the memory display.
  - decimal — (default) Sets the radix to decimal. You can abbreviate this argument to "d".
  - hex — Sets the radix to hexadecimal. You can abbreviate this argument to "h".

- **-dataradix <type>**
  (optional) Specifies the data radix for the memory display. If you do not specify this switch, the command uses the global default radix.
  - <type> — binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.
  If you do not specify a radix for an enumerated type, the command uses the symbolic representation.

  You can change the default radix for the current simulation using the `radix` command. You can change the default radix permanently by editing the `DefaultRadix` variable in the `modelsim.ini` file. Changing the default radix does not change the radix of the currently displayed memory. Use the `add memory` command to re-add the memory with the desired radix, or change the display radix from the Memory window Properties dialog.

- **-radixenumnumeric**
  (optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

- **-radixenumsymbolic**
  (optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the -radixenumnumeric option.

- **-wordsperline <num>**
  (optional) Specifies how many words are displayed on each line in the memory window. By default, the information displayed will wrap depending on the width of the window.
  - num — Any positive integer
• `<object_name> ...`
  (required) Specifies the hierarchical path of the memory to be displayed. Multiple memories are specified as a space separated list. Must be specified as the final argument to the `add memory` command.

  Wildcard characters are allowed.

**Note**

The `WildcardFilter` Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.)

**Related Topics**

- Memory and Memory Data Windows
- Using the WildcardFilter Preference Variable
add watch

This command adds signals and variables to the Watch window in the Main window. See “Wildcard Characters” for wildcard usage as it pertains to the add commands.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

add watch <object_name> ... [-radix <type>] [-radixenumnumeric | -radixenumsymbolic]

Arguments

- <object_name> ...
  (required) Specifies the name of the object to be added. Multiple objects are entered as a space separated list. Must be specified as the first argument to the add watch command.
  Wildcard characters are allowed. (Note that the WildcardFilter Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.)
  Variables must be preceded by the process name. For example,
  
  add watch myproc/int1

- -radix <type>
  (optional) Specifies a user-defined radix.
  (optional) Specifies a user-defined radix. If you do not specify this switch, the command uses the global default radix.
  
  <type> — binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.
  You can change the default radix for the current simulation using the radix command. You can change the default radix permanently by editing the DefaultRadix variable in the modelsim.ini file.

- -radixenumnumeric
  (optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

- -radixenumsymbolic
  (optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the -radixenumnumeric option.

Related Topics

- Watch window
- Using the WildcardFilter Preference Variable
add wave

This command adds the following objects to the Wave window:

- VHDL signals and variables
- Verilog nets and registers
- SystemVerilog class objects
- Dividers and user-defined buses.

If no port mode is specified, this command will display all objects in the selected region with names matching the object name specification.

See “Wildcard Characters” for wildcard usage as it pertains to the add commands.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

```
add wave [ -allowconstants ] [ -clampanalog {0 | 1} ] [ -color <standard_color_name> ]
[ -depth <level> ] [ [ -divider [ <divider_name> ... ] ] [ -expand <signal_name> ]
[ -format <type> | -<format> ] [ -group [ <group_name> [ <sig_name1> ... ] ] ] [ -height <pixels> ]
{ [ -in ] | [ -inout ] | [ -out ] | [ -ports ] } [ -internal ] [ -label <name> ] [ -max <real_num> ]
[ -min <real_num> ] [ -noupdate ] [ -position <location> ]
[ -<radix_type> | -radix <type> ] [ -radixenumnumeric | -radixenumsymbolic ] [ -recursive ]
[ -time ] [ [ <object_name> ... ] [ { <object_name> [ <sig1> <sig2> ... ] } ] ]
```

Arguments

- **-allowconstants**
  (optional) *For use with wildcard searches.* Specifies that constants matching the wildcard search should be added to the Wave window.
  By default, constants are ignored because they do not change.

- **-clampanalog {0 | 1}**
  (optional) Clamps the display of an analog waveform to the values specified by **-max** and **-min**. Specifying a value of 1 prevents the waveform from extending above the value specified for **-max** or below the value specified for **-min**.
  
  0 — not clamped
  1 — (default) clamped

- **-color <standard_color_name>**
  (optional) Specifies the color used to display a waveform.
  
  `<standard_color_name>` — You can use either of the following:
  standard X Window color name — enclose 2-word names in quotes ("), for example:
  ```
  -color "light blue"
  ```
rgb value — for example:
  -color #357f77

- depth <level>
  (optional) Restricts a recursive search, as specified with -recursive to a specified level of hierarchy.
  <level> — Any integer greater than or equal to zero. For example, if you specify -depth 1, the command descends only one level in the hierarchy.

- divider [ <divider_name> ... ]
  (optional) Adds a divider to the Wave window. If you do not specify this argument, the command inserts an unnamed divider.
  <divider_name> ... — Specifies the name of the divider, which appears in the pathnames column. Multiple objects entered as a space separated list.
  When you specify more than one <divider_name> the command creates a divider for each name.
  You can begin a name with a space, but you must enclose the name within quotes (" ) or braces ({ }) You cannot begin a name with a hyphen (-).

- expand <signal_name>
  (optional) Instructs the command to expand a compound signal immediately, but only one level down.
  <signal_name> — Specifies the name of the signal. This string can include wildcards.

- format <type> | -<format>
  (optional) Specifies the display format of the objects. Valid entries are:

<table>
<thead>
<tr>
<th>-format &lt;type&gt;</th>
<th>-&lt;format&gt;</th>
<th>Display Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>-format literal</td>
<td>-literal</td>
<td>Literal waveforms are displayed as a box containing the object value.</td>
</tr>
<tr>
<td>-format logic</td>
<td>-logic</td>
<td>Logic signals may be U, X, 0, 1, Z, W, L, H, or ‘-’.</td>
</tr>
<tr>
<td>-format analog-step</td>
<td>-analog-step</td>
<td>Analog-step changes to the new time before plotting the new Y.</td>
</tr>
<tr>
<td>-format analog-interpolated</td>
<td>-analog-interpolated</td>
<td>Analog-interpolated draws a diagonal line.</td>
</tr>
<tr>
<td>-format analog-backstep</td>
<td>-analog-backstep</td>
<td>Analog-backstep plots the new Y before moving to the new time.</td>
</tr>
<tr>
<td>-format event</td>
<td>-event</td>
<td>Displays a mark at every transition.</td>
</tr>
</tbody>
</table>
The Y-axis range of analog signals is bounded by `-max` and `-min` switches.

- `-group <group_name> [<sig_name1> ...]`
  (optional) Creates a wave group with the specified group_name.
  
  `<group_name>` — Specifies the name of the group. You must enclose this argument in quotes (""") or braces ({ }) if it contains any spaces.
  
  `<sig_name>` ... — Specifies the signals to add to the group. Multiple signals are entered as a space separated list. This command creates an empty group if you do not specify any signal names.

- `-height <pixels>`
  (optional) Specifies the height of the waveform in pixels.
  
  `<pixels>` — Any positive integer.

- `-in`
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode IN if they match the object_name specification.

- `-out`
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode OUT if they match the object_name specification.

- `-inout`
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include ports of mode INOUT if they match the object_name specification.

- `-ports`
  (optional) *For use with wildcard searches.* Specifies that the scope of the listing is to include ports of modes IN, OUT, or INOUT.

- `-internal`
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to include internal objects (non-port objects) if they match the object_name specification.

- `-label <name>`
  (optional) Specifies an alternative name for the signal being added. For example,

  ```text
  add wave -label c clock
  ```

  adds the `clock` signal, labeled as "c".

  This alternative name is not valid in a `force` or `examine` command.

- `-max <real_num>`
  (optional) Specifies the maximum Y-axis data value to be displayed for an analog waveform. Used in conjunction with the `-min` switch; the value you specify for `-max` must be greater than the value you specify for `-min`.
  
  `<real_num>` — Any integer that is greater than the value specified for `-min`. 

---

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add wave

- **-min <real_num>**
  (optional) Specifies the minimum Y-axis data value to be displayed for an analog waveform. Used in conjunction with the **-max** switch; the value you specify for **-min** must be less than the value you specify for **-max**.

  <real_num> — Any integer that is less than the value specified for **-max**.

  For example, if you know the Y-axis data for a waveform varies between 0.0 and 5.0, you could add the waveform with the following command:

  ```
  add wave -analog -min 0 -max 5 -height 100 my_signal
  ```

- **-noupdate**
  (optional) Prevents the Wave window from updating when a series of add wave commands are executed in series.

- **-position <location>**
  (optional) Specifies where the command adds the signals.

  <location> — Can be any of the following:

  top — Adds the signals to the beginning of the list of signals.

  bottom | end — Adds the signals to the end of the list of signals.

  before | above — Adds the signals to the location before the first selected signal in the wave window.

  after | below — Adds the signals to the location after the first selected signal in the wave window.

  <integer> — Adds the signals beginning at the specified point in the list of signals.

- **-<radix_type>**
  (optional) Specifies the radix type for the objects that follow in the command. Valid entries (or any unique abbreviations) are: binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

  If no radix is specified for an enumerated type, the default radix is used. You can change the default radix for the current simulation using the **radix** command. You can change the default radix permanently by editing the **DefaultRadix** variable in the **modelsim.ini** file.

  If you specify a radix for an array of a VHDL enumerated type, ModelSim converts each signal value to 1, 0, Z, or X.

- **-radix <type>**
  (optional) Specifies a user-defined radix. The **-radix <type>** switch can be used in place of the **-<radix_type>** switch. For example, -radix hexadecimal is the same as -hex.

---

**Note**

Although **-offset** and **-scale** are still supported, the **-max** and **-min** arguments provide an easier way to define upper and lower limits of an analog waveform.
<type> — binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

- **-radixenumnumeric**
  (optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

- **-radixenumsymbolic**
  (optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the -radixenumnumeric option.

- **-recursive**
  (optional) *For use with wildcard searches.* Specifies that the scope of the search is to descend recursively into subregions.

  If you do not specify this switch, the search is limited to the selected region. You can use the `-depth` argument to specify how far down the hierarchy to descend.

- **-time**
  (optional) Use time as the radix for Verilog objects that are register-based types (register vectors, time, int, and integer types).

- **<object_name> ...**
  (required unless specifying `{<object_name> {sig1 sig2 ...}}`) Specifies the names of objects to be included in the Wave window. Must be specified as the final argument to the `add wave` command. Wildcard characters are allowed. Multiple objects are entered as a space separated list. Note that the `WildcardFilter` Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.

  Variables may be added if preceded by the process name. For example,

  `add wave myproc/int1`

- **{<object_name> {sig1 sig2 ...}}**
  (required unless specifying `<object_name>`) Creates a user-defined bus with the specified object name containing the specified signals (sig1 and so forth) concatenated within the user-defined bus. Must be specified as the final argument to the `add wave` command.

  **sig** — A space-separated list of signals, enclosed in braces ( `{ }` ), that are included in the user-defined bus. The signals may be either scalars or various sized arrays as long as they have the same element enumeration type.

**Note**

You can also select **Wave > Combine Signals** (when the Wave window is selected) to create a user-defined bus.

**Examples**

- Display an object named `out2`. The object is specified as being a logic object presented in gold.
add wave -logic -color gold out2

- Display a user-defined, hex formatted bus named \textit{address}.
  
\texttt{add wave -hex \{address \{a\_7 a\_6 a\_5 a\_4 a\_3 a\_2 a\_1 a\_0\}\}}

- Add all wave objects in the region.
  
\texttt{add wave *}

- Add all wave input ports in the region.
  
\texttt{add wave -in *}

- Create a user-defined bus named "mybus" consisting of three signals. \textit{Scalar1} and \textit{scalar2} are of type std\_logic and \textit{vector1} is of type std\_logic\_vector (7 downto 1). The bus is displayed in hex.
  
\texttt{add wave -hex \{mybus \{scalar1 vector1 scalar2\}\}}

Slices and arrays may be added to the bus using either VHDL or Verilog syntax. For example:

\texttt{add wave \{vector3(1)\}}

\texttt{add wave \{vector3[1]\}}

\texttt{add wave \{vector3(4 downto 0)\}}

\texttt{add wave \{vector3[4:0]\}}

- Add the object \textit{vec1} to the Wave window using symbolic values, adds \textit{vec2} in hexadecimal, and adds \textit{vec3} and \textit{vec4} in decimal.

\texttt{add wave vec1 -hex vec2 -dec vec3 vec4}

- Add a divider with the name "-Example-". Note that for this to work, the first hyphen of the name must be preceded by a space.

\texttt{add wave -divider " -Example- "}

- Add an unnamed divider.

\texttt{add wave -divider \"\}}

\texttt{add wave -divider "\}}

\texttt{add wave -divider \{\}}

\textbf{Related Topics}

- add list
- log
- Concatenation Directives
- Extended Identifiers
- Using the WildcardFilter Preference
- Variable
- See Wave Window for more information
  on analog formats of waveform signals.
add_cmdhelp

This command adds the specified command name, description, and command arguments to the command-line help. You can then access the information using the help command.

To delete an entry, invoke the command with an empty command description and arguments. See examples.

The arguments to this command are order-dependent. Please read through the argument descriptions for more information.

Syntax
add_cmdhelp {<command_name>} {<command_description>} {<command_arguments>}

Arguments

- {<command_name>}
  (required) Specifies the command name that will be entered as an argument to the help command. Must be enclosed in braces ({ }). The command_name must not interfere with an already existing command_name. Must be specified as the first argument to the add_cmdhelp command.

- {<command_description>}
  (required) Specifies a description of the command. Must be enclosed in braces ({ }). Must be specified as the second argument to the add_cmdhelp command.

- {<command_arguments>}
  (required) A space-separated list of arguments for the command. Must be enclosed in braces ({ }). If the command doesn’t have any arguments, enter {}. Must be specified as the third argument to the add_cmdhelp command.

Examples

- Add a command named "date" with no arguments.
  
  add_cmdhelp date {Displays date and time.} {}

  Entering:
  
  VSIM> help date

  returns:
  
  Displays date and time.
  Usage: date

- Add the change date command.
  
  add_cmdhelp {change date} {Modify date or time.} {-time|-date <arg>}

  Entering:
  
  VSIM> help change date
returns:

Modify data or time.
Usage: change date -time|-date <arg>

• Deletes the change date command from the command-line help.

   add_cmdhelp {change date} {} {}
**alias**

This command displays or creates user-defined aliases. Any arguments passed on invocation of the alias will be passed through to the specified commands.

Returns nothing. Existing commands (e.g., run, env, etc.) cannot be aliased.

**Syntax**

```markdown
alias [<name> ["<cmds>"]]
```

**Arguments**

- `<name>`
  
  (optional) Specifies the new procedure name to be used when invoking the commands.

- "<cmds>"
  
  (optional) Specifies the command or commands to be evaluated when the alias is invoked. Multiple commands are specified as a semicolon (;) separated list. You must enclose the string in quotes (""").

**Examples**

- List all aliases currently defined.
  
  ```markdown
  alias
  ```

- List the alias definition for the specified name if one exists.
  
  ```markdown
  alias <name>
  ```

- Create a Tcl procedure, "myquit", that when executed, writes the contents of the List window to the file mylist.save by invoking write list, and quits ModelSim by invoking quit.
  
  ```markdown
  alias myquit "write list ./mylist.save; quit -f"
  ```
**batch_mode**

This command returns “1” if ModelSim is operating in batch mode, otherwise it returns “0.” It is typically used as a condition in an if statement.

**Syntax**

```
batch_mode
```

**Arguments**

None

**Examples**

Some GUI commands do not exist in batch mode. If you want to write a script that will work in or out of batch mode, you can use the `batch_mode` command to determine which command to use. For example:

```
if [batch_mode] {
    log /*
} else {
    add wave /*
}
```

**Related Topics**

- Modes of Operation
This command deletes a breakpoint. You can delete multiple breakpoints by specifying separate information groupings on the same command line.

Arguments to this command are order-dependent. Please read through the argument descriptions for more information.

Syntax

\[
\text{bd } \begin{cases} \langle \text{filename} \rangle \text{ } \langle \text{line_number} \rangle \\ \langle \text{id_number} \rangle \text{ } | \text{ } \langle \text{label} \rangle \end{cases}
\]

Arguments

- \(\langle \text{filename} \rangle\)
  (required when not specifying \(\langle \text{id_number} \rangle\) or \(\langle \text{label} \rangle\).) A string that specifies the name of the source file in which the breakpoint is to be deleted. The filename must match the one used previously to set the breakpoint, including whether you used a full pathname or a relative name. Must be specified as the first argument to the \text{bd} command.

- \(\langle \text{line_number} \rangle\)
  (required) A string that specifies the line number of the breakpoint to be deleted.

- \(\langle \text{id_number} \rangle \text{ } | \text{ } \langle \text{label} \rangle\)
  (required when not specifying \(\langle \text{filename} \rangle\).) Specifies the identification of breakpoints using markers assigned by the \text{bp} command. Must be specified as the first argument to the \text{bd} command.

  \(\langle \text{id_number} \rangle\) — A string that specifies the identification number of the breakpoint to be deleted. The identification number is set with the \text{-id} argument to the \text{bp} command.

  \(\langle \text{label} \rangle\) — A string that specifies the label of the breakpoint to be deleted. The label is set with the \text{-label} switch to the \text{bp} command.

Examples

- Delete the breakpoint at line 127 in the source file named \text{alu.vhd}.
  \[
  \text{bd alu.vhd 127}
  \]

- Delete the breakpoint with id# 5.
  \[
  \text{bd 5}
  \]

- Delete the breakpoint with the label top_bp
  \[
  \text{bd top_bp}
  \]

- Delete the breakpoint with id# 6 and the breakpoint at line 234 in the source file named \text{alu.vhd}.
  \[
  \text{bd alu.vhd 234}
  \]
Commands

bd

bd 6 alu.vhd 234

Related Topics

- bp
- onbreak
**bookmark add wave**

This command creates a named reference to a specific zoom range and scroll position in the specified Wave window. Bookmarks are saved in the wave format file and are restored when the format file is read.

You can also interactively add a bookmark through the GUI by selecting the **Wave > Bookmarks > Bookmarks** menu item.

Arguments to this command are order-dependent. Please read through the argument descriptions for more information.

**Syntax**

```
bookmark add wave <label> [[<range_start> [<unit>]] [<range_end> [<unit>]] [<topindex>]]
```

**Arguments**

- `<label>`
  
  (required) A string that specifies the name for the bookmark. Must be specified as the first argument to the **bookmark add wave** command.

- `<range_start> [<unit>]`
  
  (optional) Specifies the beginning point of the zoom range where the default starting point is zero (0).

  `<unit>` — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting `<unit>`. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr. If `<unit>` is specified, you must enclose `<limit>` and `<unit>` within curly braces ({}).

  The complete grouping of `<range_start>` and `<range_end>` must also be enclosed in braces ({})) or quotes (""), for example:

  ```
  {{100 ns} {10000 ns}}
  {10000}
  ```

- `<range_end> [<unit>]`
  
  (optional) Specifies the end point of the zoom range.

  `<unit>` — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting `<unit>`. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr. If `<unit>` is specified, you must enclose `<limit>` and `<unit>` within curly braces ({}).

- `<topindex>`
  
  (optional) An integer that specifies the vertical scroll position of the window. You must specify a zoom range to specify **topindex**. The number identifies which object the window should be scrolled to. For example, specifying 20 means the Wave window will be scrolled down to show the 20th object.
Commands

**bookmark add wave**

**Examples**

- Add a bookmark named "foo" to the current default Wave window. The bookmark marks a zoom range from 10ns to 1000ns and a scroll position of the 20th object in the window.

  `bookmark add wave foo {{10 ns} {1000 ns}} 20`

**Related Topics**

- bookmark delete wave
- bookmark goto wave
- bookmark list wave
- write format
**bookmark delete wave**

This command deletes bookmarks from the specified Wave window.

You can also interactively delete a bookmark through the GUI by selecting the **Wave > Bookmarks > Bookmarks** menu item.

Arguments to this command are order-dependent. Please read through the argument descriptions for more information.

**Syntax**

`bookmark delete wave {<label> | -all }`

**Arguments**

- `<label> | -all`
  
  (required) Controls which bookmarks to delete. Must be specified as the first argument to the `bookmark delete wave` command.

  - `<label>` — Specifies the name of the bookmark to delete.
  - `-all` — Specifies that all bookmarks in the window be deleted.

**Examples**

- Delete the bookmark named "foo" from the current default Wave window.

  `bookmark delete wave foo`

**Related Topics**

- `bookmark add wave`
- `bookmark goto wave`
- `bookmark list wave`
- `write format`
bookmark goto wave

This command zooms and scrolls a Wave window using the specified bookmark.

You can also interactively navigate between bookmarks through the GUI by selecting the Wave > Bookmarks > Bookmarks menu item.

Arguments to this command are order-dependent. Please read through the argument descriptions for more information.

Syntax

bookmark goto wave <label>

Arguments

• <label> (required) Specifies the bookmark to go to. Must be specified as the first argument to the bookmark goto wave command.

Related Topics

• bookmark add wave
• bookmark delete wave
• bookmark list wave
• write format
**bookmark list wave**

This command displays a list of available bookmarks in the Transcript window.

**Syntax**

```
bookmark list wave
```

**Related Topics**

- bookmark add wave
- bookmark delete wave
- bookmark goto wave
- write format
bp

This command sets either a file-line breakpoint or returns a list of currently set breakpoints. It allows enum names, as well as literal values, to be used in condition expressions.

Arguments to this command are order-dependent. Please read through the argument descriptions for more information.

Syntax

Setting an HDL breakpoint

```plaintext
bp { <filename> <line_number> } [-appendinst] [ <command> ... ]
   [-cond "<condition_expression>" ] [-disable] [-id <id_number> | -label "<label>" ]
   [-inst <region> [-inst <region> ... ]] ...
```

Querying a breakpoint

```plaintext
bp [-query <filename> [ <line_number> ]] ...
```

Reporting all breakpoints

If you specify this command with no arguments, it returns a list of all breakpoints in the design containing information about each breakpoint. For example:

```plaintext
bp
```

returns:

```plaintext
# bp top.vhd 70; # 2
```

- `bp` — an echo of the command
- `<file_name>`
- `<line_number>`
- `# <id_number>`

Arguments

- `<filename>`
  (required to set an HDL breakpoint) Specifies the name of the source file in which to set the breakpoint. Must be specified as the first argument to the `bp` command.

- `<line_number>`
  (required to set an HDL breakpoint) Specifies the line number where the breakpoint is to be set. Must be specified as the second argument to the `bp` command.

- `-appendinst`
  (optional) When specifying multiple breakpoints with `-inst`, append each instance-path condition to the earlier condition. This overrides the default behavior, in which each condition overwrites the previous one.
- **-disable**
  (optional) Sets the breakpoint to a disabled state. You can enable the breakpoint later using the `enablebp` command. This command enables breakpoints by default.

- **<command>…**
  (optional) Specifies one or more commands that are to be executed at the breakpoint. You must separate multiple commands with semicolons (;) or place them on multiple lines. Braces are required only if the string contains spaces.

  **Note**
  You can also specify this command string by choosing **Tools > Breakpoints...** from the main menu and using the **Modify Breakpoints** dialog box.

  Any commands that follow a `run` or `step` command are ignored. A run or step command terminates the breakpoint sequence. This rule also applies if you use a macro within the command string.

  If many commands are needed after the breakpoint, you could place them in a macro file.

- **-cond "<condition_expression>"**
  (optional) Specifies condition(s) that determine whether the breakpoint is hit.

  "<condition_expression>" — A conditional expression that results in a true/false value. You must enclose the condition expression within quotation marks (" ").

  If the condition is true, the simulation stops at the breakpoint. If false, the simulation bypasses the breakpoint. A condition cannot refer to a VHDL variable (only a signal).

  The `-cond` switch re-parses expressions each time the breakpoint is hit. This allows expressions with local references to work. Condition expressions referencing items outside the context of the breakpoint must use absolute names. This is different from the behavior in previous ModelSim versions where a relative signal name was resolved at the time the `bp` command was issued, allowing the breakpoint to work even though the relative signal name was inappropriate when the breakpoint was hit.

  **Note**
  You can also specify this expression by choosing **Tools > Breakpoints...** from the main menu and using the **Modify Breakpoints** dialog box.

  The condition expression can use the following operators:

<table>
<thead>
<tr>
<th>Operation</th>
<th>Operator Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>equals</td>
<td>==, =</td>
</tr>
<tr>
<td>not equal</td>
<td>!-, /=</td>
</tr>
<tr>
<td>AND</td>
<td>&amp;&amp;, AND</td>
</tr>
<tr>
<td>OR</td>
<td></td>
</tr>
</tbody>
</table>
The operands may be object names, `signame` event, or constants. Subexpressions in parentheses are permitted. The command will be executed when the expression is evaluated as TRUE or 1. The formal BNF syntax for an expression is:

```
condition ::= Name | { expression }
expression ::= expression AND relation
            | expression OR relation
relation ::= Name = Literal
           | Name /= Literal
           | Name ` EVENT
           | ( expression )
Literal ::= '<char>' | "<bitstring>" | <bitstring>
```

The "=" operator can occur only between a Name and a Literal. This means that you cannot compare the value of two signals (for example, Name = Name is not valid).

You can construct a breakpoint such that the simulation breaks when a SystemVerilog Class is associated with a specific handle, or address:

```
bp <filename> <line_number> -cond "this==<class_handle>"
bp <filename> <line_number> -cond "this!=<class_handle>"
```

where you can obtain the class handle with the `examine` `-handle` command. The string "this" is a literal that refers to the specific `line_number`.

You can construct a breakpoint such that the simulation breaks when a line number is of a specific class type or extends the specified class type:

```
bp <filename> <line_number> -cond "this ISA <class_type_name>"
```

where `class_type_name` is the actual class name, not a variable.

- `-id <id_number> | -label "<label>"` (optional) Attempts to assign an id number or label to the breakpoint. The command returns an error if the id number you specify is already assigned.
  - `-id <id_number>` — Any positive integer that is not already assigned.
  - `-label "<label>"` — Associates a name or label with the specified breakpoint. Adds a level of identification to the breakpoint. The label may contain special characters. Quotation marks (" ") or braces ({ }) are required only if `<label>` contains spaces or special characters.

**Note**

Id numbers for breakpoints are assigned from the same pool as those used for the `when` command. So even if you have not specified a given id number for a breakpoint, that number may still be used for a `when` command.

- `-inst <region> [-inst <region> ...]` (optional) Sets an HDL breakpoint so it applies only to the specified instance. To apply multiple instance-path conditions on a single breakpoint, specify `-inst <region>` multiple
times. By default, this overrides the previous breakpoint condition (you can use the -appendinst argument to append conditions instead).

<region> — The full path to the instance specified.

Note
You can also specify this instance by choosing Tools > Breakpoints... from the main menu and using the Modify Breakpoints dialog box.

-query <filename> [line_number]
(optional) Returns information about the breakpoint(s) set in the specified file. The information returned varies depending on the condition of the breakpoint(s) in the specified file. Returns a complete list of all breakpoints and whether they are enabled or not when specified without line_number. Returns nothing if line_number is not executable.

<filename> — The name of the file containing the breakpoint.
<line_number> — The line number where a breakpoint has been set.

The output contains six fields of information. For example:

bp -query top.vhd 70

returns

  # 1 1 top.vhd 70 2 1

  o {1 | 0} — Indicates whether a breakpoint exists at the location.
    0 — Breakpoint does not exit.
    1 — Breakpoint exists.
  o 1 — always reports a 1.
  o <file_name>
  o <line_number>
  o <id_number>
  o {1 | 0} — Indicates whether the breakpoint is enabled.
    0 — Breakpoint is not enabled.
    1 — Breakpoint is enabled.

Examples

- List all existing breakpoints in the design, including the source file names, line numbers, breakpoint id#s, labels, and any commands that have been assigned to the breakpoints.

  bp

- Set a breakpoint in the source file alu.vhd at line 147.
bp alu.vhd 147
- Execute the macro.do macro file when the breakpoint is hit.
  bp alu.vhd 147 {do macro.do}

- Set a breakpoint on line 22 of test.vhd. When the breakpoint is hit, the values of variables var1 and var2 are examined. This breakpoint is initially disabled; it can be enabled with the enablebp command.
  bp -disable test.vhd 22 {echo [exa var1]; echo [exa var2]}

- Set a breakpoint in every instantiation of the file test.vhd at line 14. When that breakpoint is executed, the Tcl command is run. This Tcl command causes the simulator to continue if the current simulation time is not 100.
  bp test.vhd 14 {if {$now / 100} then {cont}}

- Set a breakpoint so that the simulation pauses whenever clk=1 and prdy=0:
  bp test.vhd 14 -cond "clk=1 AND prdy=0"

- Set a breakpoint with the label top_bp
  bp top.vhd 14 -label top_bp

- Set a breakpoint for line 15 of a.vhd, but only for the instance a2:
  bp a.vhd 15 -inst "/top/a2"

- Set multiple breakpoints in the source file test.vhd at line 14. The second instance will overwrite the conditions of the first.
  bp test.vhd 14 -inst /test/inst1 -inst /test/inst2

- Set multiple breakpoints at line 14. The second instance will append its conditions to the first.
  bp test.vhd 14 -inst /test/inst1 -inst /test/inst2 -appendinst

- Set a breakpoint for a specific variable of a particular class type:
  set x [examine -handle my_class_var]
  bp top.sv 15 -cond "this == $x"

- List the line number and enabled/disabled status (1 = enabled, 0 = disabled) of all breakpoints in testadd.vhd.
  bp -query testadd.vhd

- List details about the breakpoint on line 48.
  bp -query testadd.vhd 48

- List all executable lines in testadd.vhd between lines 2 and 59.
  bp -query testadd.vhd 2 59
Note

Any breakpoints set in VHDL code and called by either resolution functions or functions that appear in a port map are ignored.

Related Topics

- bd
- disablebp
- enablebp
- Modifying File-Line Breakpoints
- onbreak
- when
cd

This command changes the ModelSim local directory to the specified directory.
This command cannot be executed while a simulation is in progress. Also, executing a cd command will close the current project.

Syntax

cd [<dir>]

Arguments

- <dir>
  (optional) Specifies a full or relative directory path for QuestaSim to use as the local directory. If you do not specify a directory, the command changes to your home directory.
change

This command modifies the value of a:

- VHDL constant, generic, or variable
- Verilog register or variable

Syntax

change <variable> <value>

Arguments

- <variable>

(required) A string that specifies the name of an object. The name can be a full hierarchical name or a relative name, where a relative name is relative to the current environment.

Wildcards are not permitted.

The following sections list supported objects:

- VHDL
  - Scalar variable, constant, or generics of all types except FILE.
    
    Generates a warning when changing a VHDL constant or generic. You can suppress this warning by setting the TCL variable WarnConstantChange to 0 or in the [vsim] section of the modelsim.ini file.
  - Scalar subelement of composite variable, constant, and generic of all types except FILE.
  - One-dimensional array of enumerated character types, including slices.
  - Access type. An access type pointer can be set to "null"; the value that an access type points to can be changed as specified above.

- Verilog
  - Parameter.
  - Register or memory.
  - Integer, real, realtime, time, and local variables in tasks and functions.
  - Subelements of register, integer, real, realtime, and time multi-dimensional arrays (all dimensions must be specified).
  - Bit-selects and part-selects of the above except for objects whose basic type is real.

The name can be a full hierarchical name or a relative name. A relative name is relative to the current environment. Wildcards cannot be used.
Commands

**change**

- `<value>`
  
  (required) Defines a value for `<variable>`. The specified value must be appropriate for the type of the variable. You must place `<value>` within quotation marks (" ") or curly braces ({ }) if it contains spaces.

  **Note**
  
  The initial type of `<variable>` determines the type of value that it can be given. For example, if `<variable>` is initially equal to 3.14 then only real values can be set on it. Also note that changing the value of a parameter or generic will not modify any design elements that depended on the parameter or generic during elaboration (for example, sizes of arrays).

**Examples**

- Change the value of the variable `count` to the hexadecimal value FFFF.
  
  `change count 16#FFFF`

- Change the value of the element of `rega` that is specified by the index (i.e., 16).
  
  `change {rega[16]} 0`

- Change the value of the set of elements of `foo` that is specified by the slice (i.e., 20:22).
  
  `change {foo[20:22]} 011`

- Set the Verilog register `file_name` to "test2.txt". Note that the quote marks are escaped with '\'.
  
  `change file_name "test2.txt"`

- Set the time value of the `mytimegeneric` variable to 500 ps. The time value is enclosed by curly braces (or quotation marks) because of the space between the value and the units.
  
  `change mytimegeneric {500 ps}`

**Related Topics**

- `force`
configure

The `configure` command invokes the List or Wave widget configure command for the current default List or Wave window.

To change the default window, use the `view` command.

Some arguments to this command are order-dependent. Please read through the arguments for further information.

Syntax

```
configure list | wave [<option> <value>]
```

---- List Window Arguments

[-delta [all | collapse | events | none]] [-gateduration [<duration_open>]]
[-gateexpr [<expression>]] [-usegating [off | on]] [-strobeperiod [<period>[<unit>]]]
[-strobefirst [<start_time>[<unit>]]] [-usesignaltriggers [0 | 1]] [-usestrobe [0 | 1]]

---- Wave Window Arguments

[-childrowmargin [<pixels>]] [-cursorlockcolor [<color>]] [-gridauto [off | on]]
[-gridcolor [<color>]] [-griddelta [<pixels>]] [-gridoffset [<time>[<unit>]]]
[-gridperiod [<time>[<unit>]]] [-namecolwidth [<width>]] [-rowmargin [<pixels>]]
[-signalnamewidth [<value>]] [-timecolor [<color>]] [-timeline [0 | 1]]
[-timelineunits [fs | ps | ns | us | ms | sec | min | hr]] [-valuecolwidth [<width>]]
[-vectorcolor [<color>]] [-waveselectcolor [<color>]] [-waveselectenable [0 | 1]]

Description

The command works in three modes:

- without options or values it returns a list of all attributes and their current values
- with just an option argument (without a value) it returns the current value of that attribute
- with one or more option-value pairs it changes the values of the specified attributes to the new values

The returned information has five fields for each attribute: the command-line switch, the Tk widget resource name, the Tk class name, the default value, and the current value.

Arguments

- list | wave

(required) Controls the widget to configure. Must be specified as the first argument to the `configure` command.

- list — Specifies the List widget.
- wave — Specifies the Wave widget.
configure

- <option> <value>
  -bg <color> — (optional) Specifies the window background color.
  -fg <color> — (optional) Specifies the window foreground color.
  -selectbackground <color> — (optional) Specifies the window background color when selected.
  -selectforeground <color> — (optional) Specifies the window foreground color when selected.
  -font <font> — (optional) Specifies the font used in the widget.
  -height <pixels> — (optional) Specifies the height in pixels of each row.

Arguments, List window only

- -delta [all | collapse | events | none] (optional) Specifies how information is displayed in the delta column. To use -delta, -usesignaltriggers must be set to 1 (on).
  all — Displays a new line for each time step on which objects change.
  collapse — Displays the final value for each time step.
  events — Displays an "event" column rather than a "delta" column and sorts List window data by event.
  none — Turns off the display of the delta column.

- -gateduration [<duration_open>] (optional) Extends gating beyond the back edge (the last list row in which the expression evaluates to true). The duration for gating to remain open beyond when -gateexpr (below) becomes false, expressed in x number of timescale units. The default value for normal synchronous gating is zero. If -gateduration is set to a non-zero value, a simulation value will be displayed after the gate expression becomes false (if you don’t want the values displayed, set -gateduration to zero).
  <duration_open> — Any non-negative integer where the default is 0 (values are not displayed).

- -gateexpr [<expression>] (optional) Specifies the expression for trigger gating. (Use the -usegating argument to enable trigger gating.) The expression is evaluated when the List window would normally have displayed a row of data.
  <expression> — An expression.

- -usegating [off | on] (optional) Enables triggers to be gated on or off by an overriding expression. (Use the -gateexpr argument to specify the expression.) Refer to “Using Gating Expressions to Control Triggering” for additional information on using gating with triggers.
  off — (default) Triggers are gated off (a value of 0).
on — Triggers are gated on (a value of 1).

- strobeperiod [<period>[<unit>]]
  (optional) Specifies the period of the list strobe.
  <period> — Any non-negative integer.
  <unit> — (optional) A suffix specifying a unit of time where the default is to specify the
           current simulation resolution by omitting <unit>. Valid time units are: fs, ps, ns, us,
           ms, sec, min, and hr. If <unit> is specified, you must enclose <delay> and <unit>
           within curly braces ({ }).

- strobestart [<start_time>[<unit>]]
  (optional) Specifies the start time of the list strobe.
  <start_time> — Any non-negative integer.
  <unit> — (optional) A suffix specifying a unit of time where the default is to specify the
           current simulation resolution by omitting <unit>. Valid time units are: fs, ps, ns, us,
           ms, sec, min, and hr. If <unit> is specified, you must enclose <delay> and <unit>
           within curly braces ({ }).

- usesignaltriggers [0 | 1]
  (optional) Specifies whether or not signals are to be used as triggers.
  0 — Signals are not used as triggers
  1 — Signals are used as triggers

- usestrobe [0 | 1]
  (optional) Specifies whether or not a strobe is used as a trigger.
  0 — Strobe is not used to trigger.
  1 — Strobe is used to trigger.

Arguments, Wave window only

- childrowmargin [<pixels>]
  (optional) Specifies the distance in pixels between child signals. Related Tcl variable is
  PrefWave(childRowMargin).
  <pixels> — Any non-negative integer where the default is 2.

- cursorlockcolor [<color>]
  (optional) Specifies the color of a locked cursor. Related Tcl variable is
  PrefWave(cursorLockColor).
  <color> — Any Tcl color where the default is red.

- gridauto [off | on]
  (optional) Controls the grid period when in simulation time mode.
  off — (default) user-specified grid period is used.
on — grid period is determined by the major tick marks in the time line.

- -gridcolor [<color>]
  (optional) Specifies the background grid color. Related Tcl variable is PrefWave(gridColor).
  
    <color> — Any color where the default is grey50.

- -griddelta [<pixels>]
  (optional) Specifies the closest (in pixels) two grid lines can be drawn before intermediate lines will be removed. Related Tcl variable is PrefWave(gridDelta).
  
    <pixels> — Any non-negative integer where the default is 40.

- -gridoffset [<time>[<unit>]]
  (optional) Specifies the time (in user time units) of the first grid line. Related Tcl variable is PrefWave(gridOffset).
  
    <time> — Any non-negative integer where the default is 0.
    <unit> — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting <unit>. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr. If <unit> is specified, you must enclose <delay> and <unit> within curly braces ({}).

- -gridperiod [<time>[<unit>]]
  (optional) Specifies the time (in user time units) between subsequent grid lines. Related Tcl variable is PrefWave(gridPeriod).
  
    <time> — Any non-negative integer where the default is 1.
    <unit> — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting <unit>. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr. If <unit> is specified, you must enclose <delay> and <unit> within curly braces ({}).

- -namecolwidth [<width>]
  (optional) Specifies the width of the name column in pixels. Related Tcl variable is PrefWave(nameColWidth).
  
    <width> — Any non-negative integer where the default is 150.

- -rowmargin [<pixels>]
  (optional) Specifies the distance between top-level signals in pixels. Related Tcl variable is PrefWave(rowMargin).
  
    <pixels> — Any non-negative integer where the default is 4.

- -signalnamewidth [<value>]
  (optional) Controls the number of hierarchical regions displayed as part of a signal name shown in the pathname pane. Related Tcl variable is PrefWave(SignalNameWidth). Can also be set with the WaveSignalNameWidth variable in the modelsim.ini file.
<value> — Any non-negative integer where the default is 0 (display the full path. For example, 1 displays only the leaf path element, 2 displays the last two path elements, and so on.

- `timecolor [<color>]`
  (optional) Specifies the time axis color. Related Tcl variable is `PrefWave(timeColor)`.
  
  `<color>` — Any color where the default is green.

- `timeline [0 | 1]`
  (optional) Specifies whether the horizontal axis displays simulation time or grid period count. Related Tcl variable is `PrefWave(timeline)`.
  
  0 — (default) Simulation time is displayed.
  1 — Grid period count is displayed.

- `timelineunits [fs | ps | ns | us | ms | sec | min | hr]`
  (optional) Specifies units for timeline display. Does not affect the currently-defined simulation time.
  
  fs — femtosecond (10^-15 seconds)
  ps — picosecond (10^-12 seconds)
  ns — nanosecond (10^-9 seconds) (default)
  us — microsecond (10^-6 seconds)
  ms — millisecond (10^-3 seconds)
  sec — second
  min — minute (60 seconds)
  hr — hour (3600 seconds)

- `valuecolwidth [<width>]`
  (optional) Specifies the width of the value column, in pixels. Related Tcl variable is `PrefWave(valueColWidth)`.
  
  `<width>` — Any non-negative integer where the default is 100.

- `vectorcolor [<color>]`
  (optional) Specifies the vector waveform color. Default is #b3ffb3. Related Tcl variable is `PrefWave(vectorColor)`.
  
  `<color>` — Any color where the default is #b3ffb3.

- `waveselectcolor [<color>]`
  (optional) Specifies the background highlight color of a selected waveform. Related Tcl variable is `PrefWave(waveSelectColor)`.
  
  `<color>` — Any color where the default is grey30.
- waveselectenable [0 | 1]
  (optional) Specifies whether the waveform background highlights when an object is selected. Related Tcl variable is PrefWave(waveSelectEnabled).
  
  0 — (default) Highlighting is disabled.
  1 — Highlighting is enabled.

There are more options than are listed here. See the output of a configure list or configure wave command for all options.

Examples

- Display the current value of the strobeperiod attribute.
  
  `config list -strobeperiod`

- Set the period of the list strobe and turns it on.

  `config list -strobeperiod (50 ns) -strobestart 0 -usestrobe 1`

- Set the wave vector color to blue.

  `config wave -vectorcolor blue`

- Set the display in the current Wave window to show only the leaf path of each signal.

  `config wave -signalnamewidth 1`

Related Topics

- `view`
- Simulator GUI Preferences
**dataset alias**

This command assigns an additional name (alias) to a dataset. The dataset can then be referenced by that alias. A dataset can have any number of aliases, but all dataset names and aliases must be unique.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

**Syntax**

dataset alias `<dataset_name>` [`<alias_name>`]

**Arguments**

- `<dataset_name>`
  (required) Specifies the name of the dataset to which the alias is assigned. Use the root name of the file only. Must be specified as the first argument to the `dataset alias` command.

- `<alias_name>`
  (optional) Specifies the alias name to assign to the dataset. Returns a list of all aliases currently assigned to the specified dataset.

**Examples**

Assign the alias name “bar” to the dataset named “gold.”

```
dataset alias gold bar
```

**Related Topics**

- `dataset clear`
- `dataset close`
- `dataset config`
- `dataset info`
- `dataset list`
- `dataset open`
- `dataset rename`
- `dataset restart`
- `dataset save`
- `dataset snapshot`
dataset clear

This command applies only to WLF based simulation datasets. It has no effect on coverage (UCDB) datasets. All event data is removed from the current simulation WLF file, while retaining all currently logged signals. Subsequent run commands will continue to accumulate data in the WLF file.

If the command is executed when no design is loaded then the error: “Dataset not found: sim” is returned. If the command is executed when a design is loaded, then the “sim:” dataset is cleared, irrespective of which dataset is currently set. Clearing the dataset will clear any open wave window based on the “sim:”.

Syntax

dataset clear

Examples

Clear data in the WLF file from time 0ns to 100000ns, then log data into the WLF file from time 100000ns to 200000ns.

```
add wave *
run 100000ns
dataset clear
run 100000ns
```

Related Topics

- dataset alias
- dataset close
- dataset config
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset restart
- dataset save
- dataset snapshot
- log
- Recording Simulation Results With Datasets
**dataset close**

This command closes an active dataset. To open a dataset, use the `dataset open` command.

**Syntax**

```text
dataset close {<dataset_name> | -all}
```

**Arguments**

- `<dataset_name> | -all`
  - (required) Closes dataset(s).
  - `<dataset_name>` — Specifies the name of the dataset or alias you wish to close.
  - `-all` — Closes all open datasets and the simulation.

**Related Topics**

- `dataset alias`
- `dataset clear`
- `dataset config`
- `dataset info`
- `dataset list`
- `dataset open`
- `dataset rename`
- `dataset restart`
- `dataset save`
- `dataset snapshot`
**dataset config**

This command configures WLF file parameters after a WLF file has already been opened. It has no effect on coverage datasets (UCDB).

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

**Syntax**

```
dataset config <dataset_name> [-wlfcachesize [<n>]] [-wlfdeleteonquit [0 | 1]] [-wlfopt [0 | 1]]
```

**Arguments**

- **<dataset_name>** (required) Specifies the logical name of the dataset or alias you wish to configure. Must be specified as the first argument to the `dataset config` command.
- **-wlfcachesize [<n>]** (optional) Sets the size, in megabytes, of the WLF reader cache. Does not affect the WLF write cache.
  
  `<n>` — Any non-negative integer, in MB where the default is 256.

  If you do not specify a value for `<n>`, this switch returns the size, in megabytes, of the WLF reader cache.
- **-wlfdeleteonquit [0 | 1]** (optional) Deletes the WLF file automatically when the simulation exits. Valid for the current simulation dataset only.
  
  0 — Disabled (default)
  
  1 — Enabled

  If you do not specify an argument, this switch returns the current setting for the switch.
- **-wlfopt [0 | 1]** (optional) Optimizes the display of waveforms in the Wave window.
  
  0 — Disabled
  
  1 — Enabled (default)

  If you do not specify an argument, this switch returns the current setting for the switch.

**Examples**

Set the size of the WLF reader cache for the dataset “gold” to 512 MB.

```
dataset config gold -wlfcachesize 512
```
Related Topics

- dataset alias
- dataset clear
- dataset close
- dataset config
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset restart
- dataset save
- dataset snapshot
- WLF File Parameter Overview
- vsim
**dataset current**

This command opens the specified dataset and sets the GUI context to the last selected context of the specified dataset. All context dependent GUI data is updated and all context dependent CLI commands start working with respect to the new context.

**Syntax**

dataset current [<dataset_name>]

**Arguments**

- <dataset_name>

  (optional) Specifies the logical name of the dataset or alias you wish to display. If no dataset name is specified, the command returns the name of the currently displayed dataset.

**Related Topics**

- dataset alias
- dataset clear
- dataset close
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset restart
- dataset save
- dataset snapshot
- WLF File Parameter Overview
- vsim
dataset info

This command reports a variety of information about a dataset.
Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

dataset info {name | file | exists} <dataset_name>

Arguments

• {name | file | exists}  
  (required) Identifies what type of information you want reported.
  Only one option per command is allowed. The current options include:
  name — Returns the actual name of the dataset. Useful for identifying the real dataset name of an alias.
  file — Returns the name of the WLF file or UCDB file associated with the dataset.
  exists — Returns "1" if the dataset exists, "0" if it does not.
  Must be specified as the first argument to the dataset info command.

• <dataset_name>
  (optional) Specifies the name of the dataset or alias for which you want information. If you do not specify a dataset name, ModelSim uses the dataset of the current environment.

Related Topics

• dataset alias
• dataset clear
• dataset close
• dataset config
• dataset list
• dataset open
• dataset rename
• dataset restart
• dataset save
• dataset snapshot
• environment
dataset list

This command lists all active datasets.

Syntax

dataset list [-long]

Arguments

- -long
  (optional) Lists the filename corresponding to the logical name of each dataset.

Related Topics

- dataset alias
- dataset clear
- dataset close
- dataset config
- dataset info
- dataset open
- dataset rename
- dataset restart
- dataset save
- dataset snapshot
dataset open

This command opens a WLF file (representing a prior simulation) and/or UCDB file (representing coverage data) and assigns it the logical name that you specify. To close a dataset, use `dataset close`.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

dataset open `<file_name>` [ `<logical_name>` ]

Arguments

- `<file_name>`
  
  (required) Specifies the WLF file or UCDB file to open as a view-mode dataset. Must be specified as the first argument to the `dataset open` command.

- `<logical_name>`
  
  (optional) Specifies the logical name for the dataset. This is a prefix that will identify the dataset in the current session. By default the dataset prefix will be the name of the specified WLF or UCDB file.

Examples

Open the dataset file `last.wlf` and assign it the logical name `test`.

```bash
dataset open last.wlf test
```

Related Topics

- `dataset alias`
- `dataset clear`
- `dataset close`
- `dataset config`
- `dataset info`
- `dataset list`
- `dataset rename`
- `dataset restart`
- `dataset save`
- `dataset snapshot`
- `vsim -view` option
dataset rename

This command changes the logical name of a dataset to the new name you specify.
Arguments to this command are order dependent. Follow the order specified in the Syntax section.

Syntax

dataset rename <logical_name> <new_logical_name>

Arguments

• <logical_name>
  Specifies the existing logical name of the dataset.
• <new_logical_name>
  Specifies the new logical name for the dataset.

Examples

Rename the dataset file "test" to "test2".

dataset rename test test2

Related Topics

• dataset alias
• dataset clear
• dataset close
• dataset config
• dataset info
• dataset list
• dataset open
• dataset restart
• dataset save
• dataset snapshot
dataset restart

This command unloads the specified dataset or current dataset and reloads the file using the same pathname. The contents of Wave and other coverage windows are restored for UCDB datasets after a reload.

**Syntax**

dataset restart [<file_name>]

**Arguments**

- `<file_name>`

  (optional) Specifies the WLF or UCDB file to open as a view-mode or coverage mode dataset. If `<filename>` is not specified, the current dataset is restarted.

**Related Topics**

- dataset alias
- dataset clear
- dataset close
- dataset config
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset save
- dataset snapshot
Commands
dataset save

dataset save
This command writes data from the current simulation to the specified file. This lets you save simulation data while the simulation is still in progress.
Arguments to this command are order dependent. Follow the order specified in the Syntax section.

Syntax
dataset save <dataset_name> <file_name>

Arguments
- <dataset_name>
  (required) Specifies the name of the dataset you want to save.
- <file_name>
  (required) Specifies the name of the file to save.

Examples
Save all current log data in the sim dataset to the file gold.wlf.

    dataset save sim gold.wlf

Related Topics
- dataset alias
- dataset clear
- dataset close
- dataset config
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset restart
- dataset snapshot
dataset snapshot

This command saves data from the current WLF file (vsim.wlf by default) at a specified interval. It provides you with sequential or cumulative "snapshots" of your simulation data. This command does not apply to coverage datasets (UCDB).

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

dataset snapshot [-dir <directory>] [-disable] [-enable] [-file <file_name>]
[-filemode {overwrite | increment}] [-mode {cumulative | sequential}] [-report] [-reset]
{-size <file_size> | -time <n> [<unit>]}

Arguments

• -dir <directory>
  (optional) Specifies a directory into which the files should be saved. Either absolute or relative paths may be used. Default is to save to the current working directory.

• -disable
  (optional) Turns snapshotting off. All dataset snapshot settings from the current simulation are stored in memory. All other options are ignored after you specify -disable.

• -enable
  (optional) Turns snapshotting on. Restores dataset snapshot settings from memory or from a saved dataset. (default)

• -file <file_name>
  (optional) Specifies the name of the file to save snapshot data.
  <file_name> — A specified file name where the default is vsim_snapshot.wlf. .wlf will be appended to specified filename and, possibly, an incrementing suffix.

When the duration of the simulation run is not a multiple of the interval specified by -size or -time, the incomplete portion is saved in the file vsim.wlf.

• -filemode {overwrite | increment}
  (optional) Specifies whether to overwrite the snapshot file each time a snapshot occurs.
  overwrite — (default)
  increment — A new file is created for each snapshot. An incrementing suffix (1 to n) is added to each new file (for example, vsim_snapshot_1.wlf).

• -mode {cumulative | sequential}
  (optional) Specifies whether to keep all data from the time signals are first logged.
  cumulative — (default)
  sequential — The current WLF file is cleared every time a snapshot is taken.
Commands

**dataset snapshot**

- **-report**
  (optional) Lists current snapshot settings in the Transcript window. All other options are ignored if you specify -report.

- **-reset**
  (optional) Resets values back to defaults. The behavior is to reset to the default, then apply the remainder of the arguments on the command line. See examples below. If specified by itself without any other arguments, -reset disables dataset snapshot and resets the values.

- **-size <file_size>**
  (Required if -time is not specified.) Specifies that a snapshot occurs based on WLF file size. Must be specified as the final argument to the `dataset snapshot` command.

  `<file_size>` — Size of WLF file in MB.

- **-time <n> [<unit>]**
  (Required if -size is not specified.) Specifies that a snapshot occurs based on simulation time. Must be specified as the final argument to the `dataset snapshot` command.

  `<n>` — Any positive integer.

  `<unit>` — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting `<unit>`. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr. If `<unit>` is specified, you must enclose `<limit>` and `<unit>` within curly braces ({}).

**Examples**

- Create the file `vsim_snapshot_<n>.wlf` that is written to every time the current WLF file reaches a multiple of 10 MB (i.e., at 10 MB, 20 MB, 30 MB, etc.).

  `dataset snapshot -size 10`

- Similar to the previous example, but in this case the current WLF file is cleared every time it reaches 10 MB.

  `dataset snapshot -size 10 -mode sequential`

- Assuming simulator time units are ps, this command saves a file called `gold_<n>.wlf` every 1000000 ps. If you run the simulation for 3000000 ps, three files are saved: `gold_1.wlf` with data from 0 to 1000000 ps, `gold_2.wlf` with data from 1000001 to 2000000, and `gold_3.wlf` with data from 2000001 to 3000000.

  `dataset snapshot -time 1000000 -file gold.wlf -mode sequential -filemode increment`

  Because this example sets the time interval to 1000000 ps, if you run the simulation for 3500000 ps, a file containing the data from 3000001 to 3500000 ps is saved as `vsim.wlf` (default).

- Enable snapshotting with time=10000 and default mode (cumulative) and default filemode (overwrite).
dataset snapshot -reset -time 10000

Related Topics

• dataset alias
• dataset clear
• dataset close
• dataset config
• dataset info
• dataset list
• dataset open
• dataset rename
• dataset restart
• dataset save
delete

This command removes objects from either the List or Wave window. Arguments to this command are order dependent.

Syntax

delete list [-window <wname>] <object_name>
delete wave [-window <wname>] <object_name>

Arguments

- list
  Specifies the target is a list window.
- wave
  Specifies the target is a wave window.
- -window <wname>
  (optional) Specifies the name of the List or Wave window to target for the delete command. (The view command allows you to create more than one List or Wave window.) If no window is specified, the default window is used; the default window is determined by the most recent invocation of the view command.
- <object_name>...
  (required) Specifies the name of an object. Must match an object name used in an add list or add wave command. Multiple object names are specified as a space separated list. Wildcard characters are allowed. Must be specified as the final argument to the delete list and delete wave commands.

Examples

- Remove the object vec2 from the list2 window.

  delete list -window list2 vec2

- Remove all objects beginning with the string /test from the Wave window.

  delete wave /test*

Related Topics

- add list
- add wave
- Wildcard Characters
describe

This command displays information about the following types of simulation objects and design regions in the Transcript window:

- **VHDL** — signals, variables, and constants
- **Verilog** — nets and registers
- **Design region**

VHDL signals Verilog nets and registers can be specified as hierarchical names.

**Syntax**

describe <name>...

**Arguments**

- <name>...
  
  (required) The name of an HDL object for which you want a description. Multiple object names are specified as a space separated list. Wildcard characters are allowed. HDL object names can be relative or full hierarchical names.

**Examples**

- Print the types of the three specified signals.

  
  describe clk prw prdy

**Related Topics**

- add list
- add wave
- Wildcard Characters
disablebp

This command turns off breakpoints and when commands. To turn on breakpoints or when commands again, use the enablebp command.

Syntax

disablebp [<id#> | <label>]

Arguments

- <id#>
  (optional) Specifies the ID number of a breakpoint or when statement to disable.
- <label>
  (optional) Specifies the label name of a breakpoint or when statement to disable.

If you do not specify either of these arguments, all breakpoints and when statements are disabled.

Use the bp command with no arguments to find labels and ID numbers for all breakpoints in the current simulation. Use the when command with no arguments to find labels and ID numbers of all when statements in the current simulation.

Note

Id numbers for breakpoints and when statements are assigned from the same pool. Even if you have not specified a given id number for a breakpoint, that number may still be used for a when command.

Related Topics

- bd
- bp
- enablebp
- onbreak
- resume
- when
do

This command executes the commands contained in a macro file.

A macro file can have any name and extension. An error encountered during the execution of a macro file causes its execution to be interrupted, unless an onerror command, onbreak command, or the OnErrorDefaultAction Tcl variable has specified with the resume command.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

do <filename> [parameter_value>...]

Arguments

- <filename>
  (required) Specifies the name of the macro file to be executed. The name can be a pathname or a relative file name. Pathnames are relative to the current working directory. Must be specified as the first argument to the do command.

  If the do command is executed from another macro file, pathnames are relative to the directory of the calling macro file. This allows groups of macro files to be stored in a separate sub-directory.

- <parameter_value>...
  (optional) Specifies values that are to be passed to the corresponding parameters $1 through $9 in the macro file. Multiple parameter values must be separated by spaces.

  If you want to make the parameters optional (for example, specify fewer parameter values than the number of parameters actually used in the macro), you must use the argc simulator state variable in the macro. Refer to “Making Macro Parameters Optional”.

Note

While there is no limit on the number of parameters that can be passed to macros, only nine values are visible at one time. Use the shift command to see the other parameters.

Examples

- Execute the file macros/stimulus and pass the parameter value 100 to $1 in the macro file.

  do macros/stimulus 100

- Where the macro file testfile contains the line

  bp $1 $2

  place a breakpoint in the source file named design.vhd at line 127.
Commands

do

do testfile design.vhd 127

Related Topics

- Tcl and Macros (DO Files)
- Modes of Operation
- Using a Startup File
- DOPATH variable
drivers

This command displays the names and strength of all drivers of the specified object.

The driver list is expressed relative to the top-most design signal/net connected to the specified object. If the object is a record or array, each sub-element is displayed individually.

Syntax

drivers <object_name>

Arguments

• <object_name>  
  (required) Specifies the name of the signal or net whose drivers are to be shown. All signal or net types are valid. Multiple names and wildcards are accepted.

Example

  drivers /top/dut/pkt_cnt(4)

    # Drivers for /top/dut/pkt_cnt(4):
    #       St0  : Net /top/dut/pkt_cnt[4]
    #       St0  : Driver /top/dut/pkt_counter/#IMPLICIT-WIRE(cnt_out)#6

In some cases, the output may supply a strength value similar to 630 or 52x, which indicates an ambiguous verilog strength.

Related Topics

• readers
• Verilog LRM Std 1365-2005 section 7.10.2 "Ambiguous strengths: sources and combinations"
dumplog64

This command dumps the contents of the specified WLF file in a readable format to stdout. The WLF file cannot be opened for writing in a simulation when you use this command. This command cannot be used in a DO file.

Syntax

dumplog64 <filename>

Arguments

- <filename>
  (required) The name of the WLF file to be read.
**echo**

This command displays a specified message in the Transcript window.

**Syntax**

```
echo [<text_string>]
```

**Arguments**

- `<text_string>`
  
  (required) Specifies the message text to be displayed. If the text string is surrounded by quotes, blank spaces are displayed as entered. If quotes are omitted, two or more adjacent blank spaces are compressed into one space.

**Examples**

- If the current time is 1000 ns, this command:
  ```
echo "The time is $now ns."
  ```
  returns the message:
  
  ```
The time is 1000 ns.
  ```

- If the quotes are omitted:
  ```
echo The time is $now ns.
  ```
  all blank spaces of two or more are compressed into one space.
  
  ```
The time is $now ns."
  ```

- echo can also use command substitution, such as:
  ```
echo The hex value of counter is [examine -hex counter].
  ```
  If the current value of counter is 21 (15 hex), this command returns:
  
  ```
The hex value of counter is 15.
  ```
edit

This command invokes the editor specified by the EDITOR environment variable. By default, the specified filename will open in the Source window.

Syntax
edit [<filename>]

Arguments
• <filename>
  (optional) Specifies the name of the file to edit. If the <filename> argument is omitted, the editor opens the current source file. If you specify a non-existent filename, it will open a new file. Either absolute or relative paths may be used.

Related Topics
• notepad
• EDITOR environment variable
enablebp

This command turns on breakpoints and when commands that were previously disabled.

Syntax

enablebp [<id#> | <label>]

Arguments

• <id#>

  (optional) Specifies a breakpoint ID number or when statement to enable.

• <label>

  (optional) Specifies the label name of a breakpoint or when statement to enable.

If you do not specify either of these arguments, all breakpoints are enabled.

Use the bp command with no arguments to find labels and ID numbers for all breakpoints in the current simulation. Use the when command with no arguments to find labels and ID numbers of all when statements in the current simulation.

Related Topics

• bd
• bp
• disablebp
• onbreak
• resume
• when
encoding

This command translates between the 16-bit Unicode characters used in Tcl strings and a named encoding, such as Shift-JIS. There are four encoding commands used to work with the encoding of your character representations in the GUI.

- encoding convertfrom — Convert a string from the named encoding to Unicode.
- encoding convertto — Convert a string to the named encoding from Unicode.
- encoding names — Returns a list of all valid encoding names.
- encoding system — Changes the current system encoding to a named encoding. If a new encoding is omitted the command returns the current system encoding. The system encoding is used whenever Tcl passes strings to system calls.

Syntax

encoding convertfrom <encoding_name> <string>
encoding convertto <encoding_name> <string>
encoding names
encoding system <encoding_name>

Arguments

- string — Specifies a string to be converted.
- encoding_name — The name of the encoding to use.
environment

This command has two forms, environment and env. It allows you to display or change the current dataset and region/signal environment.

Syntax

environment [-dataset | -nodataset] [<pathname> | -forward | -back]

Arguments

- -dataset
  (optional) Displays the specified environment pathname with a dataset prefix. Dataset prefixes are displayed by default.
- -nodataset
  (optional) Displays the specified environment pathname without a dataset prefix.
- <pathname>
  (optional) Specifies a new pathname for the region/signal environment.
  If omitted the command causes the pathname of the current region/signal environment to be displayed.
- -forward
  (optional) Displays the next environment in your history of visited environments.
- -back
  (optional) Displays the previous environment in your history of visited environments.

Examples

- Display the pathname of the current region/signal environment.
  env
- Change to another dataset but retain the currently selected context.
  env test:
- Change all unlocked windows to the context "test:/top/foo".
  env test:/top/foo
- Move down two levels in the design hierarchy.
  env blk1/u2
- Move to the top level of the design hierarchy.
  env /
Related Topics

- See Object Name Syntax for information on specifying pathnames.
- See Setting your Context by Navigating Source Files for more information about -forward and -back.
examine

This command has two forms, examine and exa. It examines one or more objects and displays current values (or the values at a specified previous time) in the Transcript window.

It can also compute the value of an expression of one or more objects.

The following objects can be examined:

- **VHDL** — signals, shared variables, process variables, constants, and generics
- **Verilog** — nets, registers, parameters, and variables

To display a previous value, specify the desired time using the -time option.

To compute an expression, use the -expr option. The -expr and the -time options may be used together.

Virtual signals and functions may also be examined within the GUI (actual signals are examined in the kernel).

The following rules are used by the examine command to locate an HDL object:

- If the name does not include a dataset name, then the current dataset is used.
- If the name does not start with a path separator, then the current context is used.
- If the name is a path separator followed by a name that is not the name of a top-level design unit, then the first top-level design unit in the design is used.
- For a relative name containing a hierarchical path, if the first object name cannot be found in the current context, then an upward search is done up to the top of the design hierarchy to look for a matching object name.
- If no objects of the specified name can be found in the specified context, then an upward search is done to look for a matching object in any visible enclosing scope up to an instance boundary. If at least one match is found within a given context, no (more) upward searching is done; therefore, some objects that may be visible from a given context will not be found when wildcards are used if they are within a higher enclosing scope.
- The wildcards '*' and '?' can be used at any level of a name except in the dataset name and inside of a slice specification.
- A wildcard character will never match a path separator. For example, /dut/* will match /dut/siga and /dut/clk. However, /dut* won’t match either of those.

See Design Object Names for more information on specifying names.

**Syntax**

```bash
[-internal] [-maxlen <integer>] [-expr <expression>] [-name] [-<radix_type>]
[-radix <type>] [-radixenumnumeric] [-radixenumsymbolic] [-time <time>] [-value]
```
Arguments

- `<name>`…
  (required except when specifying -expr.) Specifies the name of any HDL object.
  All object types are allowed, except those of the type file. Multiple names and wildcards are accepted. Spaces, square brackets, and extended identifiers require curly braces; see examples below for more details. To examine a VHDL variable you can add a process label to the name. For example, (make certain to use two underscore characters):

  `exa line__36/i`

- `-delta <delta>`
  (optional) Specifies a simulation cycle at the specified time step from which to fetch the value where the default is to use the last delta of the time step. You must log the objects to be examined using the `add list`, `add wave`, or `log` command for the examine command to be able return a value for a requested delta.

  `<delta>` — Any non-negative integer.

- `-env <path>`
  (optional) Specifies a path in which to look for an object name.

  `<path>` — The specified path to a object.

- `-expr <expression>`
  (optional) Specifies an expression to be examined. You must log the expression using the `add list`, `add wave`, or `log` command for the examine command to return a value for a specified expression. The expression is evaluated at the current time simulation. If you also specify the -time argument, the expression will be evaluated at the specified time. It is not necessary to specify `<name>` when using this argument. See `GUI_expression_format` for the format of the expression.

  `<expression>` — Specifies an expression enclosed in braces ({}).

- `-handle`
  (optional) Returns the memory address of the specified `<name>`. You can use this value as a tag when analyzing the simulation. This value also appears as the title of a box in the Watch window. This option will not return any value if you are in -view mode.

- `-in`
  (optional) Specifies that `<name>` include ports of mode IN.

- `-out`
  (optional) Specifies that `<name>` include ports of mode OUT.

- `-inout`
  (optional) Specifies that `<name>` include ports of mode INOUT.
-internal
(optional) Specifies that <name> include internal (non-port) signals.

-maxlen <integer>
(optional) Specifies the maximum number of characters in the output of the command.

  <integer> — Any non-negative integer where 0 is unlimited.

-ports
(optional) Specifies that <name> include all ports. Has the same effect as specifying -in, -inout, and -out together.

-name
(optional) Displays object name(s) and value(s). Related switch is -value.

-<radix_type>
(optional) Specifies the radix type for the objects that follow in the command. Valid entries (or any unique abbreviations) are: binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

If no radix is specified for an enumerated type, the default radix is used. You can change the default radix for the current simulation using the radix command. You can change the default radix permanently by editing the DefaultRadix variable in the modelsim.ini file.

-radix <type>
(optional) Specifies a user-defined radix. The -radix <type> switch can be used in place of the -<radix_type> switch. For example, -radix hexadecimal is the same as -hex.

  <type> — binary, ascii, unsigned, decimal, octal, hex, symbolic, time, and default.

You can change the default radix for the current simulation using this radix command. You can change the default radix permanently by editing the DefaultRadix variable in the modelsim.ini file.

-radixenumnumeric
(optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

-radixenumsymbolic
(optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the -radixenumnumeric option.

-time <time>
(optional) Specifies the time value between 0 and $now for which to examine the objects.

  <time> — A non negative integer where the default unit is the current time unit. If the <time> field uses a unit other than the current unit, the value and unit must be placed in curly braces. For example, the following are equivalent for ps resolution:
  
  exa -time {3.6 ns} signal_a
  exa -time 3600 signal_a
If an expression is specified it will be evaluated at that time. The objects to be examined must be logged via the add list, add wave, or log command in order for the examine command to be able to return a value for a requested time.

- **-value**
  (default) Returns value(s) as a curly-braces separated Tcl list. Use to toggle off a previous use of -name.

**Examples**

- Return the value of `/top/bus1`.
  ```tcl```
  ```
  examine /top/bus1
  ```
  ```
  ```

- Return the value of the subelement of `rega` that is specified by the index (i.e., 16). Note that you must use curly braces when examining subelements.
  ```tcl```
  ```
  examine {rega[16]}
  ```
  ```
  ```

- Return the value of the contiguous subelements of `foo` specified by the slice (i.e., 20:22). Note the curly braces.
  ```tcl```
  ```
  examine {foo[20:22]}
  ```
  ```
  ```

- Note that when specifying an object that contains an extended identifier as the last part of the name, there must be a space after the closing `\` and before the closing `}`.
  ```tcl```
  ```
  examine {/top/My extended id\}
  ```
  ```
  ```

- In this example, the `-expr` option specifies a signal path and user-defined Tcl variable. The expression will be evaluated at 3450us.
  ```tcl```
  ```
  examine -time {3450 us} -expr {/top/bus and $bit_mask}
  ```
  ```
  ```

- Using the `${fifo}` syntax limits the variable to the simple name `fifo`, instead of interpreting the parenthesis as part of the variable. Quotes are needed when spaces are involved; and by using quotes (`"`) instead of braces, the Tcl interpreter will expand variables before calling the command.
  ```tcl```
  ```
  examine -time $t -name $fifo "${fifo}(1 to 3)" ${fifo}(1)
  ```
  ```
  ```

- Because `-time` is not specified, this expression will be evaluated at the current simulation time. Note the signal attribute and array constant specified in the expression.
  ```tcl```
  ```
  examine -expr {clk\'event && (/top/xyz == 16'hffae)}
  ```
  ```
  ```

Commands like `find` and examine return their results as a Tcl list (just a blank-separated list of strings). You can do things like:

  ```tcl```
  ```
  foreach sig [find sig ABC*] {echo "$sig is [exa $sig]" ...
  ```
  ```
  if {[examine -bin signal_12] == "11101111XXXZ"} {
  ```
  ```
  examine -hex [find *]
  ```
Related Topics

- Design Object Names
- Wildcard Characters
- DefaultRadix *modelsim.ini* variable
exit

This command exits the simulator and the ModelSim application.

If you want to stop the simulation using a when command, use a stop command within your when statement, do not use an exit command or a quit command. The stop command acts like a breakpoint at the time it is evaluated.

Syntax

exit [-force] [-code <integer>]

Argument

- -force
  (optional) Quits without asking for confirmation. If this argument is omitted, ModelSim asks you for confirmation before exiting. You can also use -f as an alias for this switch.

- -code <integer>
  (optional) Quits the simulation and issues an exit code.

  <integer> — This is the value of the exit code. You should not specify an exit code that already exists in the tool. Refer to the section "Exit Codes" in the User’s Manual for a list of existing exit codes. You can also specify a variable in place of <integer>.

  You should always print a message before executing the exit -code command to explicitly state the reason for exiting.

Examples

You can use exit -code to instruct a vmake command to exit when it encounters an assertion error. The onbreak command can specify commands to be executed upon an assert failure of sufficient severity, after which the simulator can be made to return an exit status. This is shown in the following example:

```plaintext
set broken 0
onbreak {
  set broken 88
  resume
}
run -all
if { $broken } {
  puts "failure -- exit status $broken"
  exit -code $broken
} else {
  puts "success"
}
quid -f
```

The resume command gives control back to the commands following the run -all to handle the condition appropriately.
find

This command locates objects by type and name. Arguments to the command are grouped by object type:

- Arguments for nets and signals
- Arguments for instances and blocks
- Arguments for virtuals
- Arguments for classes
- Arguments for objects

Syntax

find instances | blocks { <object_name> … | -bydu <design_unit> …} [-recursive] [-nodu]
find virtuals <object_name> … [-kind <kind>] [-unsaved] [-recursive]
find classes [<class_name>]
find objects [-class <class_name>] [-isa <class_name>] [<object_name>]

Arguments for nets and signals

When searching for nets and signals, the find command returns the full pathname of all nets, signals, registers, variables, and named events that match the name specification.

- <object_name> …
  (required) Specifies the net or signal for which you want to search. Multiple nets and signals and wildcard characters are allowed. Wildcards cannot be used inside of a slice specification. Spaces, square brackets, and extended identifiers require special syntax; see the examples below for more details.

- -in
  (optional) Specifies that the scope of the search is to include ports of mode IN.

- -inout
  (optional) Specifies that the scope of the search is to include ports of mode INOUT.

- -internal
  (optional) Specifies that the scope of the search is to include internal (non-port) objects.

- -nofilter
  (optional) Specifies that the WildcardFilter Tcl preference variable be ignored when finding signals or nets.
Commands

find

- out
  (optional) Specifies that the scope of the search is to include ports of mode OUT.

- ports
  (optional) Specifies that the scope of the search is to include all ports. Has the same effect as specifying -in, -out, and -inout together.

- recursive
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

Arguments for instances and blocks

When searching for instances, the find command returns the primary design unit name.

- bydu <design_unit> ...
  (required if <object_name> is not specified.) Searches for a design unit.

  <design_unit> ... — Name of a design unit to search for. Multiple design units and wildcard characters are allowed. This argument matches the pattern specified by <design_unit> of the instance, which must be in the form: Library.Primary[Secondary]. The Secondary name is present only for design units that have secondary names, such as VHDL. The Library name is the physical name for the library.

- <object_name> ...
  (required if -bydu is not specified.) Specifies the name of an instance or block for which you want to search. Multiple instances and wildcard characters are allowed.

- recursive
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

- nodu
  (optional) Removes the "du" string from the names of design units found with -bydu argument.

Arguments for virtuals

When searching for virtuals, all optional arguments must be specified before any object names.

- <object_name> ...
  (required) Specifies the virtual object for which you want to search. Multiple virtuals and wildcard characters are allowed.

- kind <kind>
  (optional) Specifies the kind of virtual object for which you want to search.

  <kind> — A virtual object of one of the following kinds:

  - designs
• explicits
• functions
• implicit
• signals.

-unsaved

Specifies that ModelSim find only virtuals that have not been saved to a format file.

Arguments for classes
• <class_name>
  (optional) Specifies the incrTcl class for which you want to search. Wildcard characters are allowed. The options for class_name include nets, objects, signals, and virtuals. If you do not specify a class name, the command returns all classes in the current namespace context. See incrTcl commands in the Tcl Man Pages (Help > Tcl Man Pages) for more information.

Arguments for objects
• -class <class_name>
  (optional) Restricts the search to objects whose most-specific class is class_name.
• -isa <class_name>
  (optional) Restricts the search to those objects that have class_name anywhere in their heritage.
• <object_name>
  (optional) Specifies the incrTcl object for which you want to search. Wildcard characters are allowed. If you do not specify an object name, the command returns all objects in the current namespace context. See incrTcl commands in the Tcl Man Pages (Help > Tcl Man Pages) for more information.

Description
The following rules are used by the find command to locate an object:
• If the name does not include a dataset name, then the current dataset is used.
• If the name does not start with a path separator, then the current context is used.
• If the name is a path separator followed by a name that is not the name of a top-level design unit, then the first top-level design unit in the design is used.
• For a relative name containing a hierarchical path, if the first object name cannot be found in the current context, then an upward search is done up to the top of the design hierarchy to look for a matching object name.
• If no objects of the specified name can be found in the specified context, then an upward search is done to look for a matching object in any visible enclosing scope up to an
instance boundary. If at least one match is found within a given context, no (more) upward searching is done; therefore, some objects that may be visible from a given context will not be found when wildcards are used if they are within a higher enclosing scope.

- The wildcards '*' and '?' can be used at any level of a name except in the dataset name and inside of a slice specification. Square bracket ([ ]) wildcards can also be used.

- A wildcard character will never match a path separator. For example, /dut/* will match /dut/siga and /dut/clk. However, /dut* won’t match either of those.

- Because square brackets are wildcards in the find command, only parentheses (( )) can be used to index or slice arrays.

- The WildcardFilter Tcl preference variable is used by the find command to exclude the specified types of objects when performing the search.

See Design Object Names for more information on specifying names.

**Examples**

- Find all signals in the entire design.
  
  `find signals -r /*`

- Find all input signals in region /top that begin with the letters "xy".
  
  `find nets -in /top/xy*`

- Find all signals in the design hierarchy at or below the region `<current_context>/u1/u2` whose names begin with "cl".
  
  `find signals -r u1/u2/cl*`

- Find a signal named `s1`. Note that you must enclose the object in curly braces because of the square bracket wildcard characters.
  
  `find signals {s[1]}`

- Find signals `s1`, `s2`, or `s3`.
  
  `find signals {s[123]}`

- Find the element of signal `s` that is indexed by the value 1. Note that the find command uses parentheses (( )), not square brackets ([ ]), to specify a subelement index.
  
  `find signals s(1)`

- Find a 4-bit array named `data`. Note that you must use curly braces ({ }) due to the spaces in the array slice specification.
  
  `find signals{/top/data(3 downto 0)}`

- Note that when specifying an object that contains an extended identifier as the last part of the name, there must be a space after the closing '\}' and before the closing '}'.

find signals {/top/My extended id/} 

- If /dut/core/pclk exists, prints the message "pclk does exist" in the transcript. This would typically be run in a Tcl script.

  if {[find signals /dut/core/pclk] != ""} {
    echo "pclk does exist"
  }

- Find instances based on their names using wildcards. Send search results to a text file that lists instance names, including the hierarchy path, on separate lines.

  # Search for all instances with ul in path
  set pattern_match "*ul*" ;

  # Get the list of instance paths
  set inst_list [find instances -r *] ;

  # Initialize an empty list to strip off the architecture names
  set ilist [list] ;

  foreach inst $inst_list {
    set ipath [lindex $inst 0]
    if {[string match $pattern_match $ipath]} {
      lappend ilist $ipath
    }
  }

  # At this point, ilist contains the list of instances only--
  # no architecture names
  
  # Begin sorting list
  set ilist [lsort -dictionary $ilist]

  # Open a file to write out the list
  set fhandle [open "instancelist.txt" w]
  foreach inst $ilist {
    # Print instance path, one per line
    puts $fhandle $inst
  }

  # Close the file, done.
  close $fhandle ;

Related Topics

- Design Object Names
- Wildcard Characters
find infiles

This command searches for a string in the specified file(s) and prints the results to the Transcript window. The results are individually hotlinked and will open the file and display the location of the string.

When you execute this command in command-line mode from outside of the GUI, the results are sent to stdout with no hotlinks.

Arguments to this command are order dependent. Follow the order specified in the Syntax section.

Syntax

find infiles <string_pattern> <file>...

Arguments

• <string_pattern>
  (required) The string you are searching for. You can use Tcl regular expression wildcards to further restrict the search capability.

• <file>...
  (required) The file(s) to search. You can use Tcl regular expression wildcards to further restrict the search capability.

Example

Figure 2-2 shows a screen capture containing a few examples of the find infiles command and the results.

Figure 2-1. find infiles Example
find insource

This command searches for a string in the source files for the current design and prints the results to the Transcript window. The results are hotlinked individually and will open the file and display the location of the string.

When you execute this command in command-line mode from outside of the GUI, the results are sent to stdout with no hotlinks.

Syntax

find insource <pattern> [-exact | -glob | -regex] [-inline] [-nocase]

Arguments

- <pattern>
  (required) The string you are searching for. You can use regular expression wildcards to further restrict the search. You must enclose <pattern> in quotes (") if it includes spaces. You must specify the <pattern> at the end of the command line; any switches specified after <pattern> will not be registered.

- -exact | -glob | -regex
  (optional) Defines the style of regular expression used in the <pattern>
  -exact — Indicates that no characters have special meaning, thus disabling wildcard features.
  -glob — (default) Allows glob-style wildcard characters. For more information refer to the Tcl documentation:
    Help > Tcl Man Pages
    Select “Tcl Commands”, then “string”, then “string match”
  -regex — Allows Tcl regular expressions. For more information refer to the Tcl documentation:
    Help > Tcl Man Pages
    Select “Tcl Commands”, then “re_syntax”.

- -inline
  (optional) Returns the matches in the form of a Tcl list, which disables the hotlink feature but allows for easier post-processing.

- -nocase
  (optional) Treats <pattern> as case-insensitive.

Example

Figure 2-2 shows a couple of examples of the find insource command and the results.
Figure 2-2. find insource Example

```
VSim> find insource memory
# cache.vhd:116:  -- +++++++++++++++++++ Local MRU memory +++++++++++++++++++/
# memory.vhd:12:entity memory is
# memory.vhd:21: end entity memory;
# memory.vhd:25: architecture RTL of memory is
# top.vhd:44:   component memory
# top.vhd:83:   m: memory port map(clk, saddr, sdata, srw, sstrb, srdy);
VSim> find insource "memory port"
# top.vhd:83:   m: memory port map(clk, saddr, sdata, srw, sstrb, srdy);
VSim>
```
**formatTime**

This command provides global format control for all time values displayed in the GUI. When specified without arguments, this command returns the current state of the three arguments.

**Syntax**

formatTime \[[+|-]commas\] \[[+|-]nodefunits\] \[[+|-]bestunits\]

**Arguments**

- \[[+|-]commas\] (optional) Insert commas into the time value.
  - + prefix — On
  - - prefix — Off. (default)
- \[[+|-]nodefunits\] (optional) Do not include default unit in the time.
  - + prefix — On
  - - prefix — Off. (default)
- \[[+|-]bestunits\] (optional) Use the largest unit value possible.
  - + prefix — On
  - - prefix — Off. (default)

**Examples**

- Display commas in time values.
  
  `formatTime +commas`

  Instead of displaying 6458131 ps, the GUI will display 6,458,131 ps.

- Use largest unit value possible.

  `formatTime +bestunits`

  Displays 8 us instead of 8,000 ns.
force

This command allows you to apply stimulus interactively to VHDL signals and Verilog nets. When executed without arguments, this command returns a list of the most recently applied force commands and a list of forces coming from the Signal Spy signal_force() and $signal_force() calls from within VHDL, Verilog, and SystemC source code.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

It is possible to create a complex sequence of stimuli when the force command is included in a macro file.

This command provides additional information with the -help switch.

There are a number of constraints on what you can and cannot force:

- You can force “Virtual Signals” if the number of bits corresponds to the signal value. You cannot force virtual functions.
- You can force bit-selects or an entire register, you cannot force slices of a register
- You cannot force VHDL variables. See the change command for information on working with VHDL variables.
- In VHDL and mixed models, you cannot force an input port that is mapped at a higher level. In other words, you can force the signal at the top of the hierarchy connected to the input port but you cannot force the input port directly.
- You cannot force a VHDL alias of a VHDL signal.
- You cannot force an input port that has a conversion function on the input.

Syntax

force {<object_name> <value>} [-freeze [-drive | -deposit] [-cancel [@]<time>[<unit>]] [-repeat [@]<time>[<unit>]] [[@]<time>[<unit>]]}...

Arguments

- <object_name>
  (required) Specifies the name of the HDL object to be forced. A wildcard is permitted only if it matches one object. See Design Object Names for the full syntax of an object name. The object name must specify a scalar type or a one-dimensional array of character enumeration. You may also specify a record subelement, an indexed array, or a sliced array, as long as the type is one of the above. Must be specified as the first argument to the force command.
- <value>
  (required) Specifies the value to which the object is to be forced. The specified value must be appropriate for the type. Must be specified as the second argument to the force command.
A VHDL one-dimensional array of character enumeration can be forced as a sequence of character literals or as a based number with a radix of 2, 8, 10 or 16. For example, the following values are equivalent for a signal of type bit_vector (0 to 3):

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>character literal sequence</td>
</tr>
<tr>
<td>2#1111</td>
<td>binary radix</td>
</tr>
<tr>
<td>10#15</td>
<td>decimal radix</td>
</tr>
<tr>
<td>16#F</td>
<td>hexadecimal radix</td>
</tr>
</tbody>
</table>

**Note**

For based numbers in VHDL, ModelSim translates each 1 or 0 to the appropriate value for the number’s enumerated type. The translation is controlled by the translation table in the `pref.tcl` file. If ModelSim cannot find a translation for 0 or 1, it uses the left bound of the signal type (type'left) for that value.

- **-freeze**
  (optional) Freezes the object at the specified `<value>` until it is forced again or until it is unforced with the `noforce` command.

- **-drive**
  (optional) Attaches a driver to the object and drives the specified `<value>` until the object is forced again or until it is unforced with the `noforce` command.

  This option is illegal for unresolved signals.

- **-deposit**
  (optional) Sets the object to the specified `<value>`. The `<value>` remains until the object is forced again, there is a subsequent driver transaction, or it is unforced with a `noforce` command.

  **Note**

  If the `-freeze`, `-drive`, or `-deposit` options are not used, then `-freeze` is the default for unresolved objects, and `-drive` is the default for resolved objects. If you prefer `-freeze` as the default for resolved and unresolved VHDL signals, change the `DefaultForceKind` variable in the `modelsim.ini` file.

- **-cancel [@]<time>[<unit>]**
  (optional) Cancels the force command at the specified `<time>`.

  @ — A prefix applied to `<time>` to specify an absolute time interval where the default is to specify a relative time interval by omitting the `@` character.
Commands

force

-<time> — The time (either relative or absolute) at which to cancel the force command. Any non-negative integer. A value of zero cancels the force at the end of the current time period.

-<unit> — A suffix specifying a time unit where the default is to specify the current time unit by omitting <unit>. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr.

-cancel 520 \ Relative Time
-cancel 520ns \ Relative Time

Enclose with curly braces ({}) when using spaces between the arguments. See the example below.

-cancel {@ 520 ns} \ Absolute Time

- repeat [@]<time>[<unit>]

(optional) Repeats the force command. A repeating force command will force a value before other non-repeating force commands that occur in the same time step.

-@ — A prefix applied to <time> to specify an absolute time interval where the default is to specify a relative time interval by omitting the @ character.

-<time> — The time (either relative or absolute) at which to repeat the force command. Any non-negative integer. A value of zero cancels the force at the end of the current time period. Cancellation occurs at the last simulation delta cycle of a time unit.

-<unit> — A suffix specifying a time unit where the default is to specify the current time unit by omitting <unit>. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr.

Enclose with curly braces ({}) when using spaces between the arguments.

- [@]<time>[<unit>]

(optional) Specifies the time to which the <value> is to be applied.

-@ — A prefix applied to <time> to specify an absolute time interval where the default is to specify a relative time interval by omitting the @ character.

-<time> — The time (either relative or absolute) to apply to <value>. Any non-negative integer. A value of zero cancels the force at the end of the current time period. Cancellation occurs at the last simulation delta cycle of a time unit.

-<unit> — A suffix specifying a time unit where the default is to specify the current time unit by omitting <unit>. Valid time units are: fs, ps, ns, us, ms, sec, min, and hr.

Enclose with curly braces ({}) when using spaces between the arguments.

Examples

- Force input1 to 0 at the current simulator time.

    force input1 0

- Force bus1 to 01XZ at 100 nanoseconds after the current simulator time.

    force bus1 01XZ 100 ns
• Force `bus1` to 16#F at the absolute time 200 measured in the resolution units selected at simulation start-up.

```
force bus1 16#f @200
```

• Force `input1` to 1 at 10 time units after the current simulation time and to 0 at 20 time units after the current simulation time. This cycle repeats starting at 100 time units after the current simulation time, so the next transition is to 1 at 100 time units after the current simulation time.

```
force input1 1 10, 0 20 -r 100
```

• Similar to the previous example, but also specifies the time units. Time unit expressions preceding the "-r" must be placed in curly braces since a space is used between the time value and time unit.

```
force input1 1 10 ns, 0 {20 ns} -r 100ns
```

• Force signal `s` to alternate between values 1 and 0 every 100 time units until time 1000. Cancellation occurs at the last simulation delta cycle of a time unit.

```
force s 1 0, 0 100 -repeat 200 -cancel 1000
```

So,

```
force s 1 0 -cancel 0
```

will force signal `s` to 1 for the duration of the current time period.

• Force `siga` to decimal value 85 whenever the value on the signal is 1.

```
when {/mydut/siga = 10#1} {
    force -deposit /mydut/siga 10#85
}
```

### Related Topics

- `change`
- `DefaultForceKind`
- `Design Object Names`
- `Force Command Defaults`
- `noforce`
- `Virtual Signals`
**help**

This command displays in the Transcript window a brief description and syntax for the specified command.

**Syntax**

```
help [<command> | <topic>]
```

**Arguments**

- `<command>`
  (optional) Specifies the command for which you want help. The entry is case and space sensitive.

- `<topic>`
  (optional) Specifies a topic for which you want help. The entry is case and space sensitive. Specify one of the following six topics:

<table>
<thead>
<tr>
<th>Topic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>commands</td>
<td>Lists all available commands and topics</td>
</tr>
<tr>
<td>debugging</td>
<td>Lists debugging commands</td>
</tr>
<tr>
<td>execution</td>
<td>Lists commands that control execution of your simulation.</td>
</tr>
<tr>
<td>Tcl</td>
<td>Lists all available Tcl commands.</td>
</tr>
<tr>
<td>Tk</td>
<td>Lists all available Tk commands.</td>
</tr>
<tr>
<td>incrTCL</td>
<td>Lists all available incrTCL commands</td>
</tr>
</tbody>
</table>
**history**

This command lists the commands you have executed during the current session. History is a Tcl command. For more information, consult the Tcl Man Pages (Help > Tcl Man Pages).

**Syntax**

```
history [clear] [keep <value>]
```

**Arguments**

- **clear**
  
  (optional) Clears the history buffer.

- **keep <value>**
  
  (optional) Specifies the number of executed commands to keep in the history buffer.

  `<value>` — Any positive integer where the default is 50.
layout

This command allows you to perform a number of editing operations on custom GUI layouts, such as loading, saving, maximizing, and deleting.

The command options include:

- `layout active` – returns the current active window
- `layout current` – lists the current layout
- `layout delete` – removes the current layout from the .modelsim file (UNIX/Linux) or Registry (Windows)
- `layout load` – opens the specified layout
- `layout names` – lists all known layouts
- `layout normal` – minimizes the current maximized window
- `layout maximized` – return a 1 if the current layout is maximized, or a 0 if minimized
- `layout save` – saves the current layout to the specified name
- `layout togglezoom` – toggles the current zoom state of the active window (from minimized to maximized or maximized to minimized)
- `layout zoomactive` – maximizes the current active window
- `layout zoomwindow` – maximizes the specified window

**Syntax**

```
layout active
layout current
layout delete <name>
layout load <name>
layout names
layout normal
layout maximized
layout save <name>
layout togglezoom
layout zoomactive
layout zoomwindow <window>
```
Arguments

- <name>
  (required) Specifies the name of the layout.

- <window>
  (required) The window specification can be any format accepted by the view command. The window can be specified by its type (i.e., wave, list, objects, etc.), by the windowobj name (i.e., .main-pane.wave, .main-pane.library, etc.), or by the tab name (i.e., wave1, list3, etc.)

Related Topics

- Layouts and Modes of Operation
This command creates a wave log format (WLF) file containing simulation data for all HDL objects whose names match the provided specifications. Objects that are displayed using the `add list` and `add wave` commands are automatically recorded in the WLF file. By default the file is named `vsim.wlf` and stored in the current working directory. You can change the default name using the `-wlf` option of the `vsim` command or by setting the `WLFFilename` variable in the `modelsim.ini` file.

If no port mode is specified, the WLF file contains data for all objects in the selected region whose names match the object name specification.

The WLF file contains a record of all data generated for the list and wave windows during a simulation run. Reloading the WLF file restores all objects and waveforms and their complete history from the start of the logged simulation run. See `dataset open` for more information.

For all transaction streams created through the SCV or Verilog APIs, logging is enabled by default. A transaction is logged to the WLF file if logging is enabled at the beginning of a simulation run when the design calls `::begin_transaction()` or `$begin_transaction`. The effective start time of the transaction (the time passed by the design as a parameter to `::begin_transaction`) is irrelevant. For example, a stream could have logging disabled between T1 and T2 and still record a transaction in that period, through retroactive logging after time T2. A transaction is always either entirely logged or entirely ignored.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

---

**Note**

The log command is also known as the "add log" command.

---

**Syntax**

```
log [-flush] [-howmany] {[-in] [-inout] [-out] | [-ports] [ -internal]} [-out] [-ports] [-recursive [-depth <level>]] <object_name> ...
```

**Arguments**

- `-depth <level>`
  
  (optional) Restricts a recursive search (specified with the `-recursive` argument) to a certain level of hierarchy.

  `<level>` — Any non-negative integer. For example, if you specify `-depth 1`, the command descends only one level in the hierarchy.

- `-flush`
  
  (optional) Adds region data to the WLF file after each individual log command. Default is to add region data to the log file for the following conditions:

  - A command is executed that advances simulation time (e.g., run, step, etc.).
You quit the simulation.

- **-howmany**
  (optional) Returns an integer indicating the number of signals found.

- **-in**
  (optional) Specifies that the WLF file is to include data for ports of mode IN whose names match the specification.

- **-inout**
  (optional) Specifies that the WLF file is to include data for ports of mode INOUT whose names match the specification.

- **-internal**
  (optional) Specifies that the WLF file is to include data for internal (non-port) objects whose names match the specification.

- **-out**
  (optional) Specifies that the WLF file is to include data for ports of mode OUT whose names match the specification.

- **-ports**
  (optional) Specifies that the scope of the search is to include all ports, IN, INOUT, and OUT.

- **-recursive**
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region. You can use the -depth argument to specify how far down the hierarchy to descend.

- **<object_name>**
  (required) Specifies the object name that you want to log. Must be specified as the final argument to the log command. Multiple object names are specified as a space separated list. Wildcard characters are allowed. Note that the WildcardFilter Tcl preference variable identifies types to ignore when matching objects with wildcard patterns.

  By default, wildcard card logging does not log the internals of cells. Refer to the +libcell argument of the vlog command for more information.

**Examples**

- Log all objects in the design.
  
  `log -r /*`

- Log all output ports in the current design unit.

  `log -out *`
Related Topics

- add list
- add wave
- dataset alias
- dataset clear
- dataset close
- dataset config
- dataset config
- dataset info
- dataset list
- dataset open
- dataset rename
- dataset restart
- dataset save
- dataset snapshot
- nolog
- Recording Simulation Results With Datasets
- vlog +libcell
- Wildcard Characters
**Ishift**

This command takes a Tcl list as an argument and shifts it in-place, one place to the left, eliminating the left-most element.

The number of shift places may also be specified. Returns nothing.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

**Syntax**

```
Ishift <list> [<amount>]
```

**Arguments**

- `<list>`
  
  (required) Specifies the Tcl list to target with Ishift. Must be specified as the first argument to the `Ishift` command.

- `<amount>`
  
  (optional) Specifies the number of places to shift where the default is 1.

**Examples**

```
proc myfunc args {
    # throws away the first two arguments
    Ishift args 2
    ...
}
```

**Related Topics**

- See the Tcl man pages (Help > Tcl Man Pages) for details.
Isublist

This command returns a sublist of the specified Tcl list that matches the specified Tcl glob pattern.

Arguments to this command are order dependent. Follow the order specified in the Syntax section.

Syntax

Isublist <list> <pattern>

Arguments

- <list> (required) Specifies the Tcl list to target with Isublist.
- <pattern> (required) Specifies the pattern to match within the <list> using Tcl glob-style matching.

Examples

- In the example below, variable ‘t’ returns "structure signals source".

```tcl
set window_names "structure signals variables process source wave list dataflow"
set t [lsublist $window_names s*]
```

Related Topics

- The set command is a Tcl command. See the Tcl man pages (Help > Tcl Man Pages) for details.
mem compare

This command compares a selected memory to a reference memory or file. Must have the "diff" utility installed and visible in your search path in order to run this command.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

Syntax

```
mem compare { [-mem <ref_mem>] | [-file <ref_file>] } [actual_mem]
```

Arguments

- `-mem <ref_mem>`
  (optional) Specifies a reference memory to be compared with actual_mem.
  `<ref_mem>` — A memory record.

- `-file <ref_file>`
  (optional) Specifies a reference file to be compared with actual_mem.
  `<ref_file>` — A saved memory file.

- `actual_mem`
  (required) Specifies the name of the memory to be compared against the reference data. Must be specified as the final argument to the **mem compare** command.
mem display

This command prints to the Transcript window the memory contents of the specified instance. If the given instance path contains only a single array signal or variable, the signal or variable name need not be specified.

You can redirect the output of the mem display command into a file for later use with the mem load command. The output file can also be read by the Verilog $readmem system tasks if the memory module is a Verilog module and Verilog memory format (hex or binary) is specified.

Address radix, data radix, and address range for the output can also be specified, as well as special output formats.

By default, identical data lines are printed. To replace identical lines with a single line containing the asterisk character, you can enable compression with the -compress argument.

**Note**
The format settings are stored at the top of this file as a pseudo comment so that subsequent mem load commands can correctly interpret the data. Do not edit this data when manipulating a saved file.

Arguments to this command are order dependent. Please read through the argument descriptions for more information.

**Syntax**

```plaintext
mem display [-addressradix [d | h]] [-compress] [-dataradix <radix_type>]
[-endaddress <end>][-format [bin | hex | mti]] [-noaddress] [-startaddress <st>]
[-wordsperline <n>] [<path>]
```

**Arguments**

- **-addressradix [d | h]**
  (optional) Specifies the address radix for the default (MTI) formatted files.
  - d — Decimal radix. (default if -format is specified as mti.)
  - h — Hex radix.

- **-compress**
  (optional) Specifies that identical lines not be printed. Reduces the file size by replacing exact matches with a single line containing an asterisk. These compressed files are automatically expanded during a mem load operation.

- **-dataradix <radix_type>**
  (optional) Specifies the data radix for the default (MTI) formatted files. If unspecified, the global default radix is used.
  - <radix_type> A specified radix type. Valid entries (or any unique abbreviations) are: binary, decimal, unsigned, octal, hex, symbolic, and default. If no radix is specified for an enumerated type, the symbolic representation is used.
You can change the default radix type for the current simulation using the `radix` command or make the default radix permanent by editing the `DefaultRadix` variable in the `modelsim.ini` file.

- `-endaddress <end>`
  (optional) Specifies the end address for a range of addresses to be displayed.
  
  `<end>` — Any valid address in the memory. If unspecified, the default is the end of the memory.

- `-format [bin | hex | mti]`
  (optional) Specifies the output format of the contents.

  `bin`— Specifies a binary output.
  `hex`— Specifies a hex output.
  `mti` — MTI format. (default).

- `-noaddress`
  (optional) Specifies that addresses not be printed.

- `-startaddress <st>`
  (optional) Specifies the start address for a range of addresses to be displayed.

  `<st>` — Any valid address in the memory. If unspecified, the default is the start of the memory.

- `-wordsperline <n>`
  (optional) Specifies how many words are to be printed on each line.

  `<n>` — Any positive integer where the default is an 80 column display width.

- `<path>`
  (required) Specifies the full path to the memory instance. The default is the current context, as shown in the Structure window. Indexes can be specified. Must be specified as the final argument to the `mem display` command.

**Examples**

- This command displays the memory contents of instance `/top/c/mru_mem`, addresses 5 to 10:

  ```
  mem display -startaddress 5 -endaddress 10 /top/c/mru_mem
  ```

  returns:
  
  ```
  # 5: 110 110 110 110 110 000
  ```

- Display the memory contents of the same instance to the screen in hex format, as follows:

  ```
  mem display -format hex -startaddress 5 -endaddress 10 /top/c/mru_mem
  ```

  returns:
Commands

mem display

# 5: 6 6 6 6 6 0

Related Topics

- For details on MTI format, see the description contained in mem load.
**mem list**

This command displays a flattened list of all memory instances in the current or specified context after a design has been elaborated.

Each instance line is prefixed by "VHDL:" or "Verilog:”, depending on the type of model. Returns the signal/variable name, address range, depth, and width of the memory.

**Syntax**

```
mem list [-r] [<path>]
```

**Arguments**

- `-r` (optional) Recursively descends into sub-modules when listing memories.
- `<path>` (optional) The hierarchical path to the location the search should start where the default is the current context, as shown in the Structure window.

**Examples**

- Recursively list all memories at the top level of the design.
  ```
  mem list -r /
  ```
  Returns:
  ```
  # Verilog: /top/m/mem[0:255](256d x 16w)
  #
  ```

- Recursively list all memories in `/top2/uut`.
  ```
  mem list /top2/uut -r
  ```
  Returns:
  ```
  # Verilog: /top2/uut/mem[0:255] x 16w
  ```
mem load

This command updates the simulation memory contents of a specified instance. You can upload contents either from a memory data file, a memory pattern, or both. If both are specified, the pattern is applied only to memory locations not contained in the file.

A relocatable memory file is one that has been saved without address information. You can load a relocatable memory file into the instance of a memory core by specifying an address range on the mem load command line. If no address range (starting and ending address) is specified, the memory is loaded starting at the first location.

The order in which the data is placed into the memory depends on the format specified by the -format option. If you choose bin or hex format, the memory is filled low to high, to be compatible with $readmem commands. This is in contrast to the default MTI format, which fills the memory according to the memory declaration, from left index to right index.

For Verilog objects and VHDL integers and std_logic types: if the word width in a file is wider than the word width of the memory, the leftmost bits (msb) in the data words are ignored. To allow wide words use the -truncate option which will ignore the msb bits that exceed the memory word size. If the word width in the file is less than the width of the memory, and the leftmost digit of the file data is not ‘X’, then the leftmost bits are zero filled. Otherwise, they are X-filled.

The type of data required for the -filldata argument is dependent on the -filltype specified: a fixed value, or one that governs an incrementing, decrementing, or random sequence.

- For fixed pattern values, the fill pattern is repeatedly tiled to initialize the memory block specified. The pattern can contain multiple word values for this option.
- For incrementing or decrementing patterns, each memory word is treated as an unsigned quantity, and each successive memory location is filled in with a value one higher or lower than the previous value. The initial value must be specified.
- For a random pattern, a random data sequence will be generated to fill in the memory values. The data type in the sequence will match the type stored in the memory. For std_logic and associated types, unsigned integer sequences are generated. A seed value may be specified on the command line. For any given seed, the generated sequence is identical.

The interpretation of the pattern data is performed according to the default system radix setting. However, this can be overridden with a standard Verilog-style ‘<radix_char><data>’ specification.

Syntax

mem load -infile <infile> [-endaddress <end>] [-filltype {dec | inc | rand | value} -filldata <data_word>] [-fillradix <radix_type>] [-format [bin | hex | mti] [-path] [-skip <Nwords>] [-startaddress <st>] [-truncate]
Arguments

- **-infile <infile>**
  (Required unless the -filltype argument is used.) Updates memory data from the specified file.
  
  <infile> — The name of a memory file.

- **-endaddress <end>**
  (optional) Specifies the end address for a range of addresses to be loaded.
  
  <end> — Specified as any valid address in the memory.

- **-filltype {dec | inc | rand | value}**
  (Required unless the -infile argument is used, in which case it is optional.) Fills in memory addresses in an algorithmic pattern starting with the data word specified in -filldata. If a fill pattern is used without a file option, the entire memory or specified address range is filled with the specified pattern.
  
  dec — Decrement each succeeding memory word by one digit.
  inc — Increment each succeeding memory word by one digit.
  rand — Randomly generate each succeeding memory word starting with the word specified by -filldata as the seed.
  value — Value (default) Substitute each memory word in the range with the value specified in -filldata.

- **-filldata <data_word>**
  (required when -filltype is used) Specifies a data word used to fill memory addresses in the pattern specified by -filltype.
  
  <data_word> — Specifies a data word. Must be in the same format as specified by the -fillradix switch.

- **-fillradix <radix_type>**
  Specifies radix of the data specified by the -filldata switch.
  
  <radix_type> — Valid entries (or any unique abbreviations) are: binary, decimal, unsigned, octal, hex, symbolic, and default.

- **-format [bin | hex | mti]**
  (optional) Specifies the format of the file to be loaded.
  
  bin — Specifies binary data format.
  hex — Specifies hex format.
  mti — MTI format. (default).

Specifies the format of the file to be loaded. The bin and hex values are the standard Verilog hex and binary memory pattern file formats. These can be used with Verilog memories, and with VHDL memories composed of std_logic types.
In the MTI memory data file format, internal file address and data radix settings are stored within the file itself. Thus, there is no need to specify these settings on the mem load command line. If a format specified on the command line and the format signature stored internally within the file do not agree, the file cannot be loaded.

- `<path>`
  (optional) The hierarchical path to the memory instance. If the memory instance name is unique, shorthand instance names can be used. The default is the current context, as shown in the Structure window.

Memory address indexes can be specified in the instance name also. If addresses are specified both in the instance name and the file, only the intersection of the two address ranges is populated with memory data.

- `-skip <Nwords>`
  (optional) Specifies the number of words to be skipped between each fill pattern value. Used with `-filltype` and `-filldata`.

  `<Nwords>` — Specified as an unsigned integer.

- `-startaddress <st>`
  (optional) Specifies the start address for a range of addresses to be loaded.

  `<st>` — Any valid address in the memory.

- `-truncate`
  (optional) Ignores any most significant bits (msb) in a memory word which exceed the memory word size. By default, when memory word size is exceeded, an error results.

### Examples

- Load the memory pattern from the file `vals.mem` to the memory instance `/top/m/mem`, filling the rest of the memory with the fixed-value 1'b0.

  ```
  mem load -infile vals.mem -format bin -filltype value -filldata 1'b0 /top/m/mem
  ```

  When you enter the mem display command on memory addresses 0 through 12, you see the following:

  ```
  mem display -startaddress 0 -endaddress 12 /top/m/mem
  #  0: 0000000000000000 0000000000000001 0000000000000010 0000000000000011
  #  4: 0000000000000100 0000000000000101 0000000000000110 0000000000000111
  #  8: 0000000000001000 0000000000001001 0000000000000000 0000000000000000
  # 12: 0000000000000000
  ```

- Load the memory pattern from the file `vals.mem` to the memory instance `/top/m/mru_mem`, filling the rest of the memory with the fixed-value 16'Hbeef.

  ```
  mem load -infile vals.mem -format hex -st 0 -end 12 -filltype value -filldata 16'Hbeef /top/m/mru_mem
  ```
• Load memory instance /top/mem2 with two words of memory data using the Verilog Hex format, skipping 3 words after each fill pattern sequence.
  
  `mem load -filltype value -filldata "16'hab 16'hcd" /top/mem2 -skip 3`

• Truncate the msb bits that exceed the maximum word size (specified in HDL code).
  
  `mem load -format h -truncate -infile data_files/data.out /top/m_reg_inc/mem`

Related Topics

• `mem save`
mem save

This command saves the contents of a memory instance to a file in any of the supported formats: Verilog binary, Verilog hex, and MTI memory pattern data.

This command works identically to the mem display command, except that its output is written to a file rather than a display.

The order in which the data is placed into the saved file depends on the format specified by the -format argument. If you choose bin or hex format, the file is populated from low to high, to be compatible with $readmem commands. This is in contrast to the default mti format, which populates the file according to the memory declaration, from left index to right index.

You can use the mem save command to generate relocatable memory data files. The -noaddress option omits the address information from the memory data file. You can later load the generated memory data file using the memory load command.

Syntax

mem save -outfile <filename> [-addressradix {dec | hex}] [-dataradix <radix_type>] [-format {bin | hex | mti}] [-compress | -noaddress] [ <path> ] [-startaddress <st> -endaddress <end>] [-wordsperline <Nwords>]  

Arguments

- -outfile <filename>
  (required) Specifies that the memory contents are to be stored in a file.
  
  <filename> — The name of the file where the specified memory contents are to be stored.

- -addressradix {dec | hex}
  (optional) Specifies the address radix for the default mti formatted files.
  
  dec — Decimal (default).
  hex — Hexadecimal.

- -compress
  (optional) Specifies that only unique lines are printed, identical lines are not printed. Mutually exclusive with the -noaddress switch.

- -dataradix <radix_type>
  (optional) Specifies the data radix for the default mti formatted files.
  
  <radix_type> — Valid entries (or any unique abbreviations) are: binary, decimal, unsigned, octal, hex, and symbolic.

You can change the default radix for the current simulation using the radix command. You can change the default radix permanently by editing the DefaultRadix variable in the modelsim.ini file.
-endaddress <end>
  (optional) Specifies the end address for a range of addresses to be saved.
  <end> — Any valid address in the memory.

-format {bin | hex | mti}
  (optional) Specifies the format of the output file.
  bin— Binary data format.
  hex— Hexadecimal format.
  mti — MTI format. (default).

The bin and hex values are the standard Verilog hex and binary memory pattern file formats. These can be used with Verilog memories, and with VHDL memories composed of std_logic types.

In the MTI memory data file format, internal file address and data radix settings are stored within the file itself.

-noaddress
  (optional) Prevents addresses from being printed. Mutually exclusive with the -compress switch.

<path>
  (optional) The hierarchical path to the location of the memory instance. The default is the current context, as shown in the Structure window.

-startaddress <st>
  (optional) Specifies the start address for a range of addresses to be saved.
  <st> — Any valid address in the memory.

-wordsperline <Nwords>
  (optional) Specifies how many memory values are to be printed on each line.
  <Nwords> — Any unsigned integer where the default assumes an 80 character display width.

Examples

- Save the memory contents of the instance /top/m/mem(0:10) to memfile, written in the mti radix.

  mem save -format mti -outfile memfile -start 0 -end 10 /top/m/mem

  The contents of memfile are as follows:

  // memory data file (do not edit the following line - required for mem load use)
  // format=mti addressradix=d dataradix=s version = 1.0
  0: 0000000000000000 0000000000000000 0000000000000000 0000000000000000
  4: 0000000000000000 0000000000000000 0000000000000000 0000000000000000
  8: 0000000000000000 0000000000000000 0000000000000000 0000000000000000
Commands

mem save

Related Topics

- mem display
- mem load
**mem search**

This command finds and prints to the screen the first occurring match of a specified memory pattern in the specified memory instance. Shorthand instance names are accepted.

Optionally, you can instruct the command to print all occurrences. The search pattern can be one word or a sequence of words.

**Syntax**

```
mem search { -glob <word>[ <word>…] | -regexp <word>[ <word>…] }
              [-addressradix { dec | hex }] [-dataradix <radix_type> ] [-all] [-replace <word>[ <word>…]]
              [-startaddress <address>] [-endaddress <address>] [ <path> ]
```

**Arguments**

- `-glob <word>[ <word>…]`  
  (required unless using `-regexp`) Specifies the value of the pattern, accepting glob pattern syntax for the search.

  `<word>` — Any word pattern. Multiple word patterns are specified as a space separated list. Wildcards are accepted in the pattern.

  This argument and `-regexp` are mutually exclusive arguments.

- `-regexp <word>[ <word>…]`  
  (required unless using `-glob`) Specifies the value of the pattern, accepting regular expression syntax for the search.

  `<word>` — Any word pattern. Wildcards are accepted in the pattern. Multiple word patterns are specified as a space separated list.

  This argument and `-glob` are mutually exclusive arguments.

- `-addressradix { dec | hex }`  
  (optional) Specifies the radix for the address being displayed.

  - dec — Decimal (default).
  - hex — Hexadecimal.

- `-all`  
  (optional) Searches the specified memory range and returns all matching occurrences to the transcript. By default only the first matching occurrence is printed.

- `-dataradix <radix_type>`  
  (optional) Specifies the radix for the memory data being displayed.

  `<radix_type>` — Can be specified as symbolic, binary, octal, decimal, unsigned, or hex. By default the radix displayed is the system default.
You can change the default radix for the current simulation using the `radix` command. You can change the default radix permanently by editing the `DefaultRadix` variable in the `modelsim.ini` file.

- `-endaddress <address>`
  (optional) Specifies the end address for a range of addresses to search.
  
  `<address>` — Any valid address in the memory.

- `<path>`
  (optional) Specifies the hierarchical path to the location of the memory instance. The default is the current context, as shown in the Structure window.

- `-replace <word>[ <word>…]`
  (optional) Replaces the found patterns with a designated pattern.
  
  `<word>` — A word pattern Multiple word patterns are accepted, separated by a single space. No wildcards are allowed in the replaced pattern.

- `-startaddress <address>`
  (optional) Specifies the start address for a range of addresses to search.
  
  `<address>` — Any valid address in the memory.

### Examples

- Search for and print to the screen all occurrences of the pattern `16'Hbeef` in `/uut/u0/mem3`:

  ```
  mem search -glob 16'Hbeef -d hex /uut/u0/mem3
  ```

  Returns:

  ```
  #7845: beef
  #7846: beef
  #100223: beef
  ```

- Search for and print only the first occurrence of `16'Hbeef` in the address range 7845:150000, replacing it with `16'Hcafe` in `/uut/u1/mem3`:

  ```
  mem search -glob 16'Hbeef -d hex -replace 16'Hcafe -st 7846 -end 150000 /uut/u1/mem3
  ```

  Returns:

  ```
  #7846: cafe
  ```

- Replace all occurrences of `16'Hbeef` with `16'Habe` in `/uut/u1/mem3`:

  ```
  mem search -glob 16'Hbeef -r 16'Habe -addressadix hex -all /uut/u1/mem3
  ```

  Returns:
• Search for and print the first occurrence any pattern ending in f:
  
  `mem search -glob "*f"`

• Search for and print the first occurrence of this multiple word pattern:

  `mem search -glob "abe cafe" /uut/u1/mem3`

• Search for patterns "0000 0000" or "0001 0000" in m/mem:

  `mem search -data hex -regexp {000[0|1] 0{4}} m/mem -all`

• Search for a pattern that has any number of 0s followed by any number of 1s as a memory location, and which has a memory location containing digits as the value:

  `mem search -regexp {^0+1+$ \d+} m/mem -all`

• Search for any initialized location in a VHDL memory:

  `mem search -regexp {[^U]} -all <vhdl_memory>`
messages clearfilter

This command removes any filter you have set in the Message Viewer. Refer to the section “Message Viewer Filter Dialog Box” for additional information about filtering in the Message Viewer.

Syntax

messages clearfilter

Arguments

- No arguments
messages setfilter

This command performs the same action as the Message Viewer Filter Dialog Box, which controls which messages are shown in the Message Viewer.

The ideal workflow for using this command is through the GUI:

1. View > Message Viewer.
2. Right-click in the Message Viewer and select Filter.
   The Message Viewer Filter dialog box is displayed
3. Create your filter.
4. OK or Apply.
   The Message Viewer updates based on your filter and a messages setfilter command, which is equivalent to your settings, is output to the transcript.
5. Retain the messages setfilter command from the transcript for future use.

Syntax

messages setfilter <tcl_list>

Arguments

• <tcl_list> — The tcl_list argument is a complex string of tcl code that controls the filter settings.

Examples

• Severity is error and time is greater than or equal to 100 ns

  messages setfilter {{} \ 
  ( Severity Contains {Case Insensitive} error )} \ 
  (AND ( Time >= 100 ns ))

• The objects field contains neither clock or reset

  messages setfilter {{} \ 
  ( Object Contains {Case Sensitive} clock )} \ 
  (NOR ( Object Contains {Case Sensitive} data ))

• The message string either contains reg_str2 or reg_str1

  messages setfilter {{} \ 
  ( Message Contains {Case Insensitive} reg_str2 )} \ 
  (OR ( Message Contains {Case Insensitive} reg_str1 ))
The `modelsim` command starts the ModelSim GUI without prompting you to load a design. This command is valid only for Windows platforms and may be invoked in one of three ways:

- from the DOS prompt
- from a ModelSim shortcut
- from the Windows Start > Run menu

To use `modelsim` arguments with a shortcut, add them to the target line of the properties of that shortcut. (As expected, arguments also work on the DOS command line.)

You can invoke the simulator from either the ModelSim> prompt after the GUI starts or from a DO file called by `modelsim`.

**Syntax**

```
modelsim [-do <macrofile>] [ <license_option>] [-nosplash]
```

**Arguments**

- `-do <macrofile>`
  - (optional) Executes a DO file when `modelsim` is invoked.
  - `<macrofile>` — The name of a DO file

**Note**

In addition to the macro called by this argument, if a DO file is specified by the STARTUP variable in `modelsim.ini`, it will be called when the `vsim` command is invoked.

- `<license_option>`
  - (optional) Restricts the search of the license manager.
- `-nosplash`
  - (optional) Disables the splash screen.

**Related Topics**

- `do`
- `vsim`
- Using a Startup File
noforce

This command removes the effect of any active force commands on the selected HDL objects and also causes the object’s value to be re-evaluated.

Syntax

```
noforce <object_name> …
```

Arguments

- `<object_name>`
  (required) Specifies the name of an object. Must match an object name used in a previous `force` command. Multiple object names may be specified as a space separated list. Wildcard characters are allowed.

Related Topics

- `force`
- `Wildcard Characters`
nolog

This command suspends writing of data to the wave log format (WLF) file for the specified signals.

A flag is written into the WLF file for each signal turned off, and the GUI displays "-No Data-" for the signal(s) until logging (for the signal(s)) is turned back on. Logging can be turned back on by issuing another log command or by doing a nolog -reset.

Because use of the nolog command adds new information to the WLF file, WLF files created when using the nolog command cannot be read by older versions of the simulator. If you are using dumplog64.c, you will need to get an updated version.

Transactions written in SCV or Verilog are logged automatically, and can be removed with the nolog command. A transaction is logged into the .wlf file if logging is enabled (in other words, if no nolog command has disabled it) for that stream at the time when the transaction was begun. An entire span of a transaction is either logged or not logged, regardless of the begin and end times specified for that transaction.

Syntax

```
```

Arguments

- **-all**  
  (optional) Turns off logging for all signals currently logged.

- **-depth <level>**  
  (optional) Restricts a recursive search (specified with the -recursive argument) to a certain level of hierarchy.

  <level> — An integer greater than or equal to zero. For example, if you specify -depth 1, the command descends only one level in the hierarchy.

- **-howmany**  
  (optional) Returns an integer indicating the number of signals found.

- **-in**  
  (optional) Turns off logging only for ports of mode IN whose names match the specification.

- **-inout**  
  (optional) Turns off logging only for ports of mode INOUT whose names match the specification.

- **-internal**  
  (optional) Turns off logging only for internal (non-port) objects whose names match the specification.
• **-out**
  (optional) Turns off logging only for ports of mode OUT whose names match the specification.

• **-ports**
  (optional) Specifies that the scope of the search is to include all ports.

• **-recursive**
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region. You can use the **-depth** argument to specify how many levels of the hierarchy to descend.

• **-reset**
  (optional) Turns logging back on for all unlogged signals.

• **<object_name>…**
  (optional) Specifies the object name which you want to unlog. Multiple object names may be specified as a space separated list. Wildcard characters are allowed.

**Examples**

• Unlog all objects in the design.
  ```bash
  nolog -r /*
  ```

• Turn logging back on for all unlogged signals.
  ```bash
  nolog -reset
  ```

**Related Topics**

• **add list**
• **add wave**
• **log**
notepad

This command opens a simple text editor. It may be used to view and edit ASCII files or create new files.

This mode can be changed from the Notepad Edit menu.

Returns nothing.

Syntax

    notepad [<filename>] [-r | -edit]

Arguments

- <filename>
  (optional) Name of the file to be displayed.
- -r
  (optional) Specifies read-only mode.
- -edit
  (optional) Specifies editing mode. Will not save changes to an existing file that has the Read-only attribute turned on. (default)
**noview**

This command closes a window in the ModelSim GUI. To open a window, use the **view** command.

**Syntax**

```
noview [<window_name>...]  
```

**Arguments**

- `<window_name>...`
  
    (required) Specifies the window(s) to close. Multiple window types may be specified in a space separated list. Wildcards permitted. At least one type (or wildcard) is required.

Refer to the view command for a complete list of possible arguments.

You can also close Source windows using the tab or file name.

**Examples**

- Close the Wave window named "wave1".
  
  ```
  noview wave1
  ```

- Close all List windows.
  
  ```
  noview List
  ```

**Related Topics**

- **view**
nowhen

This command deactivates selected when commands.

Syntax

nowhen [<label>]

Arguments

• <label>
  (optional) Specifies an individual when command. Wildcards may be used to select more than one when command.

Examples

• Deactivate the when command labeled 99.
  
  nowhen 99

• Deactivate all when commands.
  
  nowhen *

Related Topics

• when
onbreak

This command is used within a macro and specifies one or more commands to be executed when running a macro that encounters a breakpoint in the source code. The command must be followed by a run command to take effect.

Using the onbreak command without arguments will return the current onbreak command string. An onbreak command can contain macro calls.

Use the resume command to resume execution of the macro file after encountering a breakpoint.

Use an empty string to change the onbreak command back to its default behavior:

    onbreak ""

In this case, the macro will be interrupted after a breakpoint occurs (after any associated bp command string is executed).

Syntax

    onbreak {[<command>[; <command>] …]}

Arguments

- <command>

  (optional) Any command can be used as an argument to onbreak. If you want to use more than one command, use a semicolon to separate the commands, or place them on multiple lines. The entire command string must be placed in curly braces ({}). You must use the onbreak command before a run, run -continue, or step command. It is an error to execute any commands within an onbreak command string following any of the run commands. This restriction applies to any macros or Tcl procedures used in the onbreak command string.

Examples

- Examine the value of the HDL object data when a breakpoint is encountered. Then continue the run command.

    onbreak {exa data ; cont}

- Resume execution of the macro file on encountering a breakpoint.

    onbreak {resume}

- This set of commands test for assertions. Assertions are treated as breakpoints if the severity level is greater than or equal to the current BreakOnAssertion variable setting (refer to modelsim.ini Variables). By default a severity level of failure or above causes a breakpoint; a severity level of error or below does not.
Commands
onbreak

set broken 0
onbreak {
    set broken 1
    resume
}
run -all
if { $broken } {
    puts "failure"
} else {
    puts "success"
}

Related Topics

- abort
- bp
- do
- onerror
- resume
- status

- Useful Commands for Handling Breakpoints and Errors
- Macros (DO Files)
onElabError

This command specifies one or more commands to be executed when an error is encountered during the elaboration portion of a `vsim` command. The command is used by placing it within a macro.

Use the `onElabError` command without arguments to return to a prompt.

Syntax

```plaintext
onElabError {[<command> ; <command>] …]}
```

Arguments

- `<command>`
  
  (optional) Any command can be used as an argument to `onElabError`. If you want to use more than one command, use a semicolon to separate the commands, or place them on multiple lines. The entire command string must be placed in curly braces (`{}`).

Related Topics

- `do`
onerror

This command is used within a macro before a run command; it specifies one or more commands to be executed when a running macro encounters an error.

Using the onerror command without arguments will return the current onerror command string. Use an empty string (onerror """") to change the onerror command back to its default behavior. Use onerror with a resume command to allow an error message to be printed without halting the execution of the macro file.

You can also set the global OnErrorDefaultAction Tcl variable to dictate what action ModelSim takes when an error occurs. To set the variable on a permanent basis, you must define the variable in a modelsim.tcl file (Refer to “The modelsim.tcl File” for details).

When your onerror command is successful, the macro will continue normally, unless your command instructs the tool to quit, for example:

    onerror {quit -f}

or

    onerror {break}

However, if your onerror command is not successful, the simulator will be halted, for example:

    onerror {add wave b}

when you don’t have a signal named b.

The onerror command is executed when a Tcl command (for example, break.) encounters an error in the macro file that contains the onerror command (note that a run command does not necessarily need to be in process). Conversely, OnErrorDefaultAction will run even if the macro does not contain a local onerror command. This can be useful when you run a series of macros from one script, and you want the same behavior across all macros.

Syntax

    onerror {{<command> ; <command>} …}}

Arguments

•  <command>

    (optional) Any command can be used as an argument to onerror. If you want to use more than one command, use a semicolon to separate the commands, or place them on multiple lines. The entire command string must be placed in curly braces ({}).

Example

•  Force the simulator to quit if an error is encountered while the macro is running.

    onerror {quit -f}
Related Topics

- abort
- do
- onbreak
- resume
- status

- Useful Commands for Handling Breakpoints and Errors
- Macros (DO Files)
onfinish

This command controls simulator behavior when encountering $finish or sc_stop() in the design code. When you specify this command without an argument, it returns the current setting.

Syntax

onfinish [ask | exit | final | stop | default]

Arguments

  ask — (optional) In batch mode, the simulation will exit; in GUI mode, the user is prompted for action.
  exit — (optional) The simulation exits without asking for any confirmation.
  final — (optional) The simulation executes all finish blocks before exiting.
  stop — (optional) The simulation ends but remains loaded in memory, allowing for easier post-simulation tasks.
  default — (optional) Uses the current OnFinish setting in the modelsim.ini file.

Related Topics

- OnFinish modelsim.ini variable
- vsim -onfinish
-
pause

This command interrupts the execution of a macro and allows you to perform interactive debugging of a macro file. The command is placed within the macro to be debugged.

Syntax

```
pause
```

Arguments

- None.

Description

When a macro is interrupted during execution, the macro returns the prompt:

```
VSIM(paused)>
```

This “pause” prompt notifies you that a macro has been interrupted.

When a macro is paused, you can invoke another macro. If the second macro is interrupted, you can continue invoking macros up to a nesting level of 50 macros.

The `status` command lists summary information about all interrupted macros.

Use the `resume` command to resume execution of the macro. Use the `abort` command to stop execution of some or all of the macros.

Related Topics

- `abort`
- `do`
- `resume`
- `run`
- `status`
### precision

This command determines how real numbers display in the graphic interface (e.g., Objects, Wave, Locals, and List windows). It does not affect the internal representation of a real number and therefore precision values over 17 are not allowed.

Executing the **precision** command without any arguments returns the current precision setting.

### Syntax

```
precision [digits[#]]
```

### Arguments

- `<digits>[#]` *(optional)* Specifies the number of digits to display where the default is 6.
  
  # — A suffix that forces the display of trailing zeros. See examples for more details.

### Examples

- Results in 4 digits of precision.

  ```
  precision 4
  ```

  For example:

  ```
  1.234 or 6543
  ```

- Results in 8 digits of precision including trailing zeros.

  ```
  precision 8#
  ```

  For example:

  ```
  1.2345600 or 6543.2100
  ```

- Results in 8 digits of precision but doesn’t print trailing zeros.

  ```
  precision 8
  ```

  For example:

  ```
  1.23456 or 6543.21```
printenv

This command prints to the Transcript window the current names and values of all environment variables.

If variable names are given as arguments, returns only the names and values of the specified variables.

Syntax

   printenv [<var>…]

Arguments

   •  <var>…
      (optional) Specifies the name(s) of the environment variable(s) to print.

Examples

   •  Print all environment variable names and their current values.

      printenv

      Returns:

      # CC = gcc
      # DISPLAY = srl:0.0
      ...

   •  Print the specified environment variables:

      printenv USER HOME

      Returns:

      # USER = vince
      # HOME = /scratch/srl/vince
Commands

process report

This command creates a textual report of all processes displayed in the Process Window.

Syntax

process report [-file <filename>] [-append]

Arguments

- -file <filename>
  (optional) Creates an external file where raw process data will be saved. If -file is not specified, then the output is redirected to stdout.
  <filename> — A user-specified name for the file.
- -append
  (optional) Specifies that process data is to be appended to the current process report file. If this option is not used, the process data will overwrite the existing process report file.
project

This command is used to perform common operations on projects.

Prerequisites

Some arguments to this command require a project to be opened with either the project new or project open command. Some argument must be used outside of a simulation session. Please read the argument descriptions for more information.

Syntax

```
project [addfile <filename> [<file_type>] [<folder_name>]] | [addfolder <foldername> 
    [<folder_parent>]] | [calculateorder] | [close] | [compileall [-n]] | [compileorder] | 
    [compileoutofdate [-n]] | [delete <filename>] | [env] | [history] | [new <home_dir>
    <proj_name> [<defaultlibrary>] [<initialini> [0 | 1]] | [open <project>] | [removefile 
    <filename>]
```

Arguments

- **addfile** `<filename> [<file_type>] [<folder_name>]`
  (optional) Adds the specified file to the current project. Requires a project to be open.

  - `<filename>` — (required) The name of an existing file.
  - `<file_type>` — (optional) The HDL file type of the file being added. For example do for a .do file.
  - `<folder_name>` — (optional) Places the file in an existing folder created with `project addfolder` command. If no folder name is specified the file will be placed in the top level folder.

- **addfolder** `<foldername> [<folder_parent>]`
  (optional) Creates a project folder within the project. Requires a project to be open.

  - `<foldername>` — (required) Any string.
  - `<folder_parent>` — (optional) Places `<foldername>` in an existing parent folder. If `<folder_parent>` is unspecified, `<foldername>` is placed at the top level.

- **calculateorder**
  (optional) Determines the compile order for the project by compiling each file, then moving any compiles that fail to the end of the list. This is repeated until there are no more compile errors.

- **close**
  (optional) Closes the current project.

- **compileall [-n]**
  (optional) Compiles all files in the project using the defined compile order.

  - `-n` — (optional) Returns a list of the compile commands this command would execute, without actually executing the compiles.
Commands

project

- compileorder
  (optional) Returns the current compile order list.

- compileoutofdate [-n]
  (optional) Compiles all files that have a newer date/time stamp than the last time the file was compiled.
  
  -n — Returns a list of the compile commands this command would execute, without actually executing the compiles.

- delete <filename>
  (optional) Deletes a project file.
  
  <filename> — Any .mpf file.

- env
  (optional) Returns the current project file and path.

- history
  (optional) Lists a history of manipulated projects. Must be used outside of a simulation session.

- new <home_dir> <proj_name> [defaultlibrary] [initialini] [0 | 1]
  (optional) Creates a new project under a specified home directory with a specified name and optionally a default library. The name of the work library will default to "work" unless specified. A new project cannot be created while a project is currently open or a simulation is in progress.
  
  <home_dir> — The path to the new project directory within the current working directory.
  
  <proj_name> — Specifies a name for the new project. The file will be saved as a .mpf file.
  
  <defaultlibrary> — Specifies a name for the default library.
  
  <initialini> — An optional modelsim.ini file can be specified as a seed for the project file by using the initialini option. If initialini is an empty string, then ModelSim uses the current modelsim.ini file when creating the project. You must specify a default library if you want to specify initialini.
  
  0 — (default) Copies all library mappings from the specified <initialini> file into the new project.
  
  1 — Copies library mappings referenced in an "others" clause in the initial .ini file.

- open <project>
  (optional) Closes any currently opened project and opens a specified project file (must be a valid .mpf file), making it the current project. Changes the current working directory to the project's directory. Must be used outside of a simulation session.
• removefile <filename>
  (optional) Removes the specified file from the current project.

Examples

• Make /user/george/design/test3/test3.mpf the current project and changes the current working directory to /user/george/design/test3.

  project open /user/george/design/test3/test3.mpf

• Execute current project library build scripts.

  project compileall
pwd

This Tcl command displays the current directory path in the Transcript window.

Syntax

pwd

Arguments

- None
quietly

This command turns off transcript echoing for the specified command.

Syntax

quietly <command>

Arguments

- <command>

(required) Specifies the command for which to disable transcript echoing. Any results normally echoed by the specified command will not be written to the Transcript window. To disable echoing for all commands use the transcript command with the -quietly option.

Related Topics

- transcript
Commands

quit

quit

This command exits the simulator.

If you want to stop the simulation using a when command, you must use a stop command within your when statement, you must not use an exit or a quit command. The stop command acts like a breakpoint at the time it is evaluated.

Syntax

quit [-f | -force] [-sim] [-code <integer>]

Arguments

• -f | -force
  (optional) Quits without asking for confirmation. If omitted, ModelSim asks you for confirmation before exiting. (The -f and -force arguments are equivalent.)

• -sim
  (optional) Unloads the current design in the simulator without exiting ModelSim. All files opened by the simulation will be closed including the WLF file (vsim.wlf).

• -code <integer>
  (optional) Quits the simulation and issues an exit code.

  <integer> — This is the value of the exit code. You should not specify an exit code that already exists in the tool. Refer to the section “Exit Codes” in the User’s Manual for a list of existing exit codes. You can also specify a variable in place of <integer>.

  You should always print a message before executing the quit -code command to explicitly state the reason for exiting.

Examples

Refer to the Examples section of the exit command for an example of using the -code argument. The quit and exit commands behave similarly in this regard.
radix

This command specifies the default radix to be used for the current simulation. Specifying the command with no argument returns the current radix setting.

The command can be used at any time. The specified radix is used for all commands (force, examine, change, etc.) as well as for displayed values in the Objects, Locals, Dataflow, List, and Wave windows.

Alternate methods for changing the default radix:

- In the modelsim.ini file, edit the DefaultRadix variable.
- Choose Simulate > Runtime Options from the main menu, click the Defaults tab, make your selection in the Default Radix box.

Syntax

radix [-symbolic | -binary | -octal | -decimal | -hexadecimal | -unsigned | -ascii | -time] [-enumnumeric | -enumsymbolic]

Arguments

You can abbreviate the following arguments to any length. For example, -dec is equivalent to -decimal.

- -symbolic
  (optional) Displays values in a form closest to their natural form.
- -binary
  (optional) Displays values in binary format.
- -octal
  (optional) Displays values in octal format.
- -decimal
  (optional) Displays values in decimal format. You can specify -signed as an alias for this argument.
- -hexadecimal
  (optional) Displays values in hexadecimal format.
- -unsigned
  (optional) Displays values in unsigned decimal format.
- -ascii
  (optional) Display a Verilog object as a string equivalent using 8-bit character encoding.
- -time
  (optional) Displays values of time for register-based types in Verilog.
Commands

radix

- **-enumnumeric**
  (optional) Causes Verilog and SystemC enums to be displayed as numbers (formatted by the current radix). This overrides the default behavior of always showing enums symbolically.

- **-enumsymbolic**
  (optional) Restores the default behavior of displaying Verilog and SystemC enums as symbols by reversing the action of the -enumnumeric option.

**Related Topics**

- User-Defined Radices
- radix define
- radix names
- radix list
- radix delete


**radix define**

This command is used to create or modify a user-defined radix. A user definable radix is used to map bit patterns to a set of enumeration labels. User-defined radices are available for use in the Wave and List windows or with the `examine` command.

**Syntax**

```
radix define <name> <definition_body> [-color <value>]
```

**Arguments**

- **<name>**
  
  (required) User-specified name for the radix.

- **<definition_body>**
  
  (required) A list of number pattern, label pairs. The definition body has the form:
  
  ```
  { 
    <numeric-value> <enum-label>,
    <numeric-value> <enum-label>
    -default <radix_type>
  }
  ```
  
  A `<numeric-value>` is any legitimate HDL integer numeric literal. To be more specific:
  
  ```
  <base>#<base-integer># --- <base> is 2, 8, 10, or 16
  <base>"bit-value" --- <base> is B, O, or X
  <integer>
  <size>'<base><number> --- <size> is an integer, <base> is b, d, o, or h.
  ```
  
  Check the Verilog and VHDL LRM’s for exact definitions of these numeric literals.

  The comma (,) in the definition body is optional. The `<enum-label>` is any arbitrary string. It should be surrounded by quotes (""), especially if it contains spaces.

  The `-default` entry is optional. If present, it defines the radix to use if a match is not found for a given value. The `-default` entry can appear anywhere in the list, it does not have to be at the end.

- **-color <value>**
  
  (optional) Designates a color for the waveform and text in the Wave window.

  `<value>` — The color value may be a color name or its hex value (see example below).

**Example**

- The radix define command used to create a radix called “States,” which will display state values in the List, Watch, and Wave windows instead of numeric values.

  ```
  radix define States {
    11'b00000000001 "IDLE",
    11'b00000000010 "CTRL",
  }
  ```
The following example illustrates how to specify the radix color:

```
radix define States {
    11'b00000000001 "IDLE" -color yellow,
    11'b00000000010 "CTRL" -color #ffee00,
    11'b00000000100 "WT_WD_1" -color orange,
    11'b00000001000 "WT_WD_2" -color orange,
    11'b00000010000 "WT_BLK_1",
    11'b00000100000 "WT_BLK_2",
    11'b00001000000 "WT_BLK_3",
    11'b00010000000 "WT_BLK_4",
    11'b00100000000 "WT_BLK_5",
    11'b01000000000 "RD_WD_1" -color green,
    11'b10000000000 "RD_WD_2" -color green,
    -default hex
    -defaultcolor white
}
```

If a pattern/label pair does not specify a color, the normal wave window colors will be used. If the value of the waveform does not match any pattern, then the `-default radix` and `-defaultcolor` will be used.

To specify a range of values, wildcards may be specified for bits or characters of the value. The wildcard character is `?`, similar to the iteration character in a Verilog UDP, for example:
radix define {
  6'b01??00 "Write" -color orange,
  6'b10??00 "Read" -color green
}

In this example, the first pattern will match "010000", "010100", "011000", and "011100". In case of overlaps, the first matching pattern is used, going from top to bottom.

Related Topics

- User-Defined Radices
- radix
- radix names
- radix list
- radix delete
radix delete

This command will remove the radix definition from the named radix.

Syntax

radix delete <name>

Arguments

- <name> (required) Removes the radix definition from the named radix.

Related Topics

- User-Defined Radices
- radix
- radix define
- radix list
- radix names
radix list

This command will return the complete definition of a radix, if a name is given. If no name is given, it will list all the defined radices.

Syntax

radix list [<name>]

Arguments

• <name>
  (optional) Returns the complete definition of the named radix.

Related Topics

• User-Defined Radices
• radix
• radix define
• radix names
• radix delete
radix names

This command returns a list of currently defined radix names.

Syntax

radix names

Arguments

None

Related Topics

- User-Defined Radices
- radix
- radix define
- radix list
- radix delete
**readers**

This command displays the names of all readers of the specified object.

The reader list is expressed relative to the top-most design signal/net connected to the specified object.

**Syntax**

```
readers <object_name>
```

**Arguments**

- `<object_name>`
  
  (required) Specifies the name of the signal or net whose readers are to be shown. All signal or net types are valid. Multiple names and wildcards are accepted.

**Related Topics**

- `drivers`
**report**

This command displays information relevant to the current simulation.

**Syntax**

```
report files
report where [ini] [pwd] [transcript] [wlf] [project]
report simulator control
report simulator state
```

**Arguments**

- **files**
  Returns a list of all source files used in the loaded design. This information is also available in the Specified Path column of the Files window.

- **where [ini] [pwd] [transcript] [wlf] [project]**
  Returns a list of configuration files where the arguments limit the list to those files specified. If specified without arguments, returns a list of all configuration files in the current simulation.

  - *ini* — (optional) Returns the location of the modesim.ini file.
  - *pwd* — (optional) Returns the current working directory.
  - *transcript* — (optional) Returns the location for saving the transcript file.
  - *wlf* — (optional) Returns the current location for saving the .wlf file.
  - *project* — (optional) Returns the current location of the project file.

- **simulator control**
  Displays the current values for all simulator control variables.

- **simulator state**
  Displays the simulator state variables relevant to the current simulation.

**Examples**

- Display configuration file information

  ```
  report where
  ```

  Returns:

  ```
  # INI {modelsim.ini}
  # PWD ./Testcases/dataflow
  # Transcript transcript
  # WLF vsim.wlf
  # Project {}
  ```

- Display all simulator control variables.
**report simulator control**

Returns:

```
# UserTimeUnit = ns
# RunLength =
# IterationLimit = 5000
# BreakOnAssertion = 3
# DefaultForceKind = default
# IgnoreNote = 0
# IgnoreWarning = 0
# IgnoreError = 0
# IgnoreFailure = 0
# IgnoreSVAInfo = 0
# IgnoreSVAWarning = 0
# IgnoreSVAEError = 0
# IgnoreSVAFatal = 0
# CheckpointCompressMode = 1
# NumericStdNoWarnings = 0
# StdArithNoWarnings = 0
# PathSeparator = /
# DefaultRadix = symbolic
# DelayFileOpen = 1
# WLFFilename = vsim.wlf
# WLFTimeLimit = 0
# WLFSizelimit = 0
```

- Display all simulator state variables. Only the variables that relate to the design being simulated are displayed:

  **report simulator state**

Returns:

```
# now = 0.0
# delta = 0
# library = work
# entity = type_clocks
# architecture = full
# resolution = 1ns
```

**Viewing preference variables**

Preference variables have more to do with the way things look (but not entirely) rather than controlling the simulator. You can view preference variables from the Preferences dialog box. Select **Tools > Edit Preferences** (Main window).

**Related Topics**

- modelsim.ini Variables
- Simulator GUI Preferences
Commands
restart

restart
This command reloads the design elements and resets the simulation time to zero. Only design elements that have changed are reloaded. (Note that SDF files are always reread during a restart.)

- If no design is loaded, the restart command produces a message to that effect and takes no further action.
- If a simulation is loaded, the restart command restarts the simulation.
- If multiple datasets are open, including a simulation, the environment is changed to the simulation context and the simulation is restarted.

Shared libraries are handled as follows during a restart:

- Shared libraries that implement VHDL foreign architectures only are reloaded at each restart when the architecture is elaborated (unless vsim -keeploaded is used).
- Shared libraries loaded from the command line (-foreign and -pli options) and from the Veriuser entry in the modelsim.ini file are reloaded (unless vsim -keeploaded is used).
- Shared libraries that implement VHDL foreign subprograms remain loaded (they are not reloaded) even if they also contain code for a foreign architecture.

You can configure defaults for the restart command by setting the DefaultRestartOptions variable in the modelsim.ini file. Refer to “Restart Command Defaults”.

To handle restarts with Verilog PLI applications, you need to define a Verilog user-defined task or function, and register a misctf class of callback. To handle restarts with Verilog VPI applications, you need to register reset callbacks. To handle restarts with VHDL FLI applications, you need to register restart callbacks. Refer to “Verilog Interfaces to C” for more information on the Verilog PLI/VPI/DPI and the ModelSim FLI Reference for more information on the FLI.

Syntax

Arguments
- -force
  (optional) Specifies that the simulation will be restarted without requiring confirmation in a popup window.
- -nobreakpoint
  (optional) Specifies that all breakpoints will be removed when the simulation is restarted where the default is for all breakpoints to be reinstalled after the simulation is restarted.
• -nolist
  (optional) Specifies that the current List window environment will **not** be maintained after the simulation is restarted where the default is for all currently listed HDL objects and their formats to be maintained.

• -nolog
  (optional) Specifies that the current logging environment will **not** be maintained after the simulation is restarted where the default is for all currently logged objects to continue to be logged.

• -nowave
  (optional) Specifies that the current Wave window environment will **not** be maintained after the simulation is restarted where the default is for all objects displayed in the Wave window to remain in the window with the same format.

**Related Topics**

• vsim
**Commands**

**resume**

This command is used to resume execution of a macro (DO) file after a **pause** command or a breakpoint.

This command may be input manually or placed in an **onbreak** command string. (Placing a **resume** command in a **bp** command string does not have this effect.) The **resume** command can also be used in an **onerror** command string to allow an error message to be printed without halting the execution of the macro file.

**Syntax**

```plaintext
resume
```

**Arguments**

- None

**Related Topics**

- **abort**
- **do**
- **onbreak**
- **onerror**
- **pause**
- **Useful Commands for Handling Breakpoints and Errors**
**run**

This command advances the simulation by the specified number of timesteps.

**Syntax**

run [ <timesteps>[<time_units>] | -all | -continue | -init | -next | -step | -over ]

**Arguments**

- No arguments
  - Runs the simulation for the default time (100 ns).
  - You can change the default <timesteps> and <time_units> in the GUI with the Run Length toolbar box in the Simulate toolbar or from the `modelsim.ini` file: RunLength and UserTimeUnit variables.

- <timesteps>[<time_units>] (optional)
  - Specifies the number of timesteps for the simulation to run. The number may be fractional, or may be specified as absolute by preceding the value with the character `@`.
  - `<time_units>` — Any valid time unit: fs, ps, ns, us, ms, or sec where the default is to use the current time unit.

- -all (optional)
  - Causes the simulator to run the current simulation forever, or until it hits a breakpoint or specified break event.

- -continue (optional)
  - Continues the last simulation run after a step command, step-over command or a breakpoint. A run-continue command may be input manually or used as the last command in a bp command string.

- -init (optional)
  - Initializes non-trivial static SystemVerilog variables before beginning the simulation, for example, expressions involving other variables and function calls. This could be useful for when you want to initialize values before executing any force, examine, or bp commands.
  - You cannot use run-init after any other run commands or if you have specified vsim -runinit on the command line because all variables would have been initialized by that point.

- -next (optional)
  - Causes the simulator to run to the next event time.

- -step (optional)
  - Steps the simulator to the next HDL statement.
**Commands**

**run**

- **-over**
  (optional) Directs ModelSim to run VHDL procedures and functions, Verilog tasks and functions, and C functions but to treat them as simple statements instead of entering and tracing them line by line.

**Examples**

- Advance the simulator 1000 timesteps.
  
  ```
  run 1000
  ```

- Advance the simulator the appropriate number of timesteps corresponding to 10.4 milliseconds.
  
  ```
  run 10.4 ms
  ```

- Advance the simulator to timestep 8000.
  
  ```
  run @8000
  ```

**Related Topics**

- **step**
- **Simulate Toolbar**
- **
runStatus

This command returns the current state of your simulation to stdout after issuing a run or step command.

Syntax

runStatus [-full]

Arguments

• -full
  (optional) Appends additional information to the output of the runStatus command.

Returns

Table 2-2 (runStatus results) and Table 2-3 (runStatus -full results) show outputs of the runStatus command.

### Table 2-2. runStatus Command States

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ready</td>
<td>The design is loaded and is ready to run.</td>
</tr>
<tr>
<td>break</td>
<td>The simulation stopped before completing the requested run.</td>
</tr>
<tr>
<td>error</td>
<td>The simulation stopped due to an error condition.</td>
</tr>
<tr>
<td>loading</td>
<td>The simulation is currently elaborating.</td>
</tr>
<tr>
<td>nodesign</td>
<td>There is no design loaded.</td>
</tr>
<tr>
<td>checkpoint</td>
<td>A checkpoint is being created, do not interrupt this process.</td>
</tr>
<tr>
<td>cready</td>
<td>The design is loaded and is ready to run in C debug mode.</td>
</tr>
<tr>
<td>initializing</td>
<td>The user interface initialization is in progress.</td>
</tr>
</tbody>
</table>

### Table 2-3. runStatus -full Command Information

<table>
<thead>
<tr>
<th>-full Information</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>bkpt</td>
<td>stopped at breakpoint</td>
</tr>
<tr>
<td>bkpt_builtin</td>
<td>stopped at breakpoint on builtin process</td>
</tr>
<tr>
<td>end</td>
<td>reached end of requested run</td>
</tr>
<tr>
<td>fatal_error</td>
<td>encountered fatal error (such as, divide by 0)</td>
</tr>
<tr>
<td>iteration_limit</td>
<td>iteration limit reached, possible feedback loop</td>
</tr>
<tr>
<td>silent_halt</td>
<td>mti_BreakSilent() called,</td>
</tr>
<tr>
<td>step</td>
<td>run -step completed</td>
</tr>
<tr>
<td>step_builtin</td>
<td>run -step completed on builtin process</td>
</tr>
</tbody>
</table>
### Table 2-3. runStatus -full Command Information

<table>
<thead>
<tr>
<th>-full Information</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>step_wait_suspend</td>
<td>run -step completed, time advanced.</td>
</tr>
<tr>
<td>user_break</td>
<td>run interrupted do to break-key or ^C (SIGINT)</td>
</tr>
<tr>
<td>user_halt</td>
<td>mti_Break() called.</td>
</tr>
<tr>
<td>user_stop</td>
<td>stop or finish requested from vpi, stop command, etc.</td>
</tr>
<tr>
<td>gate_oscillation</td>
<td>Verilog gate iteration limit reached.</td>
</tr>
<tr>
<td>simulation_stop</td>
<td>pli stop_simulation() called.</td>
</tr>
</tbody>
</table>
**searchlog**

This command searches one or more of the currently open logfiles for a specified condition. It can be used to search for rising or falling edges, for signals equal to a specified value, or for when a generalized expression becomes true.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

**Syntax**

```
```

**Description**

If at least one match is found, it returns the time (and, optionally, delta) at which the last match occurred and the number of matches found, in a Tcl list:

```
{{<time>} <matchCount>}
```

where `<time>` is in the format `<number> <unit>`. If the `-deltas` option is specified, the delta of the last match is also returned:

```
{{<time>} <delta> <matchCount>}
```

If no matches are found, a TCL_ERROR is returned. If one or more matches are found, but less than the number requested, it is not considered an error condition, and the time of the farthest match is returned, with the count of the matches found.

**Arguments**

- `-count <n>`
  
  (optional) Specifies to search for the nth occurrence of the match condition.
  
  `<n>` — Any positive integer.

- `-deltas`
  
  (optional) Indicates to test for a match on simulation delta cycles. Otherwise, matches are only tested for at the end of each simulation time step.

- `-endtime <time> [<unit>]`
  
  (optional) Specifies the simulation time at which to start the search. By default there is no end time specified.

  `<time>` — Specified as an integer or decimal number. Current simulation units are the default unless specifying `<unit>`.

  `<unit>` — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting `<unit>`. Valid VHDL time units are: fs, ps,
Commands

**searchlog**

- **ns, us, ms, sec, min, and hr.** If <unit> is specified, you must enclose <time> and <unit> within curly braces ({}).

- **-env <path>**

  (optional) Specifies a design region in which to look for the signal names.

  - **<path>** — A path to a design region. Wildcards not allowed.

- **-expr {<expr>}**

  (optional) Specifies a search for a general expression of signal values and simulation time. **searchlog** will search until the expression evaluates to true.

  - **{<expr>}** — An expression that evaluates to a boolean true. See GUI_expression_format for the format of the expression.

- **-reverse**

  (optional) Specifies to search backwards in time from **<startTime>**.

- **-rising**

  (optional) Specifies a search for rising edge on a scalar signal. This option is ignored for compound signals.

- **-falling**

  (optional) Specifies a search for falling edge on a scalar signal. This option is ignored for compound signals.

- **-anyedge**

  (optional) Specifies a search for a rising or falling edge on a scalar signal. This option is ignored for compound signals. (default)

- **-startDelta <num>**

  (optional) Indicates a simulation delta cycle on which to start.

  - **<num>** — Any positive integer.

- **-value <string>**

  (optional) Specifies a match of a single scalar or compound signal against a specified string.

  - **<string>** — Specifies a string to be matched.

- **<startTime> [unit]**

  (required) Specifies the simulation time at which to start the search. The time is specified as an integer or decimal number. Must be placed immediately before the **<pattern>** argument.

  - **<unit>** — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting <unit>. Valid VHDL time units are: fs, ps, ns, us, ms, sec, min, and hr. If <unit> is specified, you must enclose <time> and <unit> within curly braces ({}).
• <pattern>

(Required unless the -expr argument is used.) Specifies one or more signal names or wildcard patterns of signal names to search on. Must be specified as the final argument to the searchlog command.

Related Topics

• virtual signal
• virtual log
• virtual nolog
• GUI_expression_format
see

This command displays the specified number of source file lines around the current execution line and places a marker to indicate the current execution line. If specified without arguments, five lines will be displayed before and four lines after.

Syntax

see [<n> | <pre> <post>]

Arguments

- `<n>`
  (optional) Designates the number of lines to display before and after the current execution line.
- `<pre>`
  (optional) Designates the number of lines to display before the current execution line.
- `<post>`
  (optional) Designates the number of lines to display after the current execution line.

Example

- Display 2 lines before and 5 lines after the current execution line.
  ```
  see 2 5
  ```

Returns:

```
#   92 :
#   93 :           if (verbose) $display("Read/Write test done");
# ->94 :               $stop(1);
#   95 :          end
#   96 :         end
#   97 :
#   98 :     or2 i1 (
#   99 :         .y(t_set),
```

Arguments to this command are order dependent. Please read the argument descriptions for more information. Must be specified as the second argument to the `seetime` command.
**setenv**

This command changes or reports the current value of an environment variable. The setting is valid only for the current ModelSim session.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

**Syntax**

```
setenv <varname> [<value>]
```

**Arguments**

- **<varname>**
  
  (required) The name of the environment variable you wish to set or check. Must be specified as the first argument to the `setenv` command.

- **<value>**
  
  (optional) The new value for `<varname>`. If you do not specify a value, ModelSim reports the variable’s current value.

**Related Topics**

- `unsetenv`
- `printenv`
shift

This command shifts macro parameter values left one place, so that the value of parameter \$2 is assigned to parameter \$1, the value of parameter \$3 is assigned to \$2, and so on. The previous value of \$1 is discarded.

The `shift` command and macro parameters are used in macro files. If a macro file requires more than nine parameters, they can be accessed using the `shift` command.

To determine the current number of macro parameters, use the `argc` variable.

**Syntax**

```
shift
```

**Arguments**

- None

**Description**

For a macro file containing nine macro parameters defined as \$1 to \$9, one `shift` command shifts all parameter values one place to the left. If more than nine parameters are named, the value of the tenth parameter becomes the value of \$9 and can be accessed from within the macro file.

**Related Topics**

- `do`
show

This command lists HDL objects and subregions visible from the current environment. The objects listed include:

- **VHDL** — signals, processes, constants, variables, and instances.
- **Verilog** — nets, registers, tasks, functions, instances, variables, and memories.

The `show` command returns formatted results to stdout. To eliminate formatting (to use the output in a Tcl script), use the `Show` form of the command instead.

**Syntax**

```
show [-all] [<pathname>]
```

**Arguments**

- `-all`
  (optional) Displays all names at and below the specified path recursively.
- `<pathname>`
  (optional) Specifies the pathname of the environment for which you want the objects and subregions to be listed; if omitted, the current environment is assumed.

**Examples**

- List the names of all the objects and subregion environments visible in the current environment.
  
  ```
  show
  ```

- List the names of all the objects and subregions visible in the environment named `/uut`.
  
  ```
  show /uut
  ```

- List the names of all the objects and subregions visible in the environment named `sub_region` which is directly visible in the current environment.
  
  ```
  show sub_region
  ```

**Related Topics**

- `environment`
- `find`
simstats

This command returns performance-related statistics about elaboration and simulation. The statistics measure the simulation kernel process (vsimk) for a single invocation of vsim. If you invoke vsim a second time, or restart the simulation, the current statistics are discarded and new values are collected.

If executed without arguments, the command returns a list of pairs similar to the following:

```
{{elab memory} 0} {{elab working set} 7245824} {{elab time} 0.942645}
{{elab cpu time} 0.190274} {{elab context} 0} {{elab page faults} 1549}
{memory 0} {working set 0} {time 0} {cpu time 0} {context 0}
{page faults} 0
```

The elaboration statistics are measured one time at the end of elaboration. The simulation memory statistics are measured at the time you invoke `simstats`. The simulation time statistics are updated at the end of each `run` command. See the arguments below for descriptions of each statistic.

Units for time values are in seconds. Units for memory values vary by platform:

- For SunOS and Linux, the memory size is reported in Kbytes
- For Windows, the memory size is reported in bytes.

Some of the values may not be available on all platforms and other values may be approximates. Different operating systems report these numbers differently.

Syntax

```
simstats [memory | working | time | cpu | context | faults]
```

Arguments

- **memory**
  (optional) Returns the amount of virtual memory that the OS has allocated for vsimk.

- **working**
  (optional) Returns the portion of allocated virtual memory that is currently being used by vsimk. If this number exceeds the actual memory size, you will encounter performance degradation.

- **time**
  (optional) Returns the cumulative "wall clock time" of all run commands.

- **cpu**
  (optional) Returns the cumulative processor time of all run commands. Processor time differs from wall clock time in that processor time is only counted when the cpu is actually running vsimk. If vsimk is swapped out for another process, cpu time does not increase.
• context
  (optional) Returns the number of context swaps (vsimk being swapped out for another process) that occurred during all run commands.

• faults
  (optional) Returns the number of page faults that occurred during all run commands.
status

This command lists summary information about currently interrupted macros. If invoked without arguments, the command lists the filename of each interrupted macro, the line number at which it was interrupted, and prints the command itself. It also displays any onbreak or onerror commands that have been defined for each interrupted macro.

Syntax

status [file | line]

Arguments

- file
  (optional) Reports the file pathname of the current macro.
- line
  (optional) Reports the line number of the current macro.

Examples

The transcript below contains examples of resume, and status commands.

```
VSIM(paused)> status
# Macro resume_test.do at line 3 (Current macro)
#     command executing: "pause"
#     is Interrupted
#     ONBREAK commands: "resume"
# Macro startup.do at line 34
#     command executing: "run 1000"
#     is Interrupted
#     ONBREAK commands: "resume"
VSIM(paused)> resume
# Resuming execution of macro resume_test.do at line 4
```

Related Topics

- abort
- do
- pause
- resume
**step**

The **step** command steps to the next HDL or C statement. Current values of local HDL variables may be observed at this time using the Locals window.

You can use the `-over` argument to skip over a VHDL procedures or functions, Verilog task or functions, or a C functions. When a wait statement or end of process is encountered, time advances to the next scheduled activity. ModelSim then updates the Process and Source windows to reflect the next activity.

### Syntax

```
step [ <n> ] [-inst <full_path_name>] [-out] [-over [ <n> ]] [-this "this==<class_handle>"]
```

### Arguments

- `<n>`
  
  (optional) Instructs the simulation to execute ‘n’ steps before returning, where `<n>` is any positive integer.

- `-inst <full_path_name>
  
  (optional) Instructs the simulation to step into a specific instance, process, or thread.

  `<full_path_name>` — Specifies the full path to an instance, process or thread.

- `-out
  
  (optional) Instructs the simulation to step out of the current function or procedure and return to the caller.

- `-over [ <n> ]
  
  (optional) Directs ModelSim to run VHDL procedures and functions, Verilog tasks and functions but to treat them as simple statements instead of entering and tracing them line by line.

  `<n>` — Moves the debugger n lines ahead. Specified as a positive integer.

- `-this "this==<class_handle>"
  
  (optional) Instructs the simulation to step into a System Verilog class. To obtain the handle of the class, use the `examine` -handle command.

  `<class_handle>` — Specifies a System Verilog class. Note that you must use quotation marks (") with this argument.

### Related Topics

- `run`
stop

This command is used with the when command to stop simulation in batch files. The stop command has the same effect as hitting a breakpoint. The stop command may be placed anywhere within the body of the when command.

Syntax

stop

Arguments

• None.

Description

Use run -continue to continue the simulation run, or the resume command to continue macro execution. If you want macro execution to resume automatically, put the resume command at the top of your macro file:

    onbreak {resume}

Note

If you want to stop the simulation using a when command, you must use a stop command within your when statement. DO NOT use an exit command or a quit command. The stop command acts like a breakpoint at the time it is evaluated.

Related Topics

• bp
• resume
• run
• when
**suppress**

This command prevents one or more specified messages from displaying. You cannot suppress Fatal or Internal messages. The `suppress` command used without arguments returns the message numbers of all suppressed messages.

Edit the `suppress` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

**Syntax**

```
suppress [-clear <msg_number>[,<msg_number>,...]] [<msg_number>[,<msg_number>,...]]
        [<code_string>[, <code_string>,...]]
```

**Arguments**

- `-clear <msg_number>[,<msg_number>,...]`
  (optional) Clears suppression of one or more messages identified by message number.
  
  `<msg_number>` — A number identifying the message. Multiple message numbers are specified as a comma separated list.

- `<msg_number>[,<msg_number>,...]`
  (optional) A number identifying the message to be suppressed. Multiple message numbers are specified as a comma separated list.

- `<code_string>[, <code_string>,...]`
  (optional) A string identifier of the message to be suppressed. Disables warning messages in the category specified by `<CODE>`. Warnings that can be disabled include the `<CODE>` name in square brackets in the warning message.

**Examples**

- Return the message numbers of all suppressed messages:
  ```
suppress
  ```

- Suppress messages by message number:
  ```
suppress 8241,8242,8243,8446,8447
  ```

- Suppress messages by numbers and code categories:
  ```
suppress 8241,TFMPC,CNNODP,8446,8447
  ```

- Clear message suppression for the designated messages:
  ```
suppress -clear 8241,8242
  ```

- Return the message numbers of all suppressed messages and clear suppression for all:
  ```
suppress -clear [suppress]
  ```
This (traceback) command (traceback) displays a stack trace for the current process in the Transcript window. This lists the sequence of HDL function calls that have been entered to arrive at the current state for the active process.

**Syntax**

```
tb
```

**Arguments**

- None
**Time**

These commands allow you to perform comparisons between, operations on, and conversions of, time values.

When [unit] is left unspecified the commands assume the current simulation time unit, as defined by the Resolution variable in the modelsim.ini file or the vsim -t command. Units of time (ns, us, and so forth) can be specified independently for each <time[1 | 2]> specified for most of the commands. See the description of each command and examples for more information.

Arguments to this command are order dependent. Follow the order specified in the Syntax for each command.

**Syntax**

- eqTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> and <time2> are equal.

- neqTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> and <time2> are not equal.

- ltTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> is less than <time2>.

- gtTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> is greater than <time2>.

- lteTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> is less than or equal to <time2>.

- gteTime <time1>[unit] <time2>[unit]
  - Returns a 1 (true) or 0 (false) if <time1> is greater than or equal to <time2>.

- addTime <time1>[unit] <time2>[unit]
  - Returns the sum of adding <time1> to <time2>

- subTime <time1>[unit] <time2>[unit]
  - Returns the value of subtracting <time2> from <time1>

- mulTime <time1>[unit] <integer>
  - Returns the value of multiplying <time1> by an <integer>

- divTime <time1>[unit] <time2>[unit]
  - Returns an integer, that is the value of dividing <time1> by <time2>. Specifying 0 for <time2> results in an error.

- intToTime <high_32bit_int> <low_32bit_int>
Returns a 64-bit time value based on two 32-bit parts of a 64-bit integer. This command is useful when you’ve performed an integer calculation that results in a 64-bit value and need to convert it to a time unit.

**scaleTime** `<time1>[unit] <scale_factor>`

Returns a time value scaled by a real number and truncated to the current time resolution.

**RealToTime** `<real>`

Returns a time value equivalent to the specified real number and truncated to the current time resolution.

**validTime** `<time>`

Returns a 1 (true) or 0 (false) if the given string is a valid time for use with any of these Time calculations.

**formatTime** `{+ | -} commas | {+ | -}nodefunit | {+ | -}bestunits`

Sets display properties for time values.

**Arguments**

- `<time1>[unit] ...`
  - `<time>` — Specified as an integer or decimal number. Current simulation units are the default unless specifying `<unit>`.
  - `<unit>` — (optional) A suffix specifying a unit of time where the default is to specify the current simulation resolution by omitting `<unit>`. Valid VHDL time units are:
    - fs — femtosecond (10\(^{-15}\) seconds)
    - ps — picosecond (10\(^{-12}\) seconds)
    - ns — nanosecond (10\(^{-9}\) seconds)
    - us — microsecond (10\(^{-6}\) seconds)
    - ms — millisecond (10\(^{-3}\) seconds)
    - sec — second
    - min — minute (60 seconds)
    - hr — hour (3600 seconds)
  - Note that if you put a space between the values, you must enclose the argument in braces ({} ) or double-quotes (" " ).
- `<high_32bit_int> | <low_32bit_int>`
  - `<high_32bit_int>` — The “high” part of the 64-bit integer.
  - `<low_32bit_int>` — The “low” part of the 64-bit integer.
- `<scale_factor>` — a real number to be used as scaling factor. Common values can include:
  - 0.25, 0.5, 1.5, 2, 10, 100
• \{+ | -\} commas — controls whether commas are displayed in time values.
  +commas — time values include commas
  -commas — time values do not include commas

• \{+ | -\}nodefunit — controls whether time values display time units
  +nodefunit — time values do not include time units and will be in current time
  resolution
  -nodefunit — time values may include time units

• \{+ | -\}bestunits — controls whether time values display the largest possible time unit, for example 8 us instead of 8,000 ns.
  +bestunits — time values display the largest possible time unit
  -bestunits — time values display the default time unit

Examples

>ltTime 100ns 1ms
Returns:
  # 1

>addTime \{1545 ns\} \{455 ns\}
Returns:
  # 2 us

>gteTime "1000 ns" "1 us"
Returns:
  # 1

>divTime 1us 10ns
Returns:
  # 100

>formatTime +bestunit
Returns:
  # -commas -nodefunit +bestunits

>scaleTime 3ms 1000
Returns:
  # 3 sec

>RealToTime 1.345e04
Returns:
  # 13450 ns
transcript

This command controls echoing of commands executed in a macro file. If no option is specified, the current setting is reported.

Syntax

transcript [on | off | -q | quietly]

Arguments

- on
  (optional) Specifies that commands in a macro file will be echoed to the Transcript window as they are executed.

- off
  (optional) Specifies that commands in a macro file will not be echoed to the Transcript window as they are executed.

- -q
  (optional) Returns "0" if transcripting is turned off or "1" if transcripting is turned on. Useful in a Tcl conditional expression.

- quietly
  (optional) Turns off the transcript echo for all commands. To turn off echoing for individual commands see the quietly command.

Examples

- Commands within a macro file will be echoed to the Transcript window as they are executed.

  transcript on

- If issued immediately after the previous example, the message:

  transcript
  Returns
  Macro transcripting is turned ON.

Related Topics

- Transcript Window
- echo
transcript file

This command sets or queries the current PrefMain(file) Tcl preference variable. You can use this command to clear a transcript in batch mode or to limit the size of a transcript file. It offers an alternative to setting the PrefMain(file) Tcl preference variable through the GUI.

Syntax

transcript file [<filename>]

Arguments

- `<filename>`
  
  (optional) Specifies the filename for the transcript file. If you specify a new file, the existing transcript file is closed and a new transcript file opened. If you specify an empty string (""), the existing file is closed and no new file is opened. If you don’t specify this argument, the current filename is returned.

Note

You can prevent overwriting older transcript files by including a pound sign (#) in `<filename>` when `<filename>` is a repeated string. The simulator replaces the ‘#’ character with the next available sequence number when saving a new transcript file.

Examples

- Close the current transcript file and stop writing data to the file. This is a method for reducing the size of your transcript.

  
  transcript file ""

- Close the current transcript file named `trans1.txt` and open a new transcript file, incrementing the file name by 1.

  
  transcript file trans#.txt

  Closes `trans1.txt` and opens `trans2.txt`.

- This series of commands results in the transcript containing only data from the second millisecond of the simulation. The first transcript file command closes the transcript so no data is being written to it. The second transcript file command opens a new transcript and records data from 1 ms to 2 ms.

  
  transcript file ""
  run 1 ms
  transcript file transcript
  run 1 ms
Related Topics

- "Creating a Transcript File"
- "Setting Preference Variables from the GUI"
- “Transcript Window”
- transcript path
- transcript sizelimit
**transcript path**

This command returns the full pathname to the current transcript file.

**Syntax**

transcript path

**Arguments**

- None

**Related Topics**

- "Creating a Transcript File"
- "Setting Preference Variables from the GUI"
- “Transcript Window”
- transcript file
transcript sizelimit

This command sets or queries the current preference value for the transcript fileSizeLimit value. If the size limit is reached, the transcript file is saved and simulation continues.

Syntax

transcript sizelimit [<size>]

Arguments

- <size>
  
  (optional) Specifies the size, in KB, of the transcript file where the default is 0 or unlimited. The actual file size may be larger by as much as one buffer size (usually about 4k), depending on the operating system default buffer size and the size of the messages written to the transcript.

Note

You can set the size of the transcript file with the $PrefMain (fileSizeLimit) Tcl variable in the Preferences dialog. Refer to "Setting Preference Variables from the GUI" for more information.

Related Topics

- "Creating a Transcript File"
- "Setting Preference Variables from the GUI"
- “Transcript Window”
- transcript file
tssi2mti

This command is used to convert a vector file in TSSI Format into a sequence of force and run commands.

The stimulus is written to the standard output.

The source code for tssi2mti is provided in the file tssi2mti.c in the examples directory.

Syntax

tssi2mti \textless signal\_definition\_file\textgreater  [\textless sef\_vector\_file\textgreater ]

Arguments

- \textless signal\_definition\_file\textgreater 
  (required) Specifies the name of the TSSI signal definition file describing the format and content of the vectors.

- \textless sef\_vector\_file\textgreater 
  (optional) Specifies the name of the file containing vectors to be converted. If none is specified, standard input is used.

Examples

- The command will produce a do file named \textit{trigger.do} from the signal definition file \textit{trigger.def} and the vector file \textit{trigger.sef}.
  
  \texttt{tssi2mti trigger.def trigger.sef > trigger.do}

- This example is the same as the previous one, but uses the standard input instead.
  
  \texttt{tssi2mti trigger.def < trigger.sef > trigger.do}

Related Topics

- force
- run
- write tssi
ui_VVMode

This command specifies behavior when encountering UI registration calls used by verification packages, such as AVM or OVM. Returns the current setting when specifies without an argument.

Syntax

ui_VVMode [off | nolog | full]

Arguments

- **off**
  (optional) Disables context registration and automatic logging when encountering UI registration calls.
- **nolog**
  (optional) Enables the context registration of the UI registration call, but does not automatically log the registration to the WLF file. (default)
- **full**
  (optional) Enables the context registration of the UI registration call and automatically logs the registration to the WLF file.

Description

UI registration calls, Verilog system tasks specific to this product, are typically included in verification packages such as AVM and OVM so that key information about the packages is available when debugging the simulation. The UI registration calls include:

- **$ui_VVInstallInst()** — Defines a region in the context tree, which will appear in the Structure window.
- **$ui_VVInstallObj()** — Adds an object to the defined parent, which will appear in the Objects window when the parent instance is selected in the Structure window.
- **$ui_VVInstallPort()** — Adds a port that is an object that connects to another component, which will appear in the Objects window when the parent instance is selected in the Structure window.
- **$ui_VVSetFilter()** — Specifies which class properties should not be shown in the GUI.
- **$ui_VVSetAllow()** — Specifies which class properties should be retained that were filtered out with $ui_VVSetFilter.
unsetenv

This command deletes an environment variable. The deletion is not permanent – it is valid only for the current ModelSim session.

Syntax

```bash
unsetenv <varname>
```

Arguments

- `<varname>`
  (required) The name of the environment variable you wish to delete.

Related Topics

- `setenv`
- `printenv`
vcd add

This command adds the specified objects to a VCD file.

The allowed objects are Verilog nets and variables and VHDL signals of type bit, bit_vector, std_logic, and std_logic_vector (other types are silently ignored). The command works with mixed HDL designs.

All vcd add commands must be executed at the same simulation time. The specified objects are added to the VCD header and their subsequent value changes are recorded in the specified VCD file. By default all port driver changes and internal variable changes are captured in the file. You can filter the output using arguments detailed below.

Related Verilog tasks: $dumpvars, $fdumpvars

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax


<object_name> ...

Arguments

- -dumpports
  (optional) Specifies port driver changes to be added to an extended VCD file. When the vcd dumpports command cannot specify all port driver changes that will appear within the VCD file, multiple vcd add -dumpports commands can be used to specify additional port driver changes.

- -file <filename>
  (optional) Specifies the name of the VCD file. This option should be used only when you have created multiple VCD files using the vcd files command.

    <filename> — A .vcd file.

- -in
  (optional) Includes only port driver changes from ports of mode IN.

- -out
  (optional) Includes only port driver changes from ports of mode OUT.

- -inout
  (optional) Includes only port driver changes from ports of mode INOUT.

- -ports
  (optional) Includes only port driver changes. Excludes internal variable or signal changes.

- -internal
  (optional) Includes only internal variable or signal changes. Excludes port driver changes.
- `-r`  
  (optional) Specifies that signal and port selection occurs recursively into subregions. If omitted, included signals and ports are limited to the current region.

- `<object_name> ...`  
  (required) Specifies the Verilog or VHDL object or objects to add to the VCD file. Multiple objects may be specified by separating names with spaces. Wildcards are accepted. Must be specified as the final argument to the `vcd add` command.

**Related Topics**

- `vcd checkpoint`
- `vcd comment`
- `vcd dumpports`
- `vcd dumpportsall`
- `vcd dumpportsflush`
- `vcd dumpportslimit`
- `vcd dumpportsoff`
- `vcd dumpportson`
- `vcd file`

- `vcd files`
- `vcd flush`
- `vcd limit`
- `vcd off`
- `vcd on`
- `vcd2wlf`
- `DumpportsCollapse`
- `Value Change Dump (VCD) Files`
- `Verilog tasks are documented in the IEEE 1364 standard.`
**vcd checkpoint**

This command dumps the current values of all VCD variables to the specified VCD file. While simulating, only value changes are dumped.

Related Verilog tasks: $dumpall, $fdumpall

**Syntax**

vcd checkpoint [<filename>]

**Arguments**

- <filename>
  
  (optional) Specifies the name of the VCD file. If omitted the command is executed on the file designated by the vcd file command or dump.vcd if vcd file was not invoked.

**Related Topics**

- vcd add
- vcd comment
- vcd dumpports
- vcd dumpportsall
- vcd dumpportsflush
- vcd dumpportslimit
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd files
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd comment

This command inserts the specified comment in the specified VCD file.

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

vcd comment <comment string> [<filename>]

Arguments

- <comment string>  
  (required) Comment to be included in the VCD file. Must be enclosed by double quotation marks or curly braces. Must be specified as the first argument to the vcd comment command.

- <filename>  
  (optional) Specifies the name of the VCD file. If omitted the command is executed on the file designated by the vcd file command or dump.vcd if vcd file was not invoked.

Related Topics

- vcd add  
- vcd checkpoint  
- vcd dumpports  
- vcd dumpportsall  
- vcd dumpportsflush  
- vcd dumpportslimit  
- vcd dumpportsoff  
- vcd dumpportson  
- vcd file  
- vcd files  
- vcd flush  
- vcd limit  
- vcd off  
- vcd on  
- vcd2wlf  
- DumpportsCollapse  
- Value Change Dump (VCD) Files  
- Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpports

This command creates a VCD file that includes port driver data.
By default all port driver changes are captured in the file. You can filter the output using arguments detailed below. Related Verilog task: $dumpports
Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax
[-no_strength_range] [-unique] [-vcdstim] <object_name> ...

Arguments
- -compress
  (optional) Produces a compressed VCD file. ModelSim uses the gzip compression algorithm. It is not necessary to specify -compress if you specify a .gz extension with the -file <filename> argument
- -direction
  (optional) Includes driver direction data in the VCD file.
- -file <filename>
  (optional) Creates a VCD file. Defaults to the current working directory and the filename dumpports.vcd. Multiple filenames can be opened during a single simulation.
    <filename> — Specifies a filename. When specified with a .gz extension, the file is compressed.
- -force_direction
  (optional) Causes vcd dumpports to use the specified port direction (instead of driver location) to determine whether the value being dumped is input or output. This argument overrides the default use of the location of drivers on the net to determine port direction (this is because Verilog port direction is not enforced by the language or by ModelSim).
- -in
  (optional) Includes ports of mode IN.
- -out
  (optional) Includes ports of mode OUT.
- -inout
  (optional) Includes ports of mode INOUT.
• -no_strength_range
  (optional) Ignores strength ranges when resolving driver values. This argument is an extension to the IEEE 1364 specification. Refer to Resolving Values for additional information.

• -unique
  (optional) Generates unique VCD variable names for ports even if those ports are connected to the same collapsed net.

• -vcdstim
  (optional) Ensures that port name order in the VCD file matches the declaration order in the instance module or entity declaration. Refer to Port Order Issues for further information.

• <object_name> ...
  (required) Specifies one or more Verilog, VHDL, or SystemC objects to add to the VCD file. You can specify multiple objects by separating names with spaces. Wildcards are accepted. Must be specified as the final argument to the vcd dumpports command.

**Examples**

• Create a VCD file named counter.vcd of all IN ports in the region /test_design/dut/.
  
  ```
  vcd dumpports -in -file counter.vcd /test_design/dut/*
  ```

• These two commands resimulate a design from a VCD file. Refer to Simulating with Input Values from a VCD File for further details.
  
  ```
  vcd dumpports -file addern.vcd /testbench/uut/*
  vsim -vcdstim addern.vcd addern -gn=8 -do "add wave /*; run 1000"
  ```

• This series of commands creates VCD files for the instances proc and cache and then re-simulates the design using the VCD files in place of the instance source files. Refer to Replacing Instances with Output Values from a VCD File for more information.
  
  ```
  vcd dumpports -vcdstim -file proc.vcd /top/p/*
  vcd dumpports -vcdstim -file cache.vcd /top/c/*
  run 1000
  vsim top -vcdstim /top/p=proc.vcd -vcdstim /top/c=cache.vcd
  ```
Commands

vcd dumpports

Related Topics

- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpportsall
- vcd dumpportsflush
- vcd dumpportslot
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd files
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpportsall

This command creates a checkpoint in the VCD file which shows the value of all selected ports at that time in the simulation, regardless of whether the port values have changed since the last timestep.

Related Verilog task: $dumpportsall

Syntax

vcd dumpportsall [<filename>]

Arguments

- `<filename>`
  (optional) Specifies the name of the VCD file. If omitted the command is executed on all open VCD files.

Related Topics

- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpports
- vcd dumpportsflush
- vcd dumpportslimit
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd files
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpportsflush

This command flushes the contents of the VCD file buffer to the specified VCD file.
Related Verilog task: $dumpportsflush

Syntax
vcd dumpportsflush [filename]

Arguments
- filename
  (optional) Specifies the name of the VCD file. If omitted the command is executed on all open VCD files.

Related Topics
- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpports
- vcd dumpportsall
- vcd dumpportslimit
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd files
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpportslimit

This command specifies the maximum size of the VCD file (by default, limited to available disk space). When the size of the file exceeds the limit, a comment is appended to the file and VCD dumping is disabled.

Related Verilog task: $dumpportslimit

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

vcd dumpportslimit <dumplimit> [filename]

Arguments

• <dumplimit>  
  (required) Specifies the maximum VCD file size in bytes. Must be specified as the first argument to the vcd dumpportslimit command.

• <filename>  
  (optional) Specifies the name of the VCD file. If omitted the command is executed on all open VCD files.

Related Topics

• vcd add  
• vcd checkpoint  
• vcd comment  
• vcd dumpports  
• vcd dumpportsall  
• vcd dumpportsflush  
• vcd dumpportsoff  
• vcd dumpportson  
• vcd file  
• vcd files  
• vcd flush  
• vcd limit  
• vcd off  
• vcd on  
• vcd2wlf  
• DumpportsCollapse  
• Value Change Dump (VCD) Files  
• Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpportsoff

This command turns off VCD dumping and records all dumped port values as x.

Related Verilog task: $dumpportsoff

Syntax

vcd dumpportsoff [<filename>]

Arguments

• <filename>
  (optional) Specifies the name of the VCD file. If omitted the command is executed on all open VCD files.

Related Topics

• vcd add
• vcd checkpoint
• vcd comment
• vcd dumpports
• vcd dumpportsall
• vcd dumpportsflush
• vcd dumpportslimit
• vcd dumpportson
• vcd file
• vcd files
• vcd flush
• vcd limit
• vcd off
• vcd on
• vcd2wlf
• DumpportsCollapse
• Value Change Dump (VCD) Files
• Verilog tasks are documented in the IEEE 1364 standard.
vcd dumpportson

This command turns on VCD dumping and records the current values of all selected ports. This command is typically used to resume dumping after invoking vcd dumpportsoff.

Related Verilog task: $dumpportson

Syntax

vcd dumpportson [ <filename> ]

Arguments

• <filename>
  (optional) Specifies the name of the VCD file. If omitted the command is executed on all open VCD files.

Related Topics

- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpports
- vcd dumpportsall
- vcd dumpportsflush
- vcd dumpportslimit
- vcd dumpportsoff
- vcd file
- vcd files
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd file

This command specifies the filename and state mapping for the VCD file created by a vcd add command. The vcd file command is optional. If used, it must be issued before any vcd add commands.

Related Verilog task: $dumpfile

Syntax


Arguments

- **-dumpports**
  (optional) Capture detailed port driver data for Verilog ports and VHDL std_logic ports. This option works only on ports, and any subsequent vcd add command will accept only qualifying ports (silently ignoring all other specified objects).

- **-direction**
  (optional) Includes driver direction data in the VCD file.

- **<filename>**
  (optional) Specifies the name of the VCD file that is created where the default is dump.vcd.

- **-map <mapping pairs>**
  (optional) Overrides the default mappings. Affects only VHDL signals of type std_logic.

  <mapping pairs> — Specified as a list of character pairs. The first character in a pair must be one of the std_logic characters UX01ZWLH- and the second character is the character you wish to be recorded in the VCD file. The Tcl convention for command strings that include spaces is to enclose them in quotes (" "). For example, to map L and H to z:

  vcd file -map "L z H z"

- **-no_strength_range**
  (optional) Ignores strength ranges when resolving driver values. This argument is an extension to the IEEE 1364 specification. Refer to Resolving Values for additional information.

- **-nomap**
  (optional) Affects only VHDL signals of type std_logic. It specifies that the values recorded in the VCD file shall use the std_logic enumeration characters of UX01ZWLH-. This option results in a non-standard VCD file because VCD values are limited to the four state character set of x01z. By default, the std_logic characters are mapped as follows.
- **unique**
  - (optional) Generates unique VCD variable names for ports even if those ports are connected to the same collapsed net.

### Related Topics

- `vcd add`
- `vcd checkpoint`
- `vcd comment`
- `vcd dumpports`
- `vcd dumpportsall`
- `vcd dumpportsflush`
- `vcd dumpportslimit`
- `vcd dumpportsoff`
- `vcd dumpportson`
- `vcd files`
- `vcd flush`
- `vcd limit`
- `vcd off`
- `vcd on`
- `vcd2wlf`
- `DumpportsCollapse`
- `Value Change Dump (VCD) Files`
- Verilog tasks are documented in the IEEE 1364 standard.
**vcd files**

This command specifies filenames and state mapping for VCD files created by the `vcd add` command. The `vcd files` command is optional. If used, it must be issued before any `vcd add` commands.

Related Verilog task: `$fdumpfile`

**Syntax**

```
```

**Arguments**

- **-compress**
  
  (optional) Produces a compressed VCD file. ModelSim uses the gzip compression algorithm. If you specify a `.gz` extension on the `-file <filename>` argument, ModelSim compresses the file even if you don’t use the `-compress` argument.

- **-direction**
  
  (optional) Includes driver direction data in the VCD file.

- **<filename>**
  
  (required) Specifies the name of a VCD file to create. Multiple files can be opened during a single simulation; however, you can create only one file at a time. If you want to create multiple files, invoke `vcd files` multiple times.

- **-map <mapping pairs>**
  
  (optional) Overrides the default mappings. Affects only VHDL signals of type std_logic.

    `<mapping pairs>` — Specified as a list of character pairs. The first character in a pair must be one of the std_logic characters UX01ZWLH- and the second character is the character you wish to be recorded in the VCD file. The Tcl convention for command strings that include spaces is to enclose them in quotes (" "). For example, to map L and H to z:

    ```
    vcd file -map "L z H z"
    ```

- **-no_strength_range**
  
  (optional) Ignores strength ranges when resolving driver values. This argument is an extension to the IEEE 1364 specification. Refer to “Resolving Values” for additional information.

- **-nomap**
  
  (optional) Affects only VHDL signals of type std_logic. It specifies that the values recorded in the VCD file shall use the std_logic enumeration characters of UX01ZWLH-. This option...
results in a non-standard VCD file because VCD values are limited to the four state character set of x01z. By default, the std_logic characters are mapped as follows.

<table>
<thead>
<tr>
<th>VHDL</th>
<th>VCD</th>
<th>VHDL</th>
<th>VCD</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>x</td>
<td>W</td>
<td>x</td>
</tr>
<tr>
<td>X</td>
<td>x</td>
<td>L</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>H</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>-</td>
<td>x</td>
</tr>
<tr>
<td>Z</td>
<td>z</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- unique
  (optional) Generates unique VCD variable names for ports even if those ports are connected to the same collapsed net.

**Examples**

The following example shows how to "mask" outputs from a VCD file until a certain time after the start of the simulation. The example uses two vcd files commands and the vcd on and vcd off commands to accomplish this task.

```
vcd files in_inout.vcd
vcd files output.vcd
vcd add -in -inout -file in_inout.vcd /*
vcd add -out -file output.vcd /*
vcd off output.vcd
run 1us
vcd on output.vcd
run -all
```

**Related Topics**

- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpports
- vcd dumpportsall
- vcd dumpportsflush
- vcd dumpportslimit
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd flush
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd flush

This command flushes the contents of the VCD file buffer to the specified VCD file. This command is useful if you want to create a complete VCD file without ending your current simulation.

Related Verilog tasks: $dumpflush, $fdumpflush

Syntax

vcd flush [<filename>]

Arguments

- <filename> (optional) Specifies the name of the VCD file. If omitted, the command is executed on the file designated by the vcd file command or dump.vcd if vcd file was not invoked.

Related Topics

- vcd add
- vcd checkpoint
- vcd comment
- vcd dumpports
- vcd dumpportsall
- vcd dumpportsflush
- vcd dumpportslimit
- vcd dumpportsoff
- vcd dumpportson
- vcd file
- vcd files
- vcd limit
- vcd off
- vcd on
- vcd2wlf
- DumpportsCollapse
- Value Change Dump (VCD) Files
- Verilog tasks are documented in the IEEE 1364 standard.
vcd limit

This command specifies the maximum size of a VCD file (by default, limited to available disk space).

When the size of the file exceeds the limit, a comment is appended to the file and VCD dumping is disabled.

Related Verilog tasks: $dumplimit, $fdumplimit

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

vcd limit <filesize> [ <filename> ]

Arguments

• <filesize>  
  (Required) Specifies the maximum VCD file size, in bytes. The numerical value of <filesize> can only be a whole number. Must be specified as the first argument to the vcd limit command.

  You can specify a unit of Kb, Mb, or Gb with the numerical value (units are case insensitive). Do not insert a space between the numerical value and the unit (for example, 400Mb, not 400 Mb).

• <filename>  
  (Optional) Specifies the name of the VCD file. If omitted, the command is executed on the file designated by the vcd file command or dump.vcd if vcd file was not invoked.

Example

• Specify a maximum VCD file size of 6 gigabytes and a VCD file named my_vcd_file.vcd.

  vcd limit 6gb my_vcd_file.vcd

Related Topics

• vcd add  
  • vcd checkdoint  
  • vcd comment  
  • vcd dumpports  
  • vcd dumpportsall  
  • vcd dumpportsflush  
  • vcd dumpportslimit  
  • vcd dumpportsoff  
  • vcd dumpportson  
  • vcd file  
  • vcd files  
  • vcd flush  
  • vcd off  
  • vcd on  
  • vcd2wlf  
  • DumpportsCollapse  
  • Value Change Dump (VCD) Files  
  • Verilog tasks are documented in the IEEE 1364 standard.
vcd off

This command turns off VCD dumping to the specified file and records all VCD variable values as x.

Related Verilog tasks: $dumpoff, $fdumpoff

Syntax
vcd off [<filename>]

Arguments
• <filename>  
  (optional) Specifies the name of the VCD file. If omitted, the command is executed on the file designated by the vcd file command or dump.vcd if vcd file was not invoked.

Related Topics
• vcd add
• vcd checkpoint
• vcd comment
• vcd dumpports
• vcd dumpportsall
• vcd dumpportsflush
• vcd dumpportslimit
• vcd dumpportsoff
• vcd dumpportson
• vcd file
• vcd files
• vcd flush
• vcd limit
• vcd on
• vcd2wlf
• DumpportsCollapse
• Value Change Dump (VCD) Files
• Verilog tasks are documented in the IEEE 1364 standard.
vcd on

This command turns on VCD dumping to the specified file and records the current values of all VCD variables.

By default, `vcd on` is automatically performed at the end of the simulation time that the `vcd add` command performed.

Related Verilog tasks: `$dumpon`, `$fdumpon`

Syntax

```
vcd on [<filename>]
```

Arguments

- `<filename>`
  - (optional) Specifies the name of the VCD file. If omitted the command is executed on the file designated by the `vcd file` command or `dump.vcd` if `vcd file` was not invoked.

Related Topics

- `vcd add`
- `vcd checkpoint`
- `vcd comment`
- `vcd dummports`
- `vcd dummportsall`
- `vcd dummportflush`
- `vcd dummportslimit`
- `vcd dummportsoff`
- `vcd dummportson`
- `vcd file`
- `vcd files`
- `vcd flush`
- `vcd limit`
- `vcd off`
- `vcd2wlf`
- `DumpportsCollapse`
- `Value Change Dump (VCD) Files`
- Verilog tasks are documented in the IEEE 1364 standard.
vcd2wlf

This command is a utility that translates a VCD (Value Change Dump) file into a WLF file that you can display in ModelSim using the `vsim -view` argument. This command only works on VCD files containing positive time values.

Description

The `vcd2wlf` command functions as simple one-pass converter. If you are defining a bus in a VCD file, you must specify all bus bits before the next $scope or $upscope statement appears in the file. The best way to ensure that bits get converted together as a bus is to declare them on consecutive lines.

For example:

Line 21 : $var wire 1 $ in [2] $end
Line 22 : $var wire 1 $u in [1] $end
Line 23 : $var wire 1 # in [0] $end

Arguments to this command are order dependent. Please read the argument descriptions for more information.

Syntax

```
```

Arguments

- `-splitio`
  (optional) Specifies that extended VCD port values are to be split into their corresponding input and output components by creating two signals instead of just one in the resulting .wlf file. By default the new input-component signal keeps the same name as the original port name while the output-component name is the original name with "__o" appended to it.

- `-splitio_in_ext <extension>`
  (optional) Adds an extension to input-component signal names created by using `-splitio`.

- `<extension>` — Specifies a string.

- `-splitio_out_ext <extension>`
  (optional) Adds an extension to output-component signal names created by using `-splitio`.

- `<extension>` — Specifies a string.

- `-nocase`
  (optional) Converts all alphabetic identifiers to lowercase.

- `<vcd filename>`
  (required) Specifies the name of the VCD file you want to translate into a WLF file. Must be specified immediately preceding the `<wlf filename>` argument to the `vcd2wlf` command.
• `<wlf filename>`
  (required) Specifies the name of the output WLF file. Must be specified as the final argument to the `vcd2wlf` command.

Related Topics

- `vcd add`
- `vcd checkpoint`
- `vcd comment`
- `vcd dumpports`
- `vcd dumpportsall`
- `vcd dumpportsflush`
- `vcd dumpportslimit`
- `vcd dumpportsoff`
- `vcd dumpportson`
- `vcd file`

- `vcd files`
- `vcd flush`
- `vcd limit`
- `vcd off`
- `vcd on`
- `DumpportsCollapse`
- `Value Change Dump (VCD) Files`
- Verilog tasks are documented in the IEEE 1364 standard.
vcom

The **vcom** command compiles VHDL source code into a specified working library (or to the **work** library by default).

You can invoke **vcom** either from within ModelSim or from the command prompt of your operating system. You can invoke this command during simulation.

Compiled libraries are dependent on the major version of ModelSim. When moving between major versions, you must refresh compiled libraries using the **-refresh** argument to **vcom**. This is not required for minor versions (letter releases).

All arguments to the **vcom** command are case-sensitive. For example, **-WORK** and **-work** are not equivalent.

**Syntax**

```
vcom [options] <filename> [ <filename> ... ]
```

**[options]:**

- **[-87]** [**[-93]**] [**[-2002]**] [**[-2008]**]
- [**-allowProtectedBeforeBody**]
  - **[-amsstd]** [**[-noamsstd]**]
- [**-bindAtCompile**] [**-bindAtLoad**]
- [**-check_synthesis**]
- [**-debugVA**] [**-deferSubpgmCheck**] [**-noDeferSubpgmCheck**] [**-dpiforceheader**]
- [**-error <msg_number>,[<msg_number>,…] [**[-explicit]**]
- [**-f <filename>**] [**-fatal <msg_number>,[<msg_number>,…] [**[-fsmimplicittrans]**] [**[-fsmresettrans]**] [**[-nofsmresettrans]**]
- [**[-fsmsingle]**] [**[-nofsmsingle]**] [**[-fsmverbose [b | t | w]]**] [**[-force_refresh <design_unit>]**]
- [**-gen_xml <design_unit> <filename>**]
- [**-help**]
- [**-ignoredefaultbinding**] [**-ignorevitalerrors**]
- [**-just abcep**]
- [**-line <number>**] [**-lint**]
- [**-mixedsvvh [b | 1 | r | i]**] [**-modelsimini <ini_filepath>**]
- [**-no1164**] [**-noaccel <package_name>**] [**-nocasestaticerror**] [**-nocheck**]
  - [**-nodbgsym**] [**-noindexcheck**] [**-nofsmxassign**] [**-nologo**]
  - [**-nonstddriverinit**] [**-nothersstaticerror**]
  - [**-note <msg_number>,[<msg_number>,…]**] [**-novital**] [**-novitalcheck**]
  - [**-nowarn <category_number>**]
```
[-pedanticerrors] [-performdefaultbinding]

[-quiet]
[-rangecheck | -norangecheck] [-refresh]
[-s] [-skip abcep] [-source] [-suppress <msg_number>[,<msg_number>,...]]
[-time]
[-version] [-vmake]
[-warning <msg_number>[,<msg_number>,...]] [-work <library_name>]

Arguments

- **-87**
  Disables support for VHDL-1993 and 2002. Optional. Default is -2002. See additional discussion in the examples. You can modify the VHDL93 variable in the modelsim.ini file to set this permanently (Refer to modelsim.ini Variables).

- **-93**

- **-2002**
  Specifies that the compiler is to support VHDL-2002. Optional. This is the default.

- **-2008**

- **-allowProtectedBeforeBody**
  Allows a variable of a protected type to be created prior to declaring the body. Optional.

- **-amsstd | -noamsstd**
  Specifies whether vcom adds the declaration of REAL_VECTOR to the STANDARD package. This is useful for designers using VHDL-AMS to test digital parts of their model.

  - amsstd — REAL_VECTOR is included in STANDARD.
  - noamsstd — REAL_VECTOR is not included in STANDARD (default).

  You can also control this with the AmsStandard variable or the MGC_AMS_HOME environment variable.

- **-bindAtCompile**
  Forces ModelSim to perform default binding at compile time rather than at load time. Optional. Refer to “Default Binding” for more information. You can change the permanent default by editing the BindAtCompile variable in the modelsim.ini.
• **-bindAtLoad**
  Forces ModelSim to perform default binding at load time rather than at compile time. Optional. Default.

• **-check_synthesis**
  Turns on limited synthesis rule compliance checking. Specifically, it checks to see that signals read by a process are in the sensitivity list. Optional. The checks understand only combinational logic, not clocked logic. Edit the `CheckSynthesis` variable in the `modelsim.ini` file to set a permanent default.

• **-debugVA**
  Prints a confirmation if a VITAL cell was optimized, or an explanation of why it was not, during VITAL level-1 acceleration. Optional.

• **-deferSubpgmCheck**
  Forces the compiler to report array indexing and length errors as warnings (instead of as errors) when encountered within subprograms. Subprograms with indexing and length errors that are invoked during simulation cause the simulator to report errors, which can potentially slow down simulation because of additional checking.

• **-dpiforceheader**
  Forces the generation of a DPI header file even if it will be empty of function prototypes.

• **-error <msg_number>[,<msg_number>,…]**
  Changes the severity level of the specified message(s) to "error." Optional. Edit the `error` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

• **-explicit**
  Directs the compiler to resolve ambiguous function overloading by favoring the explicit function definition over the implicit function definition. Optional. Strictly speaking, this behavior does not match the VHDL standard. However, the majority of EDA tools choose explicit operators over implicit operators. Using this switch makes ModelSim compatible with common industry practice.

• **-f <filename>**
  Refer to the section "Argument Files" for more information.

• **-fatal <msg_number>[,<msg_number>,…]**
  Changes the severity level of the specified message(s) to "fatal." Optional. Edit the `fatal` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.
• `fsmimplicittrans`
  Enables recognition of implied same state transitions. Optional.

• `fsmresettrans`
  Enables recognition of implicit asynchronous reset transitions. Optional. This includes asynchronous reset transitions in coverage results.

• `fsmsingle`
  Enables recognition FSMs having single bit current state variable. Optional.

• `fsmverbose [b | t | w]`
  Provides information about FSMs detected, including state reachability analysis. Optional.
  - `b` — displays only basic information.
  - `t` — displays a transition table in addition to the basic information.
  - `w` — displays any warning messages in addition to the basic information.

  When you do not specify an argument, this switch reports all information similar to:

  ```
  # ** Note: (vcom-1947)   FSM RECOGNITION INFO
  # Fsm detected in : ../fpu/rtl/vhdl/serial_mul.vhd
  # Current State Variable : s_state :
  #   ../fpu/rtl/vhdl/serial_mul.vhd(76)
  # Clock : clk_i
  # Reset States are: { waiting , busy }
  # State Set is : { busy , waiting }
  # Transition table is
  # -------------------------------------------
  #   busy   =>   waiting Line : (114 => 114)
  #   busy   =>   busy Line : (111 => 111)
  #   waiting =>   waiting Line : (120 => 120) (114 => 114)
  #   waiting =>   busy Line : (111 => 111)
  # -------------------------------------------
  
  When you do not specify this switch, you will receive a message similar to:

  ```
  # ** Note: (vcom-143) Detected '1' FSM/s in design unit 'serial_mul.rtl'.
  ```

• `force_refresh <design_unit>`
  Forcs the refresh of all specified design units. Optional. By default, the work library is updated; use `-work <library_name>`, in conjunction with `-force_refresh`, to update a different library (for example, vcom -work <your_lib_name> -force_refresh).

  When the compiler refreshes a design unit, it checks each dependency to ensure its source has not been changed and recompiled. Sometimes the dependency checking algorithm changes from release to release. This can lead to false errors during the integrity checks performed by the `-refresh` argument. An example of such a message follows:

  ** Error: (vsim-13) Recompile /u/test/dware/dware_61ebeta.dwpackages because /home/users/questasim/linux/../synopsys.attributes has changed.

  The `-force_refresh` argument forces the refresh of the design unit, overriding any dependency checking errors encountered by the `-refresh` argument.
A more conservative approach to working around `-refresh` dependency checks is to recompile the source code, if it is available.

- `-gen_xml <design_unit> <filename>`
  Produces an XML-tagged file containing the interface definition of the specified entity. Optional. This option requires a two-step process where you must 1) compile `<filename>` into a library with `vcom` (without `-gen_xml`) then 2) execute `vcom` with the `-gen_xml` switch, for example:
  
  ```
  vlib work
  vcom counter.vhd
  vcom -gen_xml counter counter.xml
  ```

- `-help`
  Displays the command’s options and arguments. Optional.

- `-ignoredefaultbinding`
  Instructs the compiler not to generate a default binding during compilation. Optional. You must explicitly bind all components in the design to use this switch.

- `-ignorevitalerrors`
  Directs the compiler to ignore VITAL compliance errors. Optional. The compiler still reports that VITAL errors exist, but it will not stop the compilation. You should exercise caution in using this switch; as part of accelerating VITAL packages, we assume that compliance checking has passed.

- `-just abcep`
  Directs the compiler to include only the following:
  
  a — architectures
  b — bodies
  c — configurations
  e — entities
  p — packages
  
  Any combination in any order can be used, but you must specify at least one choice if you use this optional switch.

- `-line <number>`
  Starts the compiler on the specified line in the VHDL source file. Optional. By default, the compiler starts at the beginning of the file.

- `-lint`
  (optional) Performs additional static checks on case statement rules and enables warning messages for the following situations:
  
  o  The result of the built-in concatenation operator ("&") is the actual for a subprogram formal parameter of an unconstrained array type.
- If you specify the -BindAtCompile switch with vcom, the entity to which a component instantiation is bound has a port that is not on the component, and for which there is no error otherwise.

- A direct recursive subprogram call.

- In cases involving class SIGNAL formal parameters, as described in the IEEE Standard VHDL Language Reference Manual entitled "Signal parameters". This check only applies to designs compiled using -87. If you compile using -93, it would be flagged as a warning or error, even without the -lint argument. Can also be enabled using the Show_Lint variable in the modelsim.ini file.

- mixedsvvh [b | l | r | i]
  Facilitates using VHDL packages at the SystemVerilog-VHDL boundary of a mixed-language design. When you compile a VHDL package with -mixedsvvh, the package can be included in a SystemVerilog design as if it were defined in SystemVerilog itself. Optional.

  b — treats all scalars and vectors in the package as SystemVerilog bit type
  l — treats all scalars and vectors in the package as SystemVerilog logic type
  r — treats all scalars and vectors in the package as SystemVerilog reg type
  i — ignores the range specified with VHDL integer types

- modelsimini <ini_filepath>
  Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (/).

- no1164
  Causes the source files to be compiled without taking advantage of the built-in version of the IEEE std_logic_1164 package. Optional. This will typically result in longer simulation times for VHDL programs that use variables and signals of type std_logic.

- noaccel <package_name>
  Turns off acceleration of the specified package in the source code using that package.

- nocasestaticerror
  Suppresses case statement static warnings. Optional. VHDL standards require that case statement alternative choices be static at compile time. However, some expressions which are globally static are allowed. This switch prevents the compiler from warning on such expressions. If the -pedanticerrors switch is specified, this switch is ignored.

- nocheck
  Disables index and range checks. Optional. You can disable these individually using the -noindexcheck and -norangecheck arguments, respectively.
• **-nodbgsym**
  Disables the generation of the symbols debugging database in the compiled library.
  
  The symbols debugging database is the `.dbs` file in the compiled library that provides information to the GUI allowing you to view detailed information about design objects at the source level. Two major GUI features that use this database include source window annotation and textual dataflow.
  
  You should only specify this switch if you know that anyone using the library will not require this information for design analysis purposes.

• **-noDeferSubpgmCheck**
  Causes range and length violations detected within subprograms to be reported as errors (instead of as warnings). As an alternative to using this argument, you can set the NoDeferSubpgmCheck property in the modelsim.ini file to a value of 1.

• **-noindexcheck**
  Disables checking on indexing expressions to determine whether indices are within declared array bounds. Optional.

• **-nofsmresettrans**
  Disables recognition of implicit asynchronous reset transitions. Optional. This has the effect of excluding asynchronous reset transitions from any coverage results.

• **-nofsmsingle**
  Disables recognition of FSMs having single bit current state variable. Optional.

• **-nofsmxassign**
  Disable recognition of FSMs containing `x` assignment. Optional.

• **-noFunctionInline**
  Turns off VHDL subprogram inlining for design units using a local copy of a VHDL package. This may be needed in case the local package has the same name as an MTI supplied package.

• **-nologo**
  Disables display of the startup banner. Optional.

• **-nonstddriverinit**
  Forces ModelSim to match pre-5.7c behavior in initializing drivers in a particular case. Optional. Prior to 5.7c, VHDL ports of mode out or inout could have incorrectly initialized drivers if the port did not have an explicit initialization value and the actual signal connected to the port had explicit initial values. Depending on a number of factors, ModelSim could incorrectly use the actual signal's initial value when initializing lower level drivers. Note that the argument does not cause all lower-level drivers to use the actual signal's initial value. It does this only in the specific cases where older versions used the actual signal's initial value.
• **-noothersstaticerror**
  Disables warnings that result from array aggregates with multiple choices having "others" clauses that are not locally static. Optional. If the **-pedanticerrors** switch is specified, this switch is ignored.

• **-norangecheck**
  Disables run time range checking. In some designs, this results in a 2X speed increase. Range checking is enabled by default or, once disabled, can be enabled using **-rangecheck**. Refer to “Range and Index Checking” for additional information.

• **-note <msg_number> [,<msg_number>, …]**
  Changes the severity level of the specified message(s) to "note." Optional. Edit the note variable in the **modelsim.ini** file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

• **-novital**
  Causes **vcom** to use VHDL code for VITAL procedures rather than the accelerated and optimized timing and primitive packages built into the simulator kernel. Optional. Allows breakpoints to be set in the VITAL behavior process and permits single stepping through the VITAL procedures to debug your model. Also all of the VITAL data can be viewed in the Locals or Objects windows.

• **-novitalcheck**
  Disables Vital level 1 checks and also Vital level 0 checks defined in section 4 of the Vital-95 Spec (IEEE Std 1076.4-1995). Optional.

• **-nowarn <category_number>**
  Selectively disables a category of warning messages. Optional. Multiple **-nowarn** switches are allowed. Warnings may be disabled for all compiles via the Main window **Compile > Compile Options** menu command or the **modelsim.ini** file (Refer to **modelsim.ini Variables**).

The warning message categories are described in **Table 2-4:**

<table>
<thead>
<tr>
<th>Category number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>unbound component</td>
</tr>
<tr>
<td>2</td>
<td>process without a wait statement</td>
</tr>
<tr>
<td>3</td>
<td>null range</td>
</tr>
<tr>
<td>4</td>
<td>no space in time literal</td>
</tr>
<tr>
<td>5</td>
<td>multiple drivers on unresolved signal</td>
</tr>
<tr>
<td>6</td>
<td>VITAL compliance checks (&quot;VitalChecks&quot; also works)</td>
</tr>
</tbody>
</table>
-pedanticerrors
Forces display of an error message (rather than a warning) on a variety of conditions. Refer to “Enforcing Strict 1076 Compliance” for a complete list of these conditions. Optional. This argument overrides -nocasestaticerror and -nothersstaticerror (see above).

-performdefaultbinding
Enables default binding when it has been disabled via the RequireConfigForAllDefaultBinding option in the modelsim.ini file. Optional.

-quiet
Disables ‘Loading’ messages. Optional.

-rangecheck
Enables run time range checking. Default. Range checking can be disabled using the -norangecheck argument. Refer to “Range and Index Checking” for additional information.

-refresh
Regenerates a library image. Optional. By default, the work library is updated. To update a different library, use -work <library_name> with -refresh (for example, vcom -work <your_lib_name> -refresh). If a dependency checking error occurs which prevents the refresh, use the vcom -force_refresh argument. See the vcom Examples for more information. You may use a specific design name with -refresh to regenerate a library image for that design, but you may not use a file name.

-s
Instructs the compiler not to load the standard package. Optional. This argument should only be used if you are compiling the standard package itself.

-skip abcep
Directs the compiler to skip all:
   a — architectures
   b — bodies

### Table 2-4. Warning Message Categories for vcom -nowarn

<table>
<thead>
<tr>
<th>Category number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>VITAL optimization messages</td>
</tr>
<tr>
<td>8</td>
<td>lint checks</td>
</tr>
<tr>
<td>9</td>
<td>signal value dependency at elaboration</td>
</tr>
<tr>
<td>10</td>
<td>VHDL-1993 constructs in VHDL-1987 code</td>
</tr>
<tr>
<td>13</td>
<td>constructs that coverage can't handle</td>
</tr>
<tr>
<td>14</td>
<td>locally static error deferred until simulation run</td>
</tr>
</tbody>
</table>
c — configurations
  e — entities
  p — packages
Any combination in any order can be used, but one choice is required if you use this optional switch.

- source
  Displays the associated line of source code before each error message that is generated during compilation. Optional. By default, only the error message is displayed.

- suppress <msg_number>,[<msg_number>,....]
  Prevents the specified message(s) from displaying. The <msg_number> is the number preceding the message you wish to suppress. Optional. You cannot suppress Fatal or Internal messages. Edit the suppress variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

- time
  Reports the "wall clock time" vcom takes to compile the design. Optional. Note that if many processes are running on the same system, wall clock time may differ greatly from the actual "cpu time" spent on vcom.

- version
  Returns the version of the compiler as used by the licensing tools. Optional.

- vmake
  Generates a complete record of all command line data and files accessed during the compile of a design. This data is then used by the vmake command to generate a comprehensive makefile for recompiling the design library. By default, vcom stores compile data needed for the -refresh switch and ignores compile data not needed for -refresh. The -vmake switch forces inclusion of all file dependencies and command line data accessed during a compile, whether they contribute data to the initial compile or not. Executing this switch can increase compile time in addition to increasing the accuracy of the compile. See the vmake command for more information.

- warning <msg_number>,[<msg_number>,....]
  Changes the severity level of the specified message(s) to "warning." Optional. Edit the warning variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

- work <library_name>
  Specifies a logical name or pathname of a library that is to be mapped to the logical library work. Optional: by default, the compiled design units are added to the work library. The specified pathname overrides the pathname specified for work in the project file.
Commands

vcom

• `<filename>`
  Specifies the name of a file containing the VHDL source to be compiled. One filename is required; multiple filenames can be entered separated by spaces or wildcards may be used (e.g., `*.vhd`).

  If you don’t specify a filename, and you are using the GUI, a dialog box pops up allowing you to select the options and enter a filename.

Examples

• Compile the VHDL source code contained in the file `example.vhd`.
  
  `vcom example.vhd`

• ModelSim supports designs that use elements conforming to the 1987, 1993, and 2002 standards. Compile the design units separately using the appropriate switches.
  
  `vcom -87 o_units1.vhd o_units2.vhd`
  `vcom -93 n_unit91.vhd n_unit92.vhd`

• When compiling source that uses the `numeric_std` package, this command turns off acceleration of the `numeric_std` package, located in the `ieee` library.
  
  `vcom -noaccel numeric_std example.vhd`

• Although it is not obvious, the `=` operator is overloaded in the `std_logic_1164` package. All enumeration data types in VHDL get an “implicit” definition for the `=` operator. So while there is no explicit `=` operator, there is an implicit one. This implicit declaration can be hidden by an explicit declaration of `=` in the same package (LRM Section 10.3). However, if another version of the `=` operator is declared in a different package than that containing the enumeration declaration, and both operators become visible through `use` clauses, neither can be used without explicit naming.
  
  `vcom -explicit example.vhd`

  To eliminate that inconvenience, the VCOM command has the `-explicit` option that allows the explicit `=` operator to hide the implicit one. Allowing the explicit declaration to hide the implicit declaration is what most VHDL users expect.

  `ARITHMETIC::"="(left, right)`

• The `-work` option specifies `mylib` as the library to regenerate. `-refresh` rebuilds the library image without using source code, allowing models delivered as compiled libraries without source code to be rebuilt for a specific release of ModelSim (4.6 and later only).
  
  `vcom -work mylib -refresh`
vdel

This command deletes a design unit from a specified library.

Syntax

vdel [-help] [-lib <library_path>] [-modelsimini <ini_filepath>] [-verbose]
[-all | <primary> [<arch_name>]]

Arguments

- `-all`
  (optional) Deletes an entire library.

  **Caution**
  BE CAREFUL! Libraries cannot be recovered once deleted. You are not prompted for confirmation.

- `<arch_name>`
  (optional) Specifies the name of an architecture to be deleted. Optional. If omitted, all of the architectures for the specified entity are deleted. Invalid for a configuration or a package.

- `<primary>`

  (required unless `-all` is used) Specifies the entity, package, configuration, or module to be deleted. `-help`
  (optional) Displays the command’s options and arguments.

- `-lib <library_path>`
  (optional) Specifies location of the library that holds the design unit to be deleted. By default, the design unit is deleted from the `work` library.

  `<library_path>` — A logical name or pathname of the library.

- `-modelsimini <ini_filepath>`
  (optional) Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable.

  `<ini_filepath>` — Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (`/`).

- `-verbose`
  (optional) Displays progress messages.

Examples

- Delete the `work` library.

  `vdel -all`

- Delete the `synopsys` library.
vdel -lib synopsys -all

- Delete the entity named xor and all its architectures from the work library.
  
vdel xor

- Delete the architecture named behavior of the entity xor from the work library.
  
vdel xor behavior

- Delete the package named base from the work library.
  
vdel base
This command lists the contents of a design library.

This command also checks the compatibility of a vendor library. If `vdir` cannot read a vendor-supplied library, the library may not be compatible with ModelSim.

**Syntax**

```
vdir [-all | [-lib <library_name>]] [<design_unit>] [-help] [-l | [-prop <prop>]]
[-modelsimini <ini_filepath>]] [-r]
```

**Arguments**

- `-all`
  (optional) Lists the contents of all libraries listed in the Library section of the active `modelsim.ini` file. Refer to `modelsim.ini Variables` for more information.

- `-lib <library_name>`
  (optional) Specifies the logical name or the pathname of a library to be listed. By default, the contents of the `work` library are listed.

  `<library_name>` — A logical name or pathname of the library.

- `<design_unit>`
  (optional) Indicates the design unit to search for within the specified library. If the design unit is a VHDL entity, its architectures are listed. By default all entities, configurations, modules, packages, and optimized design units in the specified library are listed.

- `-help`
  (optional) Displays options and arguments for this command.

- `-l`
  (optional) Prints the version of `vcom/vlog` with which each design unit was compiled, plus any compilation options used. Also prints the object-code version number that indicates which versions of `vcom/vlog` and ModelSim are compatible.

- `-prop <prop>`
  (optional) Reports on a design unit property.

  `<prop>` — Specifies a design property as listed in Table 2-5. If you do not specify a value for `<prop>`, an error message is displayed.

**Table 2-5. Design Unit Properties**

<table>
<thead>
<tr>
<th>Value of <code>&lt;prop&gt;</code></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>archcfg</td>
<td>configuration for arch</td>
</tr>
<tr>
<td>bbox</td>
<td>blackbox for optimized</td>
</tr>
<tr>
<td>body</td>
<td>needs a body</td>
</tr>
</tbody>
</table>

VHDL entity, its architectures are listed. By default all entities, configurations, modules, packages, and optimized design units in the specified library are listed.
Commands

vdir

- modelsimini <ini_filepath>
  (optional) Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable.
  
  <ini_filepath> — Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (/).

- -r
  (optional) Prints architecture information for each entity in the output.

Examples

- List the architectures associated with the entity named my_asic that reside in the HDL design library called design.

  vdir -lib design my_asic

- Show the output of vdir -l, including any compilation options used to compile the library:

  > # MODULE ram_tb
  > # Verilog Version: RV9i]?9FGhibjG<jXXV_.`1
  > # Version number: CRW2<UhheaW;LIL2_B5o31

Table 2-5. Design Unit Properties

<table>
<thead>
<tr>
<th>Value of &lt;prop&gt;</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>default</td>
<td>default options</td>
</tr>
<tr>
<td>dir</td>
<td>source directory</td>
</tr>
<tr>
<td>dpnd</td>
<td>depends on</td>
</tr>
<tr>
<td>entcfg</td>
<td>configuration for entity</td>
</tr>
<tr>
<td>extern</td>
<td>package reference number</td>
</tr>
<tr>
<td>inline</td>
<td>module inlined</td>
</tr>
<tr>
<td>lrm</td>
<td>language standard</td>
</tr>
<tr>
<td>mtime</td>
<td>source modified time</td>
</tr>
<tr>
<td>name</td>
<td>short name</td>
</tr>
<tr>
<td>opcode</td>
<td>opcode format</td>
</tr>
<tr>
<td>options</td>
<td>compile options</td>
</tr>
<tr>
<td>root</td>
<td>optimized Verilog design root</td>
</tr>
<tr>
<td>src</td>
<td>source file</td>
</tr>
<tr>
<td>top</td>
<td>top level model</td>
</tr>
<tr>
<td>ver</td>
<td>version string</td>
</tr>
<tr>
<td>vlogv</td>
<td>Verilog version</td>
</tr>
</tbody>
</table>


Source modified time: 1132284874
Source file: ram_tb.v
Start source location: ram_tb.v:47
Version number: CRW2<UhheaW;LIL2_B5o31
Opcode format: 6.1c; VLOG SE Object version 31
Optimized Verilog design root: 1
Language standard: 1
Compile options: -cover bcst
Compile defaults: GenerateLoopIterationMax=100000
Source directory: C:\Verif\QuestaSim_6.1c\examples\tutorials\verilog\memory
vencrypt

This command encrypts Verilog and SystemVerilog code contained within encryption envelopes. The code is not pre-processed before encryption, so macros and other `directives are unchanged. This allows IP vendors to deliver encrypted IP with undefined macros and `directives.

Upon execution of this command, the filename extension will be changed to .vp for Verilog files (.v files) and .svp for SystemVerilog files (.sv files). As the vencrypt utility processes the file (or files), if it does not find any encryption directives it reprocesses the file using the following default encryption:

```
`pragma protect data_method = "aes128-cbc"
`pragma protect key_keyowner = "MTI"
`pragma protect key_keyname = "MGC-DVT-MTI"
`pragma protect key_method = "rsa"
`pragma protect key_block encoding = (enctype = "base64")
`pragma protect begin
```

The vencrypt command must be followed by a compile command, such as vlog, for the design to be compiled.

Syntax

```
```

- `<filename>` (required) Specifies the name of the Verilog source code file to encrypt. Multiple filenames can be entered separated by spaces. Wildcards can be used. Default encryption pragmas will be used, as described above, if no encryption directives are found during processing.

- `-d <dirname>` (optional) Specifies directory that will contain encrypted Verilog files. If no directory is specified, current working directory will be used. The original file extension (.v for Verilog and .sv for SystemVerilog) will be preserved.

  `<dirname>` —

- `-e <extension>` (optional) Specifies a filename extension.

  `<extension>` —

- `-f <filename>` (optional) Specifies a file with more command line arguments. Allows complex arguments to be reused without retyping. Nesting of `-f` options is allowed.

  `<filename>` —

Refer to the section "Argument Files" for more information.
• `-h <filename>`
  (optional) Concatenates header information, specified by `<file>`, into all design files listed with `<filename>`. Allows the user to pass a large number of files to the vencrypt utility that do not contain the `pragma protect` or `protect` information about how to encrypt the file. Saves the user from editing hundreds of files to add in the same `pragma protect` to every file.

  `<filename>` —

• `-help`
  (optional) Displays vencrypt command arguments.

• `-l <filename>`
  (optional) Redirects output to the file designated by `<filename>`.

  `<filename>` —

• `-o <filename>`
  (optional) Combines all encrypted output into a single file.

  `<filename>` —

• `-p <prefix>`
  (optional) Prepends file names with a prefix.

  `<prefix>` —

• `-quiet`
  (optional) Disables encryption messages.

See also


Example

• Insert header information into all design files listed.

  vencrypt -h encrypt_head top.v cache.v gates.v memory.v

The `encrypt_head` file may look like the following:

```
`pragma protect data_method = "aes128-cbc"
`pragma protect author = "IP Provider"
`pragma protect key_keyowner = "MTI", key_method = "rsa"
`pragma protect key_keyname = "MGC-DVT-MTI"
`pragma protect begin
```

There is no `pragma protect end` expression in the header file, just the header block that starts the encryption. The `pragma protect end` expression is implied by the end of the file. For more detailed examples, see "Protecting Your Source Code" in the User’s Manual.
verror

The `verror` command prints a detailed description about a message number. It may also point to additional documentation related to the error.

Syntax

```
verror [-fmt | -tag | -fmt -tag | -full] <msgNum> ...
verror [-fmt | -tag | -fmt -tag | -full] [-tool <tool>] -all
verror -ranges
verror -help
```

Arguments

- `-fmt | -tag | -full`
  Specifies the type and amount of information to return.
  - `-fmt` — returns the format string used in the error message.
  - `-tag` — returns a tag associated with the error message.
  - `-full` — returns the format string, tag, and complete text associated with the error message.
- `[-tool <tool>] -all`
  Allows you to return information about all error messages.
  - `-all` — returns all error messages.
  - `-tool <tool> -all` — returns all error messages associated with the specified tool, where `<tool>` can be one of the following:
    - `common`
    - `vcom`
    - `vcom-vlog`
    - `vlog`
    - `vsim`
    - `vsim-vish`
    - `wlf`
    - `vsim-sccom`
    - `sccom`
    - `vsim-systemc`
    - `ucdb`
    - `vsim-vlog`
    - `pseudo_synth`
- `<msgNum>`
  Specifies the message number(s) you would like more information about. You can find the message number in messages of the format:
  ```
  ** <Level>: ([<Tool>]-[<Group>]-]<MsgNum>) <FormattedMsg>
  ```
  You can specify `<msgNum>` any number of times for one verror command. It is suggested that you use a space-separated list.
- `-ranges`
  Prints the numeric ranges of error message numbers, organized by tool.
Example

- If you receive the following message in the transcript:

  ** Error (vsim-3061) foo.v(22): Too many Verilog port connections.

  and you would like more information about this message, you would type:

  verror 3061

  and receive the following output:

  Message # 3061:
  Too many Verilog ports were specified in a mixed VHDL/Verilog instantiation. Verify that the correct VHDL/Verilog connection is being made and that the number of ports matches.
vgencomp

Once a Verilog module is compiled into a library, you can use the `vgencomp` command to write its equivalent VHDL component declaration to standard output.

Optional switches allow you to generate bit or vl_logic port types; std_logic port types are generated by default.

Syntax

```
<module_name>
```

Arguments

- `-help`
  Displays the command’s options and arguments. Optional.

- `-lib <library_name>`
  Specifies the pathname of the working library. If not specified, the default library `work` is used. Optional.

- `-b`
  Causes `vgencomp` to generate bit port types. Optional.

- `-modelsimini <ini_filepath>`
  Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (`/`).

- `-s`
  Used for the explicit declaration of default std_logic port types. Optional.

- `-v`
  Causes `vgencomp` to generate vl_logic port types. Optional.

- `<module_name>`
  Specifies the name of the Verilog module to be accessed. Required.

Examples

- This example uses a Verilog module that is compiled into the `work` library. The module begins as Verilog source code:
module top(i1, o1, o2, io1);
    parameter width = 8;
    parameter delay = 4.5;
    parameter filename = "file.in";
    input i1;
    output [7:0] o1;
    output [4:7] o2;
    inout [width-1:0] io1;
endmodule

After compiling, \texttt{vgencomp} is invoked on the compiled module:

\texttt{vgencomp top}

and writes the following to stdout:

\begin{verbatim}
component top
generic(
    width           : integer := 8;
    delay           : real    := 4.500000;
    filename        : string  := "file.in"
);
port(
    i1              : in    std_logic;
    o1              : out   std_logic_vector(7 downto 0);
    o2              : out   std_logic_vector(4 to 7);
    io1             : inout std_logic_vector[width-1:0];
);
end component;
\end{verbatim}
The `view` command opens the specified window. The `view` command without arguments returns a list of windows currently being viewed.

To remove a window, use the `noview` command.

The `view` command with one or more options and no window names specified applies the options to the currently open windows. See examples for additional details.

**Syntax**

```
view <window_type>...
   [-title {New Window Title}]
   [-undock [{-icon} [-height <n>] [-width <n>] [-x <n>] [-y <n>]] | -dock]
```

**Arguments**

- `-aliases`
  Returns a list of `<window_type>` aliases.
- `-height <n>`
  Specifies the window height in pixels. Can only be used with the `-undock` switch. Optional.
- `-icon`
  Toggles the view between window and icon. Can only be used with the `-undock` switch. Optional.
- `-names`
  Returns a list of valid `<window_type>` arguments.
- `-title {New Window Title}`
  Specifies the window title of the designated window. Curly braces are only needed for titles that include spaces. Double quotes can be used in place of braces, for example "New Window Title". If the new window title does not include spaces, no braces or quotes are needed. For example: `-title new_wave wave` assigns the title `new_wave` to the Wave window.
- `-undock`
  Opens the specified window as a standalone window, undocked from the Main window. Optional.
- `-dock`
  Docks the specified standalone window into the Main window.
- `-width <n>`
  Specifies the window width in pixels. Can only be used with the `-undock` switch. Optional.
• `<window_type>…`
  Specifies the window type to view. Required. You do not need to type the full type name (see examples below); implicit wildcards are accepted; multiple window types are accepted. Available window types are:

  - `assertions`  
  - `atv`  
  - `branch`  
  - `browser`  
  - `calltree`  
  - `capacity`  
  - `classgraph`  
  - `classtree`  
  - `condition`  
  - `covergroups`  
  - `dataflow`  
  - `details`  
  - `duranked`  
  - `exclusions`  
  - `expression`  
  - `fcovers`  
  - `files`  
  - `fsmcoverage`  
  - `fsmlist`  
  - `fsmview`  
  - `instance`  
  - `library`  
  - `list`  
  - `locals`  
  - `memdata`  
  - `memory`  
  - `msgviewer`  
  - `objects`  
  - `process`  
  - `profiledetails`  
  - `project`  
  - `ranked`  
  - `schematic`  
  - `source`  
  - `stackview`  
  - `statement`  
  - `structural`  
  - `structure`  
  - `toggle`  
  - `tracker`  
  - `transaction`  
  - `transcript`  
  - `watch`  
  - `wave`

  Not all windows are available with all variants (ModelSim SE, ModelSim PE, Questa SV/AFV, etc.)

• `-x <n>`
  Specifies the window upper-left-hand x-coordinate in pixels. Can only be used with the `-undock` switch. Optional.

• `-y <n>`
  Specifies the window upper-left-hand y-coordinate in pixels. Can only be used with the `-undock` switch. Optional.

**Examples**

- Undock the Wave window from the Main window and makes it a standalone window.
  
  ```
  view -undock wave
  ```

- Display an undocked Processes window in the upper left-hand corner of the monitor with a window size of 300 pixels, square.
  
  ```
  view process -undock -x 0 -y 0 -width 300 -height 300
  ```

- Display the Watch and Wave windows.
  
  ```
  view w
  ```

- Display the Objects and Processes windows.
view ob pr

- Open a new Wave window with My Wave Window as its title.

  view -title {My Wave Window} wave

See also

noview
virtual count

The virtual count command reports the number of currently defined virtuals that were not read in using a macro file.

Syntax

virtual count [-kind {implicits | explicits}] [-unsaved]

Arguments

- kind {implicits | explicits}
  (optional) Reports only a subset of virtuals.
  implicits — virtual signals created internally by the product.
  explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.
- unsaved
  (optional) Reports the count of only those virtuals that have not been saved to a macro file.

See also

virtual define, virtual save, virtual show, “Virtual Objects”
virtual define

The **virtual define** command prints to the transcript the definition of the virtual signals, functions, or regions in the form of a command that can be used to re-create the object.

**Syntax**

```bash
virtual define [-kind <kind>] <pathname>
```

**Arguments**

- `-kind {implicits | explicits}`
  (optional) Transcripts only a subset of virtuals.
  - implicits — virtual signals created internally by the tool.
  - explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.
- `<pathname>`
  (required) Specifies the path to the virtual(s) for which you want definitions, where wildcards are allowed.

**Examples**

- Show the definitions of all the virtuals you have explicitly created.
  ```bash
  virtual define -kind explicits *
  ```

**See also**

- virtual describe, virtual show, “Virtual Objects”
virtual delete

The virtual delete command removes the matching virtuals.

Syntax

virtual delete [-kind <kind>] <pathname>

Arguments

- -kind {implicits | explicits}
  (optional) Removes only a subset of virtuals.
  implicits — virtual signals created internally by the product.
  explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.
- <pathname>
  (required) Specifies the path to the virtual(s) you want to delete, where wildcards are allowed.

Examples

- Delete all of the virtuals you have explicitly created.
  
  virtual delete -kind explicits *

See also

virtual signal, virtual function, “Virtual Objects”
virtual describe

The virtual describe command prints to the transcript a complete description of the data type of one or more virtual signals.

Similar to the existing describe command.

Syntax

virtual describe [-kind <kind>] <pathname>

Arguments

- -kind {implicits | explicits}
  (optional) Transcripts only a subset of virtuals.
    implicits — virtual signals created internally by the product.
    explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
    Unique abbreviations are accepted.
- <pathname>
  (required) Specifies the path to the virtual(s) for which you want descriptions, where wildcards are allowed.

Examples

- Describe the data type of all virtuals you have explicitly created.
  
  virtual describe -kind explicits *

See also

virtual define, virtual show, “Virtual Objects”
virtual expand

The virtual expand command prints to the transcript a list of all the non-virtual objects contained in the specified virtual signal(s).

You can use this to create a list of arguments for a command that does not accept or understand virtual signals.

Syntax

virtual expand [-base] <pathname> ...

Arguments

- **-base**
  (optional) Outputs the root signal parent in place of a subelement. For example:

  ```text
  vcd add [virtual expand -base myVirtualSignal]
  ```

  the resulting command after substitution would be:

  ```text
  vcd add signala signalb signalc
  ```

- **<pathname>**
  (required) Specifies the path to the signals and virtual signals to expand, where wildcards are allowed and you can specify any number of paths.

Examples

- Add the elements of a virtual signal to the VCD file.

  In the Tcl language, the square brackets specify that the enclosed command should be executed first ("virtual expand ..."), then the result substituted into the surrounding command.

    ```text
    vcd add [virtual expand myVirtualSignal]
    ```

  Therefore, if myVirtualSignal is a concatenation of signala, signalb.rec1 and signalc(5 downto 3), the resulting command after substitution would be:

    ```text
    vcd add signala signalb.rec1 {signalc(5 downto 3)}
    ```

  The slice of signalc is enclosed in curly braces, because it contains spaces.

See also

- virtual signal, “Virtual Objects”
virtual function

The virtual function command creates a new signal, known only by the GUI (not the kernel), that consists of logical operations on existing signals and simulation time, as described in `<expressionString>`.

It cannot handle bit selects and slices of Verilog registers. Please see Syntax and Conventions for more details on syntax.

If the virtual function references more than a single scalar signal, it will display as an expandable object in the Wave and Objects windows. The children correspond to the inputs of the virtual function. This allows the function to be "expanded" in the Wave window to see the values of each of the input waveforms, which could be useful when using virtual functions to compare two signal values.

Virtual functions can also be used to gate the List window display.

Note

The virtual function and virtual signal commands are interchangeable. The product will keep track of whether you’ve created a signal or a function with the commands and maintain them appropriately. We document both commands because the virtual save, virtual describe, and virtual define commands will reference your virtual objects using the correct command.

Syntax

virtual function [-env <path>] [-install <path>] [-delay <time>] {<expressionString>} <name>

Arguments

Arguments for virtual function are the same as those for virtual signal, except for the contents of the expression string.

- `-env <path>`
  (optional) Specifies a hierarchical context for the signal names in `<expressionString>` so they don't all have to be full paths.

- `-install <path>`
  (optional) Causes the newly-created signal to become a child of the specified region. If `-install` is not specified, the newly-created signal becomes a child of the nearest common ancestor of all objects appearing in `<expressionString>`. If the expression references more than one WLF file (dataset), the virtual signal will automatically be placed in region virtuals:/Functions.

- `-delay <time>`
  (optional) Specifies a value by which the virtual function will be delayed. You can use negative values to look forward in time. If units are specified, the `<time>` option must be enclosed in curly braces. See the examples below for more details.
• \{<expressionString>\}  
  (required) A text string expression, enclosed in curly braces (\{\}) using the GUI_expression_format.

• <name>  
  (required) The name you define for the virtual signal.

  Case is ignored unless installed in a Verilog region.

  Use alpha, numeric, and underscore characters only, unless you are using VHDL extended identifier notation.

  If using VHDL extended identifier notation, <name> needs to be quoted with double quotes or with curly braces.

Examples

• Create a signal /chip/section1/clk_n that is the inverse of /chip/section1/clk.
  
    virtual function \{ not /chip/section1/clk \} clk_n

• Create a std_logic_vector equivalent of a Verilog register rega and installs it as /chip/rega_slv.
  
    virtual function -install /chip \{ (std_logic_vector) chip.vlog.rega \} rega_slv

• Create a boolean signal /chip/addr_eq_fab that is true when /chip/addr[11:0] is equal to hex "fab", and false otherwise. It is acceptable to mix VHDL signal path notation with Verilog part-select notation.
  
    virtual function \{ /chip/addr[11:0] == 0xfab \} addr_eq_fab

• Create a signal that is high only during times when signal /chip/siga of the gate-level version of the design does not match /chip/siga of the rtl version of the design. Because there is no common design region for the inputs to the expression, siga_diff is installed in region virtuals:/Functions. The virtual function siga_diff can be added to the Wave window, and when expanded will show the two original signals that are being compared.
  
    virtual function \{ gate:/chip/siga XOR rtl:/chip/siga \} siga_diff

• Create a virtual signal consisting of the logical "AND" function of /top/signalA with /top/signalB, and delays it by 10 ns.
  
    virtual function -delay \{10 ns\} (/top/signalA AND /top/signalB) myDelayAandB

• Create a one-bit signal outbus_diff which is non-zero during times when any bit of /chip/outbus in the gate-level version doesn’t match the corresponding bit in the rtl version.
This expression uses the "OR-reduction" operator, which takes the logical OR of all the bits of the vector argument.

```
virtual function { | (gate:/chip/outbus XOR rtl:/chip/outbus) }
outbus_diff
```

 Commands fully compatible with virtual functions

- add log and log
- delete
- examine
- find
- searchlog
- show

 Commands not compatible with virtual functions

- drivers
- force
- noforce
- vcd add
- when

 See also

- virtual count
- virtual define
- virtual delete
- virtual describe
- virtual expand
- virtual hide
- virtual log
- virtual nohide
- virtual nolog
- virtual region
- virtual save
- virtual show
- virtual signal
- virtual type
- “Virtual Objects”
**virtual hide**

The **virtual hide** command causes the specified real or virtual signals to not be displayed in the Objects window. This is used when you want to replace an expanded bus with a user-defined bus.

You make the signals reappear using the **virtual nohide** command.

**Syntax**

```
virtual hide { [-kind <kind>] | [-region <path>]} <pattern>
```

**Arguments**

- **-kind {implicits | explicits}**
  (optional) Hides only a subset of virtuals.
  - implicits — virtual signals created internally by the tool.
  - explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.

- **-region <path>**
  (optional) Specifies a region of design space in which to look for the signal names.

- **<pattern>**
  (required) Indicates which signal names or wildcard patterns should be used in finding the signals to hide, where wildcards are allowed and you can specify any number of names or patterns.

**See also**

virtual nohide, “Virtual Objects”
virtual log

The virtual log command causes the simulation-mode dependent signals of the specified virtual signals to be logged by the kernel. If wildcard patterns are used, it will also log any normal signals found, unless the -only option is used. You unlog the signals using the virtual nolog command.

Syntax


Arguments

• -kind {implicits | explicits}
  (optional) Logs only a subset of virtuals.
  implicits — virtual signals created internally by the tool.
  explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.

• -region <path>
  (optional) Specifies a region of design space in which to look for signals to log.

• -recursive
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

• -only
  (optional) Specify that only virtual signals (as opposed to all signals) found by a <pattern> containing a wildcard should be logged.

• -in
  Specifies that the kernel log data for ports of mode IN whose names match the specification. Optional.

• -out
  (optional) Specifies that the kernel log data for ports of mode OUT whose names match the specification.

• -inout
  (optional) Specifies that the kernel log data for ports of mode INOUT whose names match the specification.

• -internal
  (optional) Specifies that the kernel log data for internal (non-port) objects whose names match the specification.
• -ports
   (optional) Specifies that the kernel log data for all ports. Optional.
• <pattern>
   (required) Indicates which signal names or wildcard patterns should be used in finding the
   signals to log, where you can specify any number of names or wildcard patterns.

See also

virtual nolog, “Virtual Objects”
**virtual nohide**

The **virtual nohide** command reverses the effect of a **virtual hide** command, causing the specified real or virtual signals to reappear the Objects window.

**Syntax**

```
virtual nohide { [-kind <kind>] | [-region <path>] } <pattern>
```

**Arguments**

- **-kind {implicits | explicits}**
  (optional) Unhides only a subset of virtuals.
  - implicits — virtual signals created internally by the tool.
  - explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.

- **-region <path>**
  (optional) Specifies a region of design space in which to look for the signal names.

- **<pattern>**
  (required) Indicates which signal names or wildcard patterns should be used in finding the signals to hide, where wildcards are allowed and you can specify any number of names or patterns.

**See also**

**virtual hide, “Virtual Objects”**
virtual nolog

The **virtual nolog** command reverses the effect of a **virtual log** command. It causes the simulation-dependent signals of the specified virtual signals to be excluded ("unlogged") by the kernel.

If wildcard patterns are used, it will also unlog any normal signals found, unless the **-only** option is used.

**Syntax**

```plaintext
```

**Arguments**

- **-kind {implicits | explicits}**
  (optional) Excludes only a subset of virtuals.
  implicits — virtual signals created internally by the tool.
  explicits — virtual signals explicitly created by a user, such as with the virtual signal command.
  Unique abbreviations are accepted.

- **-region <path>**
  (optional) Specifies a region of design space in which to look for signals to unlog.

- **-recursive**
  (optional) Specifies that the scope of the search is to descend recursively into subregions. If omitted, the search is limited to the selected region.

- **-only**
  (optional) Specify that only virtual signals (as opposed to all signals) found by a <pattern> containing a wildcard should be unlogged.

- **-in**
  (optional) Specifies that the kernel exclude data for ports of mode IN whose names match the specification.

- **-out**
  (optional) Specifies that the kernel exclude data for ports of mode OUT whose names match the specification.

- **-inout**
  (optional) Specifies that the kernel exclude data for ports of mode INOUT whose names match the specification.
Commands

**virtual nolog**

- **-internal**
  (optional) Specifies that the kernel exclude data for internal (non-port) objects whose names match the specification.

- **-ports**
  (optional) Specifies that the kernel exclude data for all ports.

- **<pattern>**
  (required) Indicates which signal names or wildcard patterns should be used in finding the signals to unlog, where wildcards are allowed and you can specify any number of names or patterns.

**See also**

virtual log, “Virtual Objects”
virtual region

The **virtual region** command creates a new user-defined design hierarchy region.

**Syntax**

```
virtual region <parentPath> <regionName>
```

**Arguments**

- `<parentPath>`
  (required) The full path to the region that will become the parent of the new region.
- `<regionName>`
  (required) The name you want for the new region.

**See also**

`virtual function`, `virtual signal`, “Virtual Objects”

---

**Note**

Virtual regions cannot be used in the `when` command.
virtual save

The virtual save command saves the definitions of virtuals to a file named virtual.do in the current directory.

Syntax

virtual save [-kind <kind>] [-append] [<filename>]

Arguments

- kind {implicits | explicits}
  (optional) Saves only a subset of virtuals.
  implicits — virtual signals created internally by the tool.
  explicits — virtual signals explicitly created by a user, such as with the virtual signal command.

Unique abbreviations are accepted.

- append
  (optional) Specifies to save only virtuals that are not already saved or weren’t read in from a macro file. These unsaved virtuals are then appended to the specified or default file. Optional.

- <filename>
  (optional) The name of the file containing the definitions. If you don’t specify <filename>, the default virtual filename (virtuals.do) will be used. You can specify a different default in the pref.tcl file.

See also

virtual count, “Virtual Objects”
**virtual show**

The **virtual show** command lists the full path names of all explicitly defined virtuals.

**Syntax**

```
virtual show [-kind <kind>]
```

**Arguments**

- `-kind {implicits | explicits}`
  
  (optional) Lists only a subset of virtuals.
  
  - **implicits** — virtual signals created internally by the tool.
  - **explicits** — virtual signals explicitly created by a user, such as with the virtual signal command.

  Unique abbreviations are accepted.

**See also**

- `virtual define`, `virtual describe`, “Virtual Objects”
virtual signal

The **virtual signal** command creates a new signal, known only by the GUI (not the kernel), that consists of concatenations of signals and subelements as specified in `<expressionString>`. It cannot handle bit selects and slices of Verilog registers. Please see Concatenation of Signals or Subelements for more details on syntax.

**Note**
The virtual function and virtual signal commands are interchangeable. The product will keep track of whether you’ve created a signal or a function with the commands and maintain them appropriately. We document both commands because the virtual save, virtual describe, and virtual define commands will reference your virtual objects using the correct command.

**Syntax**

```
virtual signal [-env <path>] [-install <path>] [-delay <time>] {<expressionString>} <name>
```

**Arguments**

- `-env <path>`
  (optional) Specifies a hierarchical context for the signal names in `<expressionString>` so they don’t all have to be full paths.

- `-install <path>`
  (optional) Causes the newly-created signal to become a child of the specified region. If `-install` is not specified, the newly-created signal becomes a child of the nearest common ancestor of all objects appearing in `<expressionString>`. If the expression references more than one WLF file (dataset), the virtual signal will automatically be placed in region virtuals:/Signals.

- `-delay <time>`
  (optional) Specifies a value by which the virtual function will be delayed. You can use negative values to look forward in time. If units are specified, the `<time>` option must be enclosed in curly braces. See the examples below for more details.

- `{<expressionString>}`
  (required) A text string expression, enclosed in curly braces (`{ }`) using the GUI_expression_format.

- `<name>`
  (required) The name you define for the virtual signal.

Case is ignored unless installed in a Verilog region.

Use alpha, numeric, and underscore characters only, unless you are using VHDL extended identifier notation.
If using VHDL extended identifier notation, `<name>` needs to be quoted with double quotes or with curly braces.

**Examples**

- **Reconstruct a bus** `sim:/chip/alu/a(4 downto 0)`, using VHDL notation, assuming that `a_ii` are all scalars of the same type.

  ```vhdl
  virtual signal -env sim:/chip/alu ( (concat_range (4 downto 0))(a_04 & a_03 & a_02 & a_01 & a_00) ) a
  ```

- **Reconstruct a bus** `sim:chip.alu.a[4:0]`, using Verilog notation. Note that the concatenation notation starts with `"{"` rather than `{"`.

  ```verilog
  virtual signal -env sim:chip.alu
  ( concat_range [4:0])&{a_04, a_03, a_02, a_01, a_00} ) a
  ```

- **Create a signal** `sim:/testbench/stuff` which is a record type with three fields corresponding to the three specified signals. The example assumes `/chipa/mode` is of type integer, `/chipa/alu/a` is of type std_logic_vector, and `/chipa/decode/inst` is a user-defined enumeration.

  ```verilog
  virtual signal -install sim:/testbench
  { /chipa/alu/a(19 downto 13) & /chipa/decode/inst & /chipa/mode } stuff
  ```

- **Create a virtual signal** that is the same as `/top/signalA` except it is delayed by 10 ps.

  ```verilog
  virtual signal -delay {10 ps} {/top/signalA} myDelayedSignalA
  ```

- **Create a three-bit signal**, `chip.address_mode`, as an alias to the specified bits.

  ```verilog
  virtual signal { chip.instruction[23:21] } address_mode
  ```

- **Concatenate signals** `a`, `b`, and `c` with the literal constant ‘000’.

  ```verilog
  virtual signal {a & b & c & 3'b000} myextendedbus
  ```

- **Add three missing bits to the bus** `num`, creates a virtual signal `fullbus`, and then adds that signal to the Wave window.

  ```verilog
  virtual signal {num & "000"} fullbus
  add wave -unsigned fullbus
  ```

- **Reconstruct a bus that was fragmented by synthesis and is missing the lower three bits.** Note that you would have to type in the actual bit names (i.e. num28, num27, etc.) represented by the … in the syntax above.

  ```verilog
  virtual signal { num31 & num30 & num29 & ... & num4 & num3 & "000" } fullbus
  add wave -unsigned fullbus
  ```

- **Create a two-bit signal** (with an enumerated type) based on the results of the subexpressions. For example, if `aold` equals `anew`, then the first bit is true (1).
Alternatively, if \textit{bold} does not equal \textit{bnew}, the second bit is false (0). Each subexpression is evaluated independently.

\begin{verbatim}
virtual signal {(aold == anew) & (bold == bnew)} myequalityvector
\end{verbatim}

- Create signal \textit{newbus} that is a concatenation of \textit{bus1} (bit-reversed) and \textit{bus2[7:4]} (bit-reversed). Assuming \textit{bus1} has indices running 7 downto 0, the result will be \textit{newbus[11:0]} with the upper 8 bits being \textit{bus1[0:7]} and the lower 4 bits being \textit{bus2[4:7]}. See \textit{Concatenation Directives} for further details.

\begin{verbatim}
virtual signal {(concat_reverse)(bus1 & bus2[7:4])} newbus
\end{verbatim}

### Commands fully compatible with virtual signals

- add list
- add log or log
- add wave
- delete
- describe
- examine
- find
- force and noforce
- restart
- searchlog
- show

### Commands compatible with virtual signals using \texttt{[virtual expand <signal>]}\texttt{]}

- drivers
- vcd add

### Commands not currently compatible with virtual signals

- when

### See also

- virtual count
- virtual define
- virtual delete
- virtual describe
- virtual expand
- virtual hide
- virtual log
- virtual nohide
- virtual nolog
- virtual region
- virtual save
- virtual show
- virtual function
- virtual type
- “Virtual Objects”
virtual type

The virtual type command creates a new enumerated type known only by the GUI, not the kernel. Virtual types are used to convert signal values to character strings. The command works with signed integer values up to 64 bits.

Virtual types cannot be used in the when command.

Note

If you are using SystemVerilog, you can also convert signal values to character strings using associative arrays in your code. See the SystemVerilog LRM for more information.

Syntax

virtual type -delete <name> | {<list_of_strings>} <name>

Arguments

• -delete <name>
  Deletes a previously defined virtual type. <name> is the name you gave the virtual type when you originally defined it. Required if not defining a type.

• {<list_of_strings>}
  A list of values and their associated character strings. Required if -delete is not used. Values can be expressed in decimal or based notation and can include "don’t-cares" (see examples below). Three kinds of based notation are supported: Verilog, VHDL, and C-language styles. The values are interpreted without regard to the size of the bus to be mapped. Bus widths up to 64 bits are supported.

  There is currently no restriction on the contents of each string, but if strings contain spaces they would need to be quoted, and if they contain characters treated specially by Tcl (square brackets, curly braces, backslashes…), they would need to be quoted with curly braces.

  See the examples below for further syntax.

• <name>
  The user-defined name of the virtual type. Required if -delete is not used. Case is not ignored. Use alpha, numeric, and underscore characters only, unless you are using VHDL extended identifier notation. If using VHDL extended identifier notation, <name> needs to be quoted with double quotes or with curly braces.

Examples

• Using positional notation, associates each string with an enumeration index, starting at zero and increasing by one in the positive direction. When myConvertedSignal is displayed in the Wave, List, or Objects window, the string "state0" will appear when mysignal == 0, "state1" when mysignal == 1, "state2" when mysignal == 2, etc.
virtual type {state0 state1 state2 state3} mystateType
virtual function {(mystateType)mysignal} myConvertedSignal
add wave myConvertedSignal

• Use sparse mapping of bus values to alphanumeric strings for an 8-bit, one-hot encoding. It shows the variety of syntax that can be used for values. The value "default" has special meaning and corresponds to any value not explicitly specified.

```
virtual type {{0 NULL_STATE} {1 st1} {2 st2} {0x04 st3} {16'h08 st4} \
    {'h10 st5} {16#20 st6} {0b01000000 st7} {0x80 st8} \
    {default BAD_STATE}} myMappedType
virtual function {{(myMappedType)mybus} myConvertedBus
add wave myConvertedBus
```

• Delete the virtual type "mystateType".

```
virtual type -delete mystateType
```

• Create a virtual type that includes "don't-cares" (the '-' character).

```
virtual type {{0x01-- add}{0x02-- sub}{default bad}} mydecodetype
```

• Create a virtual type using a mask for "don't-cares." The middle field is the mask, and the mask should have bits set to 1 for the bits that are don't care.

```
virtual type {{0x0100 0xff add}{0x0200 0xff sub}{default bad}}
mydecodetype
```

See also

virtual function, “Virtual Objects”
vlib

The vlib command creates a design library. You must use vlib rather than operating system commands to create a library directory or index file.

If the specified library already exists as a valid ModelSim library, the vlib command will exit with a warning message without touching the library.

Syntax

vlib [-archive [-compact <percent>]] [-format { 1 | 3 }] [-help] [-dos | -short | -unix | -long] [-lock | -unlock] [-locklib | -unlocklib] <name>

Arguments

• -archive [-compact <percent>]
  Causes design units that are compiled into the created library to be stored in archives rather than in subdirectories. Optional. Refer to “Archives” for more details.

   You may optionally specify a decimal number between 0 and 1 that denotes the allowed percentage of wasted space before archives are compacted. By default archives are compacted when 50% (.5) of their space is wasted. See an example below.

• -format { 1 | 3 }
  Prepares a library for conversion to be compatible with a previous release, by altering the _info file.

   1 — allows you to convert a library to be compatible with the 6.2 series and earlier.

   3 — allows you to convert a library to be compatible with the 6.3 series and newer.

The usage flow would be:

\1) Using a current release of the simulator, run:
   vlib -format 1 current_lib
   vcom -refresh -work current_lib
   \ to prepare current_lib for conversion back to a 6.2 release
\2) Using a 6.2 release of the simulator, run:
   vcom -refresh -work current_lib
   \ to refresh current_lib for use with the previous release

• -help
  Displays the command’s options and arguments. Optional.

• -dos
  Specifies that subdirectories in a library have names that are compatible with DOS. Not recommended if you use the vmake utility. Optional.

• -short
  Interchangeable with the -dos argument. Optional.
• -unix
  Specifies that subdirectories in a library may have long file names that are NOT compatible with DOS. Optional.

• -long
  Interchangeable with the -unix argument. Optional.

• -lock | -unlock
  Locks an existing design unit so it cannot be recompiled or refreshed. The -unlock switch reverses this action. Optional. File permissions are not affected by these switches.

• -locklib | -unlocklib
  Locks a complete library so that compilation cannot target the library and the library cannot be refreshed. The -unlocklib switch reverses this action. Optional. File permissions are not affected by these switches.

• <name>
  Specifies the pathname or archive name of the library to be created. Required.

Examples

• Create the design library design. You can define a logical name for the library using the vmap command or by adding a line to the library section of the modelsim.ini file that is located in the same directory.
  
  vlib design

• Create the design library uut and specifies that any design units compiled into the library are created as archives. Also specifies that each archive be compacted when 30% of its space is wasted.
  
  vlib -archive -compact .3 uut
**vlog**

The **vlog** command compiles Verilog source code and SystemVerilog extensions into a specified working library (or to the **work** library by default).

The **vlog** command may be invoked from within ModelSim or from the operating system command prompt. It may also be invoked during simulation.

Compiled libraries are major-version dependent. When moving between major versions, you have to refresh compiled libraries using the **-refresh** argument to **vlog**. This is not true for minor versions (letter releases).

All arguments to the **vlog** command are case sensitive: **-WORK** and **-work** are not equivalent.

The IEEE P1800 Draft Standard for SystemVerilog requires that the default behavior of the **vlog** command is to treat each Verilog design file listed on the command line as a separate compilation unit. This behavior is a change in **vlog** from versions prior to 6.2, wherein all files in a single command line were concatenated into a single compilation unit. To treat multiple files listed within a single command line as a single compilation unit, use either the **vlog** **-mfcu** argument or the **MultiFileCompilationUnit modelsim.ini** file variable.

**Syntax**

vlog [options] <filename> [ <filename> ... ]

[options]:

  [-93]
  [-compat] [-compile_uselibs=[<directory_name>]]
  [-convertallparams] [-cuname]
  [+define+<macro_name>[=<macro_text>]] [+delay_mode_distributed]
  [+delay_mode_path] [+delay_mode_unit] [+delay_mode_zero]
  [-dpiforceheader] [-dpiheader <filename>]
  [-E <filename>] [-Epretty <filename>] [-error <msg_number>[,<msg_number>,…]]
  [-f <filename>] [-force_refresh <design_unit>]
  [-fsmimplicitrans] [-fsmsingle | -nofsmimplicitrans]
  [-fsmsingle | -nofmsingles] [-fsmxassign | -nofsmxassign]
  [-gen_xml <design_unit> <filename>]
  [-hazards] [-help]
  [+incdir=<directory>] [-incr | -nincr] [-isymfile]
  [+libcell] [+libext=<suffix>] [-libmap <pathname>]
  [-libmap_verbose] [+librescan] [-line <number>] [-lint]
  [+maxdelays] [+mindelays] [-mixedansiports]
  [-mixedsvvh [b | s | v]] [-mfcu | -sfcu] [-modelsimini <ini_filepath>]
  [-nodbgsym][+nolibcell] [-nologo]
  [+nospecify] [-note <msg_number>[,<msg_number>,…]]
Commands

vlog

```
[+notimingchecks] [-novtblfixup] [+warn<CODE>]
[-warn <category_number>]

[-O0]
[-pedanticerrors]
[-quiet]
[-R [<simargs>]] [-refresh]
[-source] [-s] [-sv]
[-suppress <msg_number>,<msg_number>,…]]
[-time] [-timescale <time_units>/<time_precision>]
[+typdelays]
[-u]

[-warning <msg_number>,<msg_number>,…]] [-work <library_name>]
[-y <library_directory>]
```

Arguments

- **-93**
  Specifies that the VHDL interface to Verilog modules use VHDL 1076-1993 extended identifiers to preserve case in Verilog identifiers that contain uppercase letters. Optional.

- **-compat**
  Disables optimizations that result in different event ordering than Verilog-XL. Optional. ModelSim Verilog generally duplicates Verilog-XL event ordering, but there are cases where it is inefficient to do so. Using this option does not help you find event order dependencies, but it allows you to ignore them. Keep in mind that this option does not account for all event order discrepancies, and that using this option may degrade performance. Refer to “Event Ordering in Verilog Designs” for additional information.

- **-compile_uselibs [=directory_name]**
  Locates source files specified in a `uselib` directive (Refer to “Verilog-XL uselib Compiler Directive”), compiles those files into automatically created libraries, and updates the `modelsim.ini` file with the logical mappings to the new libraries. Optional. If a `directory_name` is not specified, ModelSim uses the name specified in the MTL_USELIB_DIR environment variable. If that variable is not set, ModelSim creates the directory `mti_uselibs` in the current working directory.

- **-convertallparams**
  Enables converting parameters not defined in ANSI style to VHDL generics of type `std_logic_vector`, `bit_vector`, `std_logic`, `vl_logic`, `vl_logic_vector`, and `bit`. Optional.
-cuname

Used only in conjunction with -mfcu. Optional. The -cuname names the compilation unit being created by vlog. The named compilation unit can then be specified on the vsim command line, along with the <top> design unit. The purpose of doing so is to force elaboration of specified compilation unit package, thereby forcing elaboration of a necessary 'bind' statement within that compilation unit that would otherwise not be elaborated. An example of the necessary commands is:

```
vlog -cuname pkg_name -mfcu file1.sv file2.sv
vsim top pkg_name
```

You need to do this only in cases where you have a 'bind' statement in a module that might otherwise not be elaborated, because no module in the design depends on that compilation unit. In other words, if a module that depends on that compilation unit exists, you don’t need to force the elaboration, for it occurs automatically. Also, if you are using qverilog to compile and simulate the design, this binding issue is handled properly automatically.

+define+<macro_name>[=<macro_text>]

Allows you to define a macro from the command line that is equivalent to the following compiler directive:

```
`define <macro_name> <macro_text>
```

Optional. You can specify more than one macro with a single +define. For example:

```
vlog +define+one=r1+two=r2+three=r3 test.v
```

A command line macro overrides a macro of the same name defined with the `define compiler directive.

+delay_mode_distributed

Disables path delays in favor of distributed delays. Optional. Refer to “Delay Modes” for details.

+delay_mode_path

Sets distributed delays to zero in favor of using path delays. Optional.

+delay_mode_unit

Sets path delays to zero and non-zero distributed delays to one time unit. Optional.

+delay_mode_zero

Sets path delays and distributed delays to zero. Optional.

-dpiforceheader

Forces the generation of a DPI header file even if it will be empty of function prototypes.

-dpiheader <filename>

Generates a header file that may then be included in C source code for DPI import functions. Optional. Refer to “DPI Use Flow” for additional information.
- **-E <filename>**
  Captures text processed by the Verilog parser after preprocessing has occurred and copies that text to an output file, `<filename>`. Optional. Generally, preprocessing consists of the following compiler directives: `ifdef`, `else`, `elsif`, `endif`, `ifndef`, `define`, `undef`, `include`. The `line` directive attempts to preserve line numbers and file names in the output file. White space is usually preserved, but sometimes it may be deleted or added to the output file.

- **-Epretty <filename>**
  Captures text processed by the Verilog parser after preprocessing has occurred, performs some formatting for better readability, and copies that text to an output file, `<filename>`. Optional.

- **-error <msg_number>[,<msg_number>,…]**
  Changes the severity level of the specified message(s) to "error." Optional. Edit the `error` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

- **-f <filename>**
  Specifies a file with more command line arguments. Optional. Allows complex arguments to be reused without retyping. Allows gzipped input files. Nesting of `-f` options is allowed. Refer to the section "Argument Files" for more information.

- **-force_refresh <design_unit>**
  Forces the refresh of all specified design units. Optional. By default, the work library is updated; use `-work <library_name>`, in conjunction with `-force_refresh`, to update a different library (for example, `vlog -work <your_lib_name> -force_refresh`).

  When the compiler refreshes a design unit, it checks each dependency to ensure its source has not been changed and recompiled. Sometimes the dependency checking algorithm changes from release to release. This can lead to false errors during the integrity checks performed by the `-refresh` argument. An example of such a message follows:

  ```
  ** Error: (vsim-13) Recompile /u/test/dware/dware_6le_beta.dwpackages because /home/users/questasim/linux/..//synopsys.attributes has changed.
  ```

  The `-force_refresh` argument forces the refresh of the design unit, overriding any dependency checking errors encountered by the `-refresh` argument.

  A more conservative approach to working around `-refresh` dependency checks is to recompile the source code, if it is available.

- **-fsmimplicittrans**
  Enables recognition of implied same state transitions. Optional.

- **-fsmresettrans**
  Enables recognition of implicit asynchronous reset transitions. Optional. This includes asynchronous reset transitions in coverage results.
-fsmsingle
Enables recognition of FSMs having single bit current state variable. Optional.

-fsmverbose[b | t | w]
Provides information about FSMs detected, including state reachability analysis. Optional.
  b — displays only basic information.
  t — displays a transition table in addition to the basic information.
  w — displays any warning messages in addition to the basic information.

When you do not specify an argument, this switch reports all information similar to:

```
# ** Note: (vlog-1947)   FSM RECOGNITION INFO
# Fsm detected in : ../fpu/rtl/vhdl/serial_mul.vhd
# Current State Variable : s_state :
  ../fpu/rtl/vhdl/serial_mul.vhd(76)
# Clock : clk_i
# Reset States are: { waiting , busy }
# State Set is : { busy , waiting }
# Transition table is
# -------------------------------------------
# busy      =>   waiting Line : (114 => 114)
# busy      =>   busy Line : (111 => 111)
# waiting   =>   waiting Line : (120 => 120) (114 => 114)
# waiting   =>   busy Line : (111 => 111)
# -------------------------------------------
```

When you do not specify this switch, you will receive a message similar to:

```
# ** Note: (vlog-143) Detected '1' FSM/s in design unit 'serial_mul.rtl'.
```

-fsmxassign
Enables recognition of finite state machines (FSMs) containing X assignment. Optional. This option is used to detect FSMs if current state variable or next state variable has been assigned "X" value in a "case" statement. FSMs containing X-assign are otherwise not detectable.

-gen_xml <design_unit> <filename>
Produces an XML-tagged file containing the interface definition of the specified module. Optional. This option requires a two-step process where you must 1) compile <filename> into a library with vlog (without -gen_xml) then 2) execute vlog with the -gen_xml switch, for example:

```
vlib work
vlog counter.v
vlog -gen_xml counter counter.xml
```

-hazards
Detects event order hazards involving simultaneous reading and writing of the same register in concurrently executing processes. Optional. You must also specify this argument when you simulate the design with vsim. Refer to “Hazard Detection” for more details.
Note  **hazards** implicitly enables the **compat** argument. As a result, using this argument may affect your simulation results.

- **-help**
  Displays the command’s options and arguments. Optional.

- **+incdir+<directory>**
  Specifies directories to search for files included with `include` compiler directives. Optional. By default, the current directory is searched first and then the directories specified by the **+incdir** options in the order they appear on the command line. You may specify multiple **+incdir** options as well as multiple directories separated by "+" in a single **+incdir** option.

- **-incr**
  Performs an incremental compile. Optional. Default. Compiles only code that has changed. For example, if you change only one module in a file containing several modules, only the changed module will be recompiled. Note however that if the compile options change, all modules are recompiled regardless if you use **-incr** or not.

- **-isymfile**
  Generates a complete list of all imported tasks and functions (TFs). Used with DPI to determine all imported TFs that are expected by ModelSim.

- **+libcell**
  Treats all modules found and compiled by source library search as though they contained a `celldefine` compiler directive, thus marking them as cells (refer to the -y and -Y arguments of vlog, which enable source library search). Using the +libcell argument matches historical behavior of Verilog-XL with respect to source library search. Optional.

  Note  By default, wildcard logging and code coverage exclude cells. For more information, refer to the -nocovercells and -covercells arguments of vlog and to the description of wildcard logging performed by the log command.

- **+libext+<suffix>**
  Works in conjunction with the -y option. Specifies file extensions for the files in a source library directory. Optional. By default, the compiler searches for files without extensions. If you specify the +libext argument, then the compiler will search for a file with the suffix appended to an unresolved name. You may specify only one +libext option, but it may contain multiple suffixes separated by the plus character (+). The extensions are tried in the order you specify them with the +libext argument.
• **-libmap <pathname>**
  Specifies a Verilog 2001 library map file. Optional. You can omit this argument by placing the library map file as the first option on the vlog invocation (e.g., `vlog top.map top.v top_cfg.v`).

• **-libmap_verbose**
  Displays library map pattern matching information during compilation. Optional. Use to troubleshoot problems with matching filename patterns in a library file.

• **+librescan**
  Scans libraries in command-line order for all unresolved modules. Optional.

• **-line <number>**
  Starts the compiler on the specified line in the Verilog source file. Optional. By default, the compiler starts at the beginning of the file.

• **-lint**
  (optional) Issues warnings on the following lint-style static checks:
  - when Module ports are NULL.
  - when assigning to an input port.
  - when referencing undeclared variables/nets in an instantiation.

  This switch generates additional array bounds-checking code, which can slow down simulation, to check for the following:
  - index warnings for dynamic arrays
  - when an index for a Verilog unpacked variable array reference is out of bounds.

  The warnings are reported as WARNING[8]. You can also enable this option using the `Show_Lint` variable in the `modelsim.ini` file.

• **+maxdelays**
  Selects maximum delays from the "min:typ:max" expressions. Optional. If preferred, you can defer delay selection until simulation time by specifying the same option to the simulator.

• **+mindelays**
  Selects minimum delays from the "min:typ:max" expressions. Optional. If preferred, you can defer delay selection until simulation time by specifying the same option to the simulator.

• **-mixedansiports**
  Permits partial port redeclarations.
-mixedsvvh [b | s | v]
Facilitates using SystemVerilog packages at the SystemVerilog-VHDL boundary of a mixed-language design. When you compile a SystemVerilog package with -mixedsvvh, the package can be included in a VHDL design as if it were defined in VHDL itself. Optional.

- b — treats all scalars/vectors in the package as VHDL bit/bit_vector
- s — treats all scalars/vectors in the package as VHDL std_logic/std_logic_vector
- v — treats all scalars/vectors in the package as VHDL vl_logic/vl_logic_vector

-mfcu
Instructs the compiler to treat all files within a compilation command line as a single compilation unit. Optional. The default behavior is to treat each file listed in a command as a separate compilation unit, per the SystemVerilog standard. Prior versions concatenated the contents of the multiple files into a single compilation unit by default. You can also enable this option using the MultiFileCompilationUnit variable in the modelsim.ini file.

-modelsimini <ini_filepath>
Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (/).

-nodbgsym
Disables the generation of the symbols debugging database in the compiled library. The symbols debugging database is the .dbs file in the compiled library that provides information to the GUI allowing you to view detailed information about design objects at the source level. Two major GUI features that use this database include source window annotation and textual dataflow.

You should only specify this switch if you know that anyone using the library will not require this information for design analysis purposes.

-noincr
Disables incremental compile previously turned on with -incr. Optional.

-nofsmresettrans
Disables recognition of implicit asynchronous reset transitions. Optional. This has the effect of excluding asynchronous reset transitions from any coverage results.

-nofsmsingle
Disables recognition of FSMs having single bit current state variable. Optional.

-nofsmxassign
Disables recognition of FSMs containing x assignment. Optional.
• +nolibcell
Disables treating all modules found and compiled by source library search as though they contained a ‘celldefine compiler directive. That is, this argument restores the default library search behavior if you have changed it using the +libcell argument. Optional.

• -nologo
Disables the startup banner. Optional.

• +nospecify
Disables specify path delays and timing checks. Optional.

• -note <msg_number>[,<msg_number>,...]
Changes the severity level of the specified message(s) to "note." Optional. Edit the note variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

• +notimingchecks
Removes all timing check entries from the design as it is parsed. Optional.

• -novtblfixup
Causes virtual method calls in SystemVerilog class constructors to behave as they would in normal class methods, which prevents the type of a this reference from changing during construction.

This overrides default behavior, where the type of a this reference is treated as if it is a handle to the type of the active new() method while a constructor is executing (which implies that virtual method calls resolve will not execute methods of an uninitialized class type).

• +nowarn<CODE>
Disables warning messages in the category specified by <CODE>. Optional. Warnings that can be disabled include the <CODE> name in square brackets in the warning message. For example,


This warning message can be disabled by specifying +nowarnRDGN.

• -nowarn <category_number>
Prevents the specified message(s) from displaying. The <msg_number> is the number preceding the message you wish to suppress. Optional. Multiple -nowarn switches are allowed. Warnings may be disabled for all compiles via the Main window Compile > Compile Options menu command or the modelsim.ini file (refer to modelsim.ini Variables).
The warning message categories are described in Table 2-6:

<table>
<thead>
<tr>
<th>Category number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>non-LRM compliance in order to match Cadence behavior</td>
</tr>
<tr>
<td>13</td>
<td>constructs that code coverage can't handle</td>
</tr>
</tbody>
</table>

- **-O0**
  
  Lower the optimization to a minimum with **-O0** (capital oh zero). Optional. Use this to work around bugs, increase your debugging visibility on a specific cell, or when you want to place breakpoints on source lines that have been optimized out.

- **-pedanticerrors**
  
  Enforces strict compliance of the IEEE Std 1800-2005 in the following cases:
  
  - Using "new" for queues is not legal. When strict compliance is not enforced, use of "new" creates a queue of the specified size where all elements are initialized to the default value of the queue element type.
  
  - Using underscore character (_) in sized, based literals is not legal. When you specify this switch, vlog will error on literals such as 2'b_01.
  
  - Using class extern method prototypes with lifetime (automatic/static) designations. When you specify this switch, this scenario produces an LRM-compliance error, otherwise you will receive a warning.

  Enforces strict compliance of the IEEE Std 1800-2005 in the following case:
  
  - Using “cover bool@clk” as a PSL statement.

  This argument also produces a report of mismatched ‘else directives. Optional.

- **-quiet**
  
  Disables 'Loading' messages. Optional.

- **-R [<simargs>]**
  
  Instructs the compiler to invoke **vsim** after compiling the design. The compiler automatically determines which top-level modules are to be simulated. The command line arguments following -R are passed to the simulator, not the compiler. Place the -R option at the end of the command line or terminate the simulator command line arguments with a single "-" character to differentiate them from compiler command line arguments.

  The -R option is not a Verilog-XL option, but it is used by ModelSim to combine the compile and simulate phases together as you may be used to doing with Verilog-XL. It is not recommended that you regularly use this option because you will incur the unnecessary overhead of compiling your design for each simulation run. Mainly, it is provided to ease the transition to ModelSim.
-refresh
Regenerates a library image. Optional. By default, the work library is updated. To update a different library, use `-work <library_name>` with `-refresh` (for example, vlog -work <your_lib_name> -refresh). If a dependency checking error occurs which prevents the refresh, use the vlog `-force_refresh` argument. See vlog examples for more information. You may use a specific design name with `-refresh` to regenerate a library image for that design, but you may not use a file name.

-sfcu
Instructs the compiler to treat all files within a compilation command line as a separate compilation units. This is the default behavior and is the inverse of the behavior of `-mfcu`. This switch will override the MultiFileCompilationUnit variable if it is set to "1" in the modelsim.ini file.

-source
Displays the associated line of source code before each error message that is generated during compilation. Optional; by default, only the error message is displayed.

-s
Instructs the compiler not to load the standard package. Optional. This argument should only be used when you are compiling the sv_std package.

-sv
Enables SystemVerilog features and keywords. Optional. By default ModelSim follows the rules of IEEE Std 1364-2001 and ignores SystemVerilog keywords. If a source file has a ".sv" extension, ModelSim will automatically parse SystemVerilog keywords.

-suppress <msg_number>[,<msg_number>,…]
Prevents the specified message(s) from displaying. The <msg_number> is the number preceding the message you wish to suppress. Optional. You cannot suppress Fatal or Internal messages. Edit the suppress variable in the modelsim.ini file to set a permanent default. Refer to “Changing message Severity Level” for more information.

-time
Reports the "wall clock time" vlog takes to compile the design. Optional. Note that if many processes are running on the same system, wall clock time may differ greatly from the actual "cpu time" spent on vlog.

-timescale <time_units>/<time_precision>
Specifies the default timescale for modules not having an explicit timescale directive in effect during compilation. Optional. The format of the -timescale argument is the same as that of the `timescale directive. The format for `<time_units>` and `<time_precision>` is `<n><units>`. The value of `<n>` must be 1, 10, or 100. The value of `<units>` must be fs, ps, ns, us, ms, or s. In addition, the `<time_units>` must be greater than or equal to the `<time_precision>`.
Commands

vlog

- **+typdelays**
  Selects typical delays from the "min:typ:max" expressions. Default. If preferred, you can defer delay selection until simulation time by specifying the same option to the simulator.

- **-u**
  Converts regular Verilog identifiers to uppercase. Allows case insensitivity for module names. Optional.

- **-v <library_file>**
  Specifies a source library file containing module and UDP definitions. Optional. Refer to “Verilog-XL Compatible Compiler Arguments” for more information.

  After all explicit filenames on the vlog command line have been processed, the compiler uses the -v option to find and compile any modules that were referenced but not yet defined. Modules and UDPs within the file are compiled only if they match previously unresolved references. Multiple -v options are allowed. See additional discussion in the examples.

- **-version**
  Returns the version of the compiler as used by the licensing tools. Optional.

- **-vlog01compat**

- **-vlog95compat**
  Disables Verilog 2001 keywords, which ensures that code that was valid according to the 1364-1995 spec can still be compiled. By default ModelSim follows the rules of IEEE Std 1364-2001. Some requirements in 1364-2001 conflict with requirements in 1364-1995. Optional. Edit the vlog95compat variable in the modelsim.ini file to set a permanent default.

- **-vmake**
  Generates a complete record of all command line data and files accessed during the compile of a design. This data is then used by the vmake command to generate a comprehensive makefile for recompiling the design library. By default, vcom stores compile data needed for the -refresh switch and ignores compile data not needed for -refresh. The -vmake switch forces inclusion of all file dependencies and command line data accessed during a compile, whether they contribute data to the initial compile or not. Executing this switch can increase compile time in addition to increasing the accuracy of the compile. See the vmake command for more information.

  -warning <msg_number>[, <msg_number>,...]
  Changes the severity level of the specified message(s) to "warning." Optional. Edit the warning variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

- **-work <library_name>**
  Specifies a logical name or pathname of a library that is to be mapped to the logical library work. Optional: by default, the compiled design units are added to the work library. The specified pathname overrides the pathname specified for work in the project file.
-y <library_directory>

Specifies a source library directory containing definitions for modules, packages, interfaces, and user-defined primitives (UDPs). Usually, this is a directory of source files that you want to scan if the compiled versions do not already exist in a library. Optional. Refer to “Verilog-XL Compatible Compiler Arguments” for more information.

After all explicit filenames on the vlog command line have been processed, the compiler uses the -y option to find and compile any modules that were referenced but not yet defined. Files within this directory are compiled only if the file names match the names of previously unresolved references. Multiple -y options are allowed. You will need to specify a file suffix by using -y in conjunction with the +libext+<suffix> option if your filenames differ from your module names. See additional discussion in the examples.

Note

Any -y arguments that follow a -refresh argument on a vlog command line are ignored. Any -y arguments that come before the -refresh argument on a vlog command line are processed.

<filename>

Specifies the name of the Verilog source code file to compile. One filename is required. Multiple filenames can be entered separated by spaces. Wildcards can be used.

Examples

- Compile the Verilog source code contained in the file example.vlg.

  vlog example.vlg

- After compiling top.v, vlog will scan the file und1 for modules or primitives referenced but undefined in top.v. Only referenced definitions will be compiled.

  vlog top.v -v und1

- After compiling top.v, vlog will scan the vlog_lib library for files with modules with the same name as primitives referenced, but undefined in top.v. The use of +libext+.v+.u implies filenames with a .v or .u suffix (any combination of suffixes may be used). Only referenced definitions will be compiled.

  vlog top.v +libext+.v+.u -y vlog_lib

The -work option specifies mylib as the library to regenerate. -refresh rebuilds the library image without using source code, allowing models delivered as compiled libraries without source code to be rebuilt for a specific release of ModelSim.

- If your library contains VHDL design units, be sure to regenerate the library with the vcom command using the -refresh option as well. Refer to “Regenerating Your Design Libraries” for more information.

  vlog -work mylib -refresh
• The **-incr** option determines whether or not the module source or compile options have changed as `module1.v` is parsed. If no change is found, the code generation phase is skipped. Differences in compile options are determined by comparing the compiler options stored in the `_info` file with the compiler options given. They must match exactly.

```
  vlog module1.v -u -O0 -incr
```

• The **-timescale** option specifies the default timescale for `module1.v`, which did not have an explicit timescale directive in effect during compilation. Quotes are necessary because the argument contains white spaces.

```
  vlog module1.v -timescale "1 ns / 1 ps"
```
vmake

The vmake utility allows you to use a UNIX or Windows MAKE program to maintain individual libraries. You run vmake on a compiled design library. This utility operates on multiple source files per design unit; it supports Verilog include files as well as Verilog and VHDL PSL vunit files.

Note

If a design is spread across multiple libraries, then each library must have its own makefile and you must build each one separately.

By default, the output of vmake is sent to stdout—however, you can send the output to a makefile by using the shell redirect operator (>) along with the name of the file. You can then run the makefile with a version of MAKE (not supplied with ModelSim) to reconstruct the library. This command must be invoked from either the UNIX or the Windows/DOS prompt.

A MAKE program is included with Microsoft Visual C/C++, as well as many other program development environments.

After running the vmake utility, MAKE recompiles only the design units (and their dependencies) that have changed. You run vmake only once; then you can simply run MAKE to rebuild your design. If you add new design units or delete old ones, you should re-run vmake to generate a new makefile.

The vmake utility ignores library objects compiled with -nodebug.

Syntax


Arguments

- -cygdrive
  Generates a makefile that uses a path specified with UNIX pathname conventions. Use this argument if you are using cygwin v3.81 or later (which no longer supports Windows conventions for drive and pathname). Optional.
- -du <design_unit_name>
  Specifies that a vmake file will be generated only for the specified design unit. Optional. You can specify this argument any number of times for a single vmake command.
- -f <filename>
  Specifies a file to read command line arguments from. Optional.
- -fullsrcpath
  Produces complete source file paths within generated makefiles. Optional. By default source file paths are relative to the directory in which compiles originally occurred. This argument
makes it possible to copy and evaluate generated makefiles within directories that are different from where compiles originally occurred.

- **-help**
  Displays the command’s options and arguments. Optional.

- **-ignore**
  Omits a make rule for the named primary design unit and its secondary design units. Optional.

- **<library_name>**
  Specifies the library name; if none is specified, then `work` is assumed. Optional.

- **-modelsimini <ini_filepath>**
  Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (/).

**Examples**

- To produce a makefile for the work library:
  ```
  vmake >mylib.mak
  ```

- To run `vmake` on libraries other than `work`:
  ```
  vmake mylib >mylib.mak
  ```

- To rebuild `mylib`, specify its makefile when you run MAKE:
  ```
  make -f mylib.mak
  ```

- To use `vmake` and `MAKE` on your `work` library:
  ```
  C:\MIXEDHDL> vmake >makefile
  ```

- To edit an HDL source file within the work library:
  ```
  C:\MIXEDHDL> make
  ```
  Your design gets recompiled for you. You can change the design again and re-run MAKE to recompile additional changes.

- To run `vmake` on libraries other than `work`:
  ```
  C:\MIXEDHDL> vmake mylib >mylib.mak
  ```

- To rebuild `mylib`, specify its makefile when you run MAKE:
  ```
  C:\MIXEDHDL> make -f mylib.mak
  ```
The **vmap** command defines a mapping between a logical library name and a directory by modifying the *modelsim.ini* file.

With no arguments, **vmap** reads the appropriate *modelsim.ini* file(s) and prints to the transcript the current logical library to physical directory mappings.

**Syntax**

```
vmap [-c | -del <logical_name> ... | <logical_name> [path] ]
```

**Arguments**

- **-c**
  (optional) Copies the default *modelsim.ini* file from the ModelSim installation directory to the current directory.
  This argument is intended only for making a copy of the default *modelsim.ini* file to the current directory. Do not use it while making your library mappings or the mappings may end up in the incorrect copy of the *modelsim.ini*.

- **-del <logical_name> ...**
  (optional) Deletes the mapping specified by `<logical_name>` from the current project file. You can specify multiple logical name arguments to the -del switch to delete multiple library mappings.

- **-help**
  (optional) Displays options and arguments of vmap.

- `<logical_name> [path]`
  (optional) Maps a logical library name to the specified physical library.
  If you do not specify `<path>` the command returns the current mapping for `<logical_name>`.

**Examples**

- Map two logical libraries to the physical library “work”, then delete the two logical libraries:
  ```
  vlib work
  vmap library1 work
  vmap library2 work
  ```

- Display information about the logical library “library1”:
  ```
  vmap library1
  ```

- Delete the logical library mappings:
  ```
  vmap -del library1 library2
  ```
The `vsim` command is used to invoke the VSIM simulator, to view the results of a previous simulation run (when invoked with the `-view` switch), or to view coverage data stored in the UCDB from a previous simulation run (when invoked with the `-viewcov` switch).

You can simulate a VHDL configuration or an entity/architecture pair; a Verilog module or configuration. If you specify a VHDL configuration, it is invalid to specify an architecture. During elaboration `vsim` determines if the source has been modified since the last compile.

This command may be used in batch mode from the Windows command prompt. Refer to “Batch Mode” for more information on the VSIM batch mode.

To manually interrupt design loading use the Break key or `<Ctrl-c>` from a shell.

You can invoke `vsim` from a command prompt or in the Transcript window of the Main window. You can also invoke it from the GUI by selecting Simulate > Start Simulation.

All arguments to the `vsim` command are case sensitive; for example, `-g` and `-G` are not equivalent.

**Syntax**

**Note**

This Syntax section presents all of the `vsim` switches in alphabetical order, while the Arguments section groups the arguments into the following sections:

- Arguments, all languages
- Arguments, VHDL
- Arguments, Verilog
- Arguments, object

```bash
vsim [options]
[options]:
    [-absentisempty] [+alt_path_delays] [-assertfile <filename>]

    [-c] [-capacity] [-colormap new]

    [-debugDB=<db_pathname>] [+delayed_timing_checks] [-display <display_spec>] [-displaymsgmode both | tran | wlf] [-do "<command_string>" | <macro_file_name>] [-dpiexportobj <objfile>] [+dumpports+collapse | +dumpports+nocollapse] [+dumpports+direction] [+dumpports+no_strength_range] [+dumpports+unique]

    [-error <msg_number>[,<msg_number>,…]]
    [-errorfile <filename>]

    [-f <filename>] [-fatal <msg_number>[,<msg_number>,…]]
```
[-g<Name>=<Value> …] [-G<Name>=<Value> …] [-gblso <filename>]
[-geometry <geometry_spec> ] [-gui]
[-hazards] [-help]
[-i] [-installcolormap]
[-keeploaded] [-keeploadedrestart] [-keepstdout]
[-l <filename>] [-lib <libname>] [-L <library_name> …]
[-Lf <library_name> …]
[<library_name>.<design_unit>]

[+maxdelays] [+mindelays]
[-modelsimini <ini_filepath>]
[-msgmode both | tran | wlf] [-multisource_delay min | max | latest]
[+multisource_int_delays]
[-name <name>] [+no_autdtc] [-noautoldlibpath] [-nodpiexports]
[+no_cancelled_e_ms] [+no_glitch_msg] [+no_neg_tchk] [+no_notifier]
[+no_path_edge] [+no_pulse_msg] [-no_risefall_delaynets]
[+no_show_cancelled_e] [+no_tchk_msg] [-nocollapse] [-nocapacity] [-nocompress]
[-noexcludehiz] [-nofileshare] [-noimmedca]
[+noglitch] [+nosdferror] [+nosdfwarn]
[+nospecify] [-note <msg_number>[, <msg_number>,…]]
[+notimingchecks] [+nowarnBSOB] [+nowarn<CODE>] [+ntc_warn]
[-onfinish ask | stop | exit]
[-pli "<object list>"]
[-plicompatdefault [ latest | 2005 | 2001 ]] [+<plusarg>] [-printsimstats]
[+pulse_e/<percent>] [+pulse_e_style_ondetect] [+pulse_e_style_onevent]
[+pulse_r/<percent>]
[-quiet]
[-runinit]

[+sdf_iopath_to_prim_ok]
[+sdf_nocheck_celltype]
[+sdfmin | -sdf typ | -sdfmax[@<delayScale>] ] [ <instance>=<sdf_filename>]
[+sdfmaxerrors <n>] [-sdfnoerror] [+sdfverbose]
[-std_input <filename>] [-std_output <filename>] [+show_cancelled_e] [-strictvital]
[-suppress <msg_number>[, <msg_number>,…]] [-sv_lib <shared_obj>]
[-sv_liblist <filename>] [-sv_root <dirname>]
[-sync]
[-t <multiplier>[<time_unit>]] [-tab <tabfile>] [-tag <string>] [-title <title>]
[+trace_foreign <int>] [+transport_int_delays]
[+transport_path_delays] [+typdelays]

[-v2k_int_delays][-vcdstim [ <instance>=<filename>]
[-version] [-view <dataset_name>=<WLF_filename>]
[-viewcov <dataset_name>=<UCDB_filename>] [-visual <visual>] [-vital2.2b]
Commands

vsim

[-warning <msg_number> [, <msg_number>, ... ]] [-wlf <filename>] [-wlfcachesize <n>]
[-wlfcollapsedelta] [-wlfcollapsetime] [-wlfccompressequal] [-wlflock]
[-wlfnocollapse] [-wlfnocompress] [-wlfnodeleteonquit] [-wlfnoopt]
[-wlfopt] [-wlfsimcachesize <n>] [-wlfsimlim <size>] [-wlftlim <duration>]
[-wlftthreads | -wlfnothreads]

Arguments, all languages

-assertfile <filename>

Designates an alternative file for recording VHDL assertion messages. Optional. An
alternate file may also be specified by the AssertFile modelsim.ini variable. By default,
assertion messages are output to the file specified by the TranscriptFile variable in the
modelsim.ini file (refer to “Creating a Transcript File”).

-c

Specifies that the simulator is to be run in command-line mode. Optional. Refer to “Modes
of Operation” for more information.

-capacity

Enables the fine-grain analysis display of memory capacity (coarse-grain analysis is enabled
by default). Optional.

-colormap new

Specifies that the window should have a new private colormap instead of using the default
colormap for the screen. Optional.

-display <display_spec>

Specifies the name of the display to use. Optional. Does not apply to Windows platforms.
For example:

- display :0

-displaymsgmode both | tran | wlf

Controls the transcription of $display system task messages to the transcript and/or the
Message Viewer. Refer to the section “Message Viewer Window” in the User’s Manual for
more information and the displaymsgmode .ini file variable.

      both — outputs messages to both the transcript and the WLF file.

      tran — outputs messages only to the transcript, therefore they are not available in the
Message Viewer. Default behavior

      wlf — outputs messages only to the WLF file/Message Viewer, therefore they are not
available in the transcript.

The display system tasks displayed with this functionality include: $display, $strobe,
$monitor, $write as well as the analogous file I/O tasks that write to STDOUT, such as
fwrite or $fdisplay.
• **-debugDB=\<db_pathname>**
  Instructs ModelSim to generate database of dataflow connectivity information to be used for post-sim debug in the Dataflow window. Optional. The database pathname should have a `.dbg` extension. If a database pathname is not specified, ModelSim creates a database file named `vsim.dbg` in the current directory. See Post-Simulation Debug Flow Details.

• **-do "\<command_string\>" | \<macro_file_name\>**
  Instructs `vsim` to use the command(s) specified by `<command_string>` or the macro file named by `<macro_file_name>` rather than the startup file specified in the `.ini` file, if any. Optional. Multiple commands should be separated by semi-colons (;).

• **+dumpports+collapse | +dumpports+nocollapse**
  Determines whether vectors (VCD id entries) in dumpports output or collapsed or not. Optional. The default behavior is collapsed, and can be changed by setting the `DumpportsCollapse` variable in the `modelsim.ini` file.

• **+dumpports+direction**
  Modifies the format of extended VCD files to contain direction information. Optional.

• **+dumpports+no_strength_range**
  Ignores strength ranges when resolving driver values for an extended VCD file. Optional. This argument is an extension to the IEEE 1364 specification. Refer to “Resolving Values” for additional information.

• **+dumpports+unique**
  Generates unique VCD variable names for ports in a VCD file even if those ports are connected to the same collapsed net. Optional.

• **-error <msg_number>,<msg_number>,…**
  Changes the severity level of the specified message(s) to "error." Optional. Edit the `error` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

• **-errorfile <filename>**
  Designates an alternative file for recording error messages. Optional. An alternate file may also be specified by the `ErrorFile` modelsim.ini variable. By default, error messages are output to the file specified by the `TranscriptFile` variable in the `modelsim.ini` file (refer to “Creating a Transcript File”).

• **-f <filename>**
  Specifies a file with more `vsim` command arguments. Optional. Allows complex argument strings to be reused without retyping.
  Refer to the section "Argument Files" for more information.
• **-fatal <msg_number>[,<msg_number>,…]**

Changes the severity level of the specified message(s) to "fatal." Optional. Edit the fatal variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

• **-g<Name>=<Value> …**

(conditional) Assigns a value to all specified VHDL generics and Verilog parameters that have not received explicit values in generic maps, instantiations, or via defparams (such as top-level generics/parameters and generics/parameters that would otherwise receive their default values). No spaces are allowed anywhere in the specification, except within quotes when specifying a string value. Multiple -g options are allowed, one for each generic/parameter, specified as a space separated list.

- **<Name>** — Name of a generic/parameter, exactly as it appears in the VHDL source (case is ignored) or Verilog source. Name may be prefixed with a relative or absolute hierarchical path to select generics in an instance-specific manner. For example, specifying -g/top/u1/tpd=20ns on the command line would affect only the tpd generic on the /top/u1 instance, assigning it a value of 20ns. Specifying -gu1/tpd=20ns affects the tpd generic on all instances named u1. Specifying-gtpd=20ns affects all generics named tpd.

- **<Value>** — Specifies an appropriate value for the declared data type of a VHDL generic or any legal value for a Verilog parameter. Make sure the value you specify for a VHDL generic is appropriate for VHDL declared data types. Integers are treated as signed values. For example, -gp=-10 overwrites the parameter p with the signed value of -10.

If more than one -g option selects a given generic the most explicit specification takes precedence. For example,

```
vsim -g/top/ram/u1/tpd_hl=10ns -gtpd_hl=15ns top
```

This command sets tpd_hl to 10ns for the /top/ram/u1 instance. However, all other tpd_hl generics on other instances will be set to 15ns.

Limitation: In general, generics/parameters of composite type (arrays and records) cannot be set from the command line. However, you can set string arrays, std_logic vectors, and bit vectors if they can be set using a quoted string. For example,

```
-gstrgen="This is a string"
-gslv="01001110"
```

The quotation marks must make it into vsim as part of the string because the type of the value must be determinable outside of any context. Therefore, when entering this command from a shell, put single quotes (‘’) around the string. For example:

```
-gstrgen="This is a string"
```

If working within the ModelSim GUI, you would enter the command as follows:

```
{-gstrgen="This is a string"}
```
You can also enclose the value escaped quotes (\"), for example:

\-gstrgen=\\"This is a string\\"

- -G<Name>=<Value> … (optional) Same as -g (see above) except that it will also override generics/parameters that received explicit values in generic maps, instantiations, or from defparams. No spaces are allowed anywhere in the specification, except within quotes when specifying a string value. This argument is the only way for you to alter the generic/parameter, such as its length, (other than its value) after the design has been loaded.

<Name> — Name of a generic/parameter, exactly as it appears in the VHDL source (case is ignored) or Verilog source. Name may be prefixed with a relative or absolute hierarchical path to select generics in an instance-specific manner. For example, specifying -G/top/u1/tpd=20ns on the command line would affect only the tpd generic on the /top/u1 instance, assigning it a value of 20ns. Specifying -Gu1/tpd=20ns affects the tpd generic on all instances named u1. Specifying -Gtpd=20ns affects all generics named tpd.

<Value> — Specifies an appropriate value for the declared data type of a VHDL generic or any legal value for a Verilog parameter. Make sure the value you specify for a VHDL generic is appropriate for VHDL declared data types. Integers are treated as signed values. For example, -Gp=-10 overwrites the parameter p with the signed value of -10.

- -gblso <filename>
On UNIX platforms, loads PLI/FLI shared objects with global symbol visibility. Essentially all data and functions are exported from the specified shared object and are available to be referenced and used by other shared objects. This option may also be specified with the GlobalSharedObjectsList variable in the modelsim.ini file. Optional.

- -geometry <geometry_spec>
Specifies the size and location of the main window. Optional. Where <geometry_spec> is of the form:

WxH+X+Y

- -gui
Starts the ModelSim GUI without loading a design and redirects the standard output (stdout) to the GUI Transcript window. Optional.

- -help
Displays the command’s options and arguments. Optional.

- -i
Specifies that the simulator is to be run in interactive mode. Optional.

- -installcolormap
For UNIX only. Causes vsim to use its own colormap so as not to hog all the colors on the display. This is similar to the -install switch on Netscape. Optional.
Commands

vsim

-keeploaded
Prevents the simulator from unloading/reloading any FLI/PLI/VPI shared libraries when it restarts or loads a new design. Optional. The shared libraries will remain loaded at their current positions. User application code in the shared libraries must reset its internal state during a restart in order for this to work effectively.

-keeploadedrestart
Prevents the simulator from unloading/reloading any FLI/PLI/VPI shared libraries during a restart. Optional. The shared libraries will remain loaded at their current positions. User application code in the shared libraries must reset its internal state during a restart in order for this to work effectively.

We recommend using this option if you’ll be doing warm restores after a restart and the user application code has set callbacks in the simulator. Otherwise, the callback function pointers might not be valid if the shared library is loaded into a new position.

-keepstdout
For use with foreign programs. Instructs the simulator to not redirect the stdout stream to the Main window. Optional.

-l <filename>
Saves the contents of the Transcript window to <filename>. Optional. Default is taken from the TranscriptFile variable (initially set to transcript) in the modelsim.ini.

-L <library_name> …
Specifies the library to search for design units instantiated from Verilog and for VHDL default component binding. Refer to “Library Usage” for more information. If multiple libraries are specified, each must be preceded by the -L option. Libraries are searched in the order in which they appear on the command line.

-Lf <library_name> …
Same as -L but libraries are searched before ‘uselib directives. Refer to “Library Usage” for more information. Optional.

-lib <libname>
Specifies the default working library where vsim will look for the design unit(s). Optional. Default is "work".

-msgmode both | tran | wlf
Specifies the location(s) for the simulator to output elaboration and runtime messages. Refer to the section "Message Viewer Window" in the User’s Manual for more information.

both — outputs messages to both the transcript and the WLF file. Default behavior
tran — outputs messages only to the transcript, therefore they are not available in the Message Viewer.
wlf — outputs messages only to the WLF file/Message Viewer, therefore they are not available in the transcript.
-modelsimini <ini_filepath>
Loads an alternate initialization file that replaces the current initialization file. Overrides the file path specified in the MODELSIM environment variable. Specifies either an absolute or relative path to the initialization file. On Windows systems the path separator should be a forward slash (/).

-mutisource_delay min | max | latest
Controls the handling of multiple PORT or INTERCONNECT constructs that terminate at the same port. Optional. By default, the Module Input Port Delay (MIPD) is set to the max value encountered in the SDF file. Alternatively, you may choose the min or latest of the values. If you have a Verilog design and want to model multiple interconnect paths independently, use the +multisource_int_delays argument.

+mutisource_int_delays
Enables multisource interconnect delay with pulse handling and transport delay behavior. Works for both Verilog and VITAL cells. Optional.

Use this argument when you have interconnect data in your SDF file and you want the delay on each interconnect path modeled independently. Pulse handling is configured using the +pulse_int_e and +pulse_int_r switches (described below).

The +multisource_int_delays argument cannot be used if you compiled using the -novital argument to vcom. The -novital argument instructs vcom to implement VITAL functionality using VHDL code instead of accelerated code, and multisource interconnect delays cannot be implemented purely within VHDL.

-name <name>
Specifies the application name used by the interpreter for send commands. This does not affect the title of the window. Optional.

-noautoldlibpath
Disables the default internal setting of LD_LIBRARY_PATH, enabling you to set it yourself. Optional. Use this argument to make sure that LD_LIBRARY_PATH is not set automatically while you are using the GUI.

-nocapacity
Disables the display of both coarse-grain and fine-grain analysis of memory capacity. Optional.

-nocompress
Causes VSIM to create uncompressed checkpoint files. Optional. This option may also be specified with the CheckpointCompressMode variable in the modelsim.ini file.

-noimmedca
Causes Verilog event ordering to occur without enforced prioritization—continuous assignments and primitives are not run before other normal priority processes scheduled in
the same iteration. Use this argument to prevent the default event ordering where continuous assignments and primitives are run with "immediate priority." Optional.

- **+no_notifier**
  Disables the toggling of the notifier register argument of all timing check system tasks. Optional. By default, the notifier is toggled when there is a timing check violation, and the notifier usually causes a UDP to propagate an X. This argument suppresses X propagation in both Verilog and VITAL for the entire design.

- **+nospecify**
  Disables specify path delays and timing checks in Verilog. Optional.

- **+no_tchk_msg**
  Disables error messages generated when timing checks are violated. Optional. For Verilog, it disables messages issued by timing check system tasks. For VITAL, it overrides the MsgOn arguments and generics.
 Notifier registers are still toggled and may result in the propagation of Xs for timing check violations.

- **-note <msg_number>[,<msg_number>,…]**
  Changes the severity level of the specified message(s) to "note." Optional. Edit the note variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

- **-notimingchecks**
  Disables Verilog timing checks. (This option sets the generic TimingChecksOn to FALSE for all VHDL Vital models with the Vital_level0 or Vital_level1 attribute. Generics with the name TimingChecksOn on non-VITAL models are unaffected.) Optional. By default, Verilog timing check system tasks ($setup, $hold,…) in specify blocks are enabled. For VITAL, the timing check default is controlled by the ASIC or FPGA vendor, but most default to enabled.

- **-plicompatdefault [ latest | 2005 | 2001 ]**
  Specifies the VPI object model behavior within vsim. This switch applies globally, not to individual libraries.

  latest — This is equivalent to the "2009" argument. This is the default behavior if you do not specify this switch or if you specify the switch without an argument.

  2009 — Instructs vsim to use the object models as defined in IEEE Std P1800-2009 (unapproved draft standard). You can also use "09" as an alias.

  2005 — Instructs vsim to use the object models as defined in IEEE Std 1800-2005 and IEEE Std 1364-2005. You can also use "05" as an alias.

  2001 — Instructs vsim to use the object models as defined in IEEE Std 1364-2001. When you specify this argument, SystemVerilog objects will not be accessible. You can also use "01" as an alias.
You can also control this behavior with the `PliCompatDefault` variable in the `modelsim.ini` file, where the `-plicompatdefault` argument will override the `PliCompatDefault` variable.

You should note that there are a few cases where the 2005 VPI object model is incompatible with the 2001 model, which is inherent in the specifications.

Refer to the appendix "Verilog Interfaces to C" in the User’s Manual for more information.

- **-printsimstats**
  Prints the output of the `simstats` command to the screen at the end of simulation before exiting. Edit the `PrintSimStats` variable in the `modelsim.ini` file to set the simulation to print the `simstats` data by default.

- **+pulse_int_e/\langle\text{percent}\rangle**
  Controls how pulses are propagated through interconnect delays, where `<\text{percent}>` is a number between 0 and 100 that specifies the error limit as a percentage of the interconnect delay. Optional. Used in conjunction with `+multisource_int_delays` (see above). This option works for both Verilog and VITAL cells, though the destination of the interconnect must be a Verilog cell. The source may be VITAL or Verilog.

  A pulse greater than or equal to the error limit propagates to the output in transport mode (transport mode allows multiple pending transitions on an output). A pulse less than the error limit and greater than or equal to the rejection limit (see `+pulse_int_r/\langle\text{percent}\rangle` below) propagates to the output as an X. If the rejection limit is not specified, then it defaults to the error limit. For example, consider an interconnect delay of 10 along with a `+pulse_int_e/80` option. The error limit is 80% of 10 and the rejection limit defaults to 80% of 10. This results in the propagation of pulses greater than or equal to 8, while all other pulses are filtered.

- **+pulse_int_r/\langle\text{percent}\rangle**
  Controls how pulses are propagated through interconnect delays, where `<\text{percent}>` is a number between 0 and 100 that specifies the rejection limit as a percentage of the interconnect delay. Optional. This option works for both Verilog and VITAL cells, though the destination of the interconnect must be a Verilog cell. The source may be VITAL or Verilog.

  A pulse less than the rejection limit is filtered. If the error limit is not specified by `+pulse_int_e` then it defaults to the rejection limit.

- **-quiet**
  Disable 'Loading' messages during batch-mode simulation. Optional.

- **-runinit**
  Initializes non-trivial static SystemVerilog variables, for example expressions involving other variables and function calls, before displaying the simulation prompt.

- **+sdf_iopath_to_prim_ok**
  Prevents `vsim` from issuing an error when it cannot locate specify path delays to annotate. If you specify this argument, IOPATH statements are annotated to the primitive driving the
destination port if a corresponding specify path is not found. Optional. Refer to “SDF to Verilog Construct Matching” for additional information.

- **-sdfmin | -sdfTyp | -sdfmax[@<delayScale>] [instance=]sdf_filename**
  (optional) Annotates VITAL or Verilog cells in the specified SDF file (a Standard Delay Format file) with minimum, typical, or maximum timing.
  
  @<delayScale> — scales all values by the specified value. For example, if you specify -sdfmax@1.5, all maximum values in the SDF file are scaled to 150% of their original value.

  instance= — specifies a specific instance for the associated SDF file. Use this when not performing backannotation at the top level.

  sdf_filename — specifies the file containing the SDF information.

- **-sdfminr | -sdfTypr | -sdfmaxr[@<delayScale>] [instance=]sdf_filename**
  (optional) Specifies when an instance of a black-boxed (vopt -bbox) module, which has a associated, default SDF file is to be re-annotated with minimum, typical, or maximum timing from the specified SDF file.

  @<delayScale> — scales all values by the specified value. For example, if you specify -sdfmax@1.5, all maximum values in the SDF file are scaled to 150% of their original value.

  instance= — specifies a specific instance for the associated SDF file. Use this when not performing backannotation at the top level.

  sdf_filename — specifies the file containing the SDF information.

---

**Note**

The simulator assumes that the instance/timing object hierarchy in the new SDF file is compatible with the SDF file specified during blackboxing with the vopt command.

The following is a simple usage flow:

```sh
# Assume module top contains three instances (u1, u2, and u3)
# of a black-boxed module bboxMod.
vlib work
vlog bboxMod.v

# blackbox bboxMod and annotate with sdf1.
vopt -bbox bboxMod -o bboxMod_opt -sdfmin bboxMod=sdf1
vlog top.v

# Use the default SDF file sdf1 for the blackbox instance of u1,
# but override the SDF for u2 and u3.
vsim top +sdf_verbose -sdfTypr /top/u2=sdf2 -sdfmaxr /top/u3=sdf3
run -all
```
-sdfmaxerrors <n>
Controls the number of Verilog SDF missing instance messages to be generated before terminating vsim. Optional. <n> is the maximum number of missing instance error messages to be emitted. The default number is 5.

-sdfnoerror
Errors issued by the SDF annotator while loading the design prevent the simulation from continuing, whereas warnings do not. Changes SDF errors to warnings so that the simulation can continue. Optional.

-sdfnowarn
Disables warnings from the SDF reader. Optional. Refer to “VHDL Simulation” for an additional discussion of SDF.

+sdf_verbose
Turns on the verbose mode during SDF annotation. The Transcript window provides detailed warnings and summaries of the current annotation as well as information including the module name, source file name and line number. Optional.

-suppress <msg_number>,<msg_number>...
Prevents the specified message(s) from displaying. Optional. You cannot suppress Fatal or Internal messages. Edit the suppress variable in the modelsim.ini file to set a permanent default. Refer to “Changing Message Severity Level” for more information.

-sync
Executes all X server commands synchronously, so that errors are reported immediately. Does not apply to Windows platforms.

t [multiplier]<time_unit>
Specifies the simulator time resolution. Optional. <time_unit> must be one of the following:

fs, ps, ns, us, ms, sec

The default is 1ps; the optional <multiplier> may be 1, 10 or 100. Note that there is no space between the multiplier and the unit (for example, 10fs, not 10 fs).

If you omit the -t argument, the default simulator time resolution depends on design type:

- In a VHDL design—the value specified for the Resolution variable in modelsim.ini is used.
- In a Verilog design with ‘timescale directives—the minimum specified time precision of all directives is used.
- In a Verilog design with no ‘timescale directives—the value specified for the Resolution variable in the modelsim.ini file is used.
- In a mixed design with VHDL on top—the value specified for the Resolution variable in the modelsim.ini file is used.
In a mixed design with Verilog on top—

- for Verilog modules not under a VHDL instance: the minimum value specified for their `timescale` directives is used.
- for Verilog modules under a VHDL instance: all their `timescale` directives are ignored (the minimum value for `timescale` directives in all modules not under a VHDL instance is used).

If there are no `timescale` directives in the design, the value specified for the Resolution variable in modelsim.ini is used.

**Tip:** After you have started a simulation, you can view the current simulator resolution by using the `report` command as follows:

```
report simulator state
```

- `-tab <tabfile>`
  Specifies the location of a Synopsys VCS “tab” file (.tab), which the simulator uses to automate the registration of PLI functions in the design.

  `<tabfile>` — The location of a .tab file contains information about PLI functions. The tool expects the .tab file to be based on Synopsys VCS version 7.2 syntax. Because the format for this file is non-standard, changes to the format are outside of the control of Mentor Graphics.

- `-tag <string>`
  Specifies a string tag to append to foreign trace filenames. Optional. Used with the `-trace_foreign <int>` option. Used when running multiple traces in the same directory.

- `-title <title>`
  Specifies the title to appear for the ModelSim Main window. Optional. If omitted the current ModelSim version is the window title. Useful when running multiple simultaneous simulations. Text strings with spaces must be in quotes (e.g., "my title").

- `-trace_foreign <int>`
  Creates two kinds of foreign interface traces: a log of what functions were called, with the value of the arguments, and the results returned; and a set of C-language files to replay what the foreign interface side did.

  The purpose of the logfile is to aid the debugging of your PLI/VPI code. The primary purpose of the replay facility is to send the replay file to MTI support for debugging co-simulation problems, or debugging problems for which it is impractical to send the PLI/VPI code.

- `+transport_int_delays`
  Selects transport mode with pulse control for single-source nets (one interconnect path). Optional. By default interconnect delays operate in inertial mode (pulses smaller than the
delay are filtered). In transport mode, narrow pulses are propagated through interconnect delays.

This option works for both Verilog and VITAL cells, though the destination of the interconnect must be a Verilog cell. The source may be VITAL or Verilog. This option works independently from `+multisource_int_delays`.

- `-vcdstim [<instance>=]<filename>`
  Specifies a VCD file from which to re-simulate the design. Optional. The VCD file must have been created in a previous ModelSim simulation using the `vcd dumpports` command. Refer to “Using Extended VCD as Stimulus” for more information.

- `-version`
  Returns the version of the simulator as used by the licensing tools. Optional.

- `-view [<dataset_name>=]<WLF_filename>`
  Specifies a wave log format (WLF) file for `vsim` to read. Allows you to use `vsim` to view the results from an earlier simulation. The Structure, Objects, Wave, and List windows can be opened to look at the results stored in the WLF file (other ModelSim windows will not show any information when you are viewing a dataset). See additional discussion in the Examples.

- `-viewcov [<dataset_name>=]<UCDB_filename>`
  Invokes `vsim` in the coverage view mode to display UCDB data.

- `-visual <visual>`
  Specifies the visual to use for the window. Optional. Does not apply to Windows platforms. Where `<visual>` may be:

  `<class> <depth>` — One of the following:
  
  `{directcolor | grayscale | greyscale | pseudocolor | staticcolor | staticgray | staticgrey | truecolor}
  
  followed by:

  `<depth>` — Specifies how many bits per pixel are needed for the visual.

  `default` — Instructs the tool to use the default visual for the screen

  `<number>` — Specifies a visual X identifier.

  `best <depth>` — Instructs the tool to choose the best possible visual for the specified `<depth>`, where:

  `<depth>` — Specifies how many bits per pixel are needed for the visual.

- `-warning <msg_number>[,<msg_number>,…]`
  Changes the severity level of the specified message(s) to "warning." Optional. Edit the `warning` variable in the `modelsim.ini` file to set a permanent default. Refer to “Changing Message Severity Level” for more information.
• `-wlf <filename>`
  Specifies the name of the wave log format (WLF) file to create. The default is `vsim.wlf`. Optional. This option may also be specified with the `WLFFilename` variable in the `modelsim.ini` file.

• `-wlfcachesize <n>`
  Specifies the size in megabytes of the WLF reader cache. Optional. By default the cache size is set to zero. WLF reader caching caches blocks of the WLF file to reduce redundant file I/O. This should have significant benefit in slow network environments. This option may also be specified with the `WLFCacheSize` variable in the `modelsim.ini` file.

• `-wlfcollapsedelta`
  Instructs ModelSim to record values in the WLF file only at the end of each simulator delta step. Any sub-delta values are ignored. May dramatically reduce WLF file size. This option may also be specified with the `WLFCollapseMode` variable in the `modelsim.ini` file. Default.

• `-wlfcollapsetime`
  Instructs ModelSim to record values in the WLF file only at the end of each simulator time step. Any delta or sub-delta values are ignored. May dramatically reduce WLF file size. This option may also be specified with the `WLFCollapseMode` variable in the `modelsim.ini` file. Optional.

• `-wlfcompress`
  Creates compressed WLF files. Default. Use `-wlfnocompress` to turn off compression. This option may also be specified with the `WLFCompress` variable in the `modelsim.ini` file.

• `-wlfdeleteonquit`
  Deletes the current simulation WLF file (`vsim.wlf`) automatically when the simulator exits. Optional. This option may also be specified with the `WLFDeleteOnQuit` variable in the `modelsim.ini` file.

• `-wlffindex`
  (optional) Enables indexing of the WLF file. Indexing enables fast seeking to specific times. Makes viewing of wave data faster, however performance during optimization will be slower because indexing and optimization require significant memory and CPU resources. Indexing may also be specified with the `WLFIndex` variable in the `modelsim.ini` file. (default)

• `-wlfnoindex`
  Disables indexing and optimization of the WLF file. Disabling indexing makes viewing wave data slow unless the display is near the start of the WLF file. May provide a significant performance boost when archiving WLF files. Indexing and optimization information can be added back to the file using `wlfman optimize`.

• `-wlflock`
  Locks a WLF file. Optional. An invocation of ModelSim will not overwrite a WLF file that is being written by a different invocation.
• **-wlfnocollapse**
  Instructs ModelSim to preserve all events for each logged signal and their event order to the WLF file. May result in relatively larger WLF files. This option may also be specified with the **WLFCollapseMode** variable in the *modelsim.ini* file. Optional.

• **-wlfnocompress**
  Causes **vsim** to create uncompressed WLF files. Optional. WLF files are compressed by default in order to reduce file size. This may slow simulation speed by one to two percent. You may want to disable compression to speed up simulation or if you are experiencing problems with faulty data in the resulting WLF file. This option may also be specified with the **WLFCompress** variable in the *modelsim.ini* file.

• **-wlfnodeleteonquit**
  Preserves the current simulation WLF file (**vsim.wlf**) when the simulator exits. Default. This option may also be specified with the **WLFDeleteOnQuit** variable in the *modelsim.ini* file.

• **-wlfnolock**
  Disables WLF file locking. Optional. This will prevent **vsim** from checking whether a WLF file is locked prior to opening it as well as preventing **vsim** from attempting to lock a WLF once it has been opened.

• **-wlfnoopt**
  Disables optimization of waveform display in the Wave window. Optional. This option may also be specified with the **WLFOptimize** variable in the *modelsim.ini* file.

• **-wlfopt**
  Optimizes the WLF file. Enables faster display of waveforms in the Wave window when the display is zoomed out to display a larger time range. Default. Optional. This option may also be specified with the **WLFOptimize** variable in the *modelsim.ini* file.

• **-wlfsimcachesize <n>**
  Specifies the size in megabytes of the WLF reader cache for the current simulation dataset only. Optional. By default the cache size is set to zero. This makes it easier to set different sizes for the WLF reader cache used during simulation and those used during post-simulation debug. WLF reader caching caches blocks of the WLF file to reduce redundant file I/O. If neither **-wlfsimcachesize** nor **WLFSimCacheSize** *modelsim.ini* variable are specified, the **-wlfcachesize** or **WLFCacheSize** settings will be used.

• **-wlfslim <size>**
  (optional) Specifies a size restriction for the event portion of the WLF file.

    *size* — an integer, in megabytes, where the default is 0, which implies an unlimited size.

Note that a WLF file contains event, header, and symbol portions. The size restriction is placed on the event portion only. When ModelSim exits, the entire header and symbol portion of the WLF file is written. Consequently, the resulting file will be larger than the specified size.
QuestaSim uses 64-bit file I/O for maintaining the WLF file, which allows access to file systems supporting up to $2^{63}$-byte files. File size limitations are also governed by the OS file system in use as well as per-process limits on file size. You can determine any per-process limit by using the following shell commands:

- sh/bash/ksh: `ulimit -a`
- csh/tcsh: `limit`

If used in conjunction with `-wlftlim`, the more restrictive of the limits takes precedence.

This option may also be specified with the `WLFSizeLimit` variable in the `modelsim.ini` file. (See Limiting the WLF File Size.)

- `-wlftthreads` | `-wlfnthreads`

Specifies whether the logging of information to the WLF file is performed using multithreading.

This behavior is on (-wlftthreads) by default on Solaris and Linux platforms where there are more than one processor on the system. If there is only one processor available, or you are running on a Windows system, this behavior is off by default (-wlfnthreads).

When this behavior is enabled, the logging of information is performed on the secondary processor while the simulation and other tasks are performed on the primary processor.

You can turn this option off with the `-wlfnthreads` option, which you may want to do if you are performing several simulations with logging at the same time.

You can also control this behavior with the `WLFUseThreads` variable in the `modelsim.ini` file.

- `-wlftlim `<duration`

Specifies the duration of simulation time for WLF file recording. Optional. The default is infinite time (0). The `<duration>` is an integer of simulation time at the current resolution; you can optionally specify the resolution if you place curly braces around the specification. For example,

```
{5000 ns}
```

sets the duration at 5000 nanoseconds regardless of the current simulator resolution.

The time range begins at the current simulation time and moves back in simulation time for the specified duration. For example,

```
vsim -wlftlim 5000
```

writes at most the last 5000ns of the current simulation to the WLF file (the current simulation resolution in this case is ns).

If used in conjunction with `-wlfslim`, the more restrictive of the limits will take effect.

This option may also be specified with the `WLFTimeLimit` variable in the `modelsim.ini` file.
The `-wlfslim` and `-wlftlim` switches were designed to help users limit WLF file sizes for long or heavily logged simulations. When small values are used for these switches, the values may be overridden by the internal granularity limits of the WLF file format. (See Limiting the WLF File Size.)

**Arguments, VHDL**

- **-absentisempty**
  Causes VHDL files opened for read that target non-existent files to be treated as empty, rather than ModelSim issuing fatal error messages. Optional.

- **-nocollapse**
  Disables the optimization of internal port map connections. Optional.

- **-nofileshare**
  Turns off file descriptor sharing. Optional. By default ModelSim shares a file descriptor for all VHDL files opened for write or append that have identical names.

- **-noglitch**
  Disables VITAL glitch generation. Optional.
  Refer to “VHDL Simulation” for additional discussion of VITAL.

- **+no_glitch_msg**
  Disable VITAL glitch error messages. Optional.

- **-std_input <filename>**
  Specifies the file to use for the VHDL TextIO STD_INPUT file. Optional.

- **-std_output <filename>**
  Specifies the file to use for the VHDL TextIO STD_OUTPUT file. Optional.

- **-strictvital**
  Specifies to exactly match the VITAL package ordering for messages and delta cycles. Optional. Useful for eliminating delta cycle differences caused by optimizations not addressed in the VITAL LRM. Using this argument negatively impacts simulator performance.

- **-togglemaxintvalues <int>**
  Specifies the maximum number of VHDL integer values to record for toggle coverage. Optional. This limit variable may be changed on a per-signal basis. The default value of <int> is 100 values.

- **-vital2.2b**
  Selects SDF mapping for VITAL 2.2b (default is VITAL 2000). Optional.
Arguments, Verilog

- **+alt_path_delays**
  Configures path delays to operate in inertial mode by default. Optional. In inertial mode, a pending output transition is cancelled when a new output transition is scheduled. The result is that an output may have no more than one pending transition at a time, and that pulses narrower than the delay are filtered. The delay is selected based on the transition from the cancelled pending value of the net to the new pending value. The `+alt_path_delays` option modifies the inertial mode such that a delay is based on a transition from the current output value rather than the cancelled pending value of the net. This option has no effect in transport mode (see `+pulse_e/<percent>` and `+pulse_r/<percent>`).

- **+delayed_timing_checks**
  Causes timing checks to be performed on the delayed versions of input ports (used when there are negative timing check limits). Optional. ModelSim automatically detects and applies `+delayed_timing_checks` to optimized cells with negative timing checks. To turn off this feature, specify `+no_autodtc` with vsim.

- **-dpiexportobj <objfile>**
  Generates the C export wrappers and associated compiled object code for your design. The C wrapper code is written to your `<work>/_dpi/` directory, so it must have the proper permissions. The object file(s) are written to whatever location you specify with the `<objfile>` argument.

  For Windows platforms, this is a required switch when using DPI that generates a .obj file suitable for linking into a .dll. Refer to “DPI Use Flow” for additional information.

  For Linux and UNIX platforms, this switch generates both a .o and a so file. The .o file is suitable for linking into a larger .so file, which may contain import code. The .so file can be used directly, for example as an argument to the vsim -gblso switch or as a dependent library in the link command for an import shared object.

  Once you compile the export wrapper code into a shared object or .dll, you can manually load it into the simulation using -sv_lib, or perhaps -gblso. When you do manually load the export wrapper code, you should use the -nodpiexports switch so that the simulation does not automatically generate and load the `<work>/_dpi/exportwrapper.so` file, which would cause symbol collisions.

- **-hazards**
  Enables event order hazard checking in Verilog modules (Verilog only). Optional. You must also specify this argument when you compile your design with vlog. Refer to “Hazard Detection” for more details.

**Note**
Using -hazards implicitly enables the -compat argument. As a result, using this argument may affect your simulation results.
• +maxdelays
  Selects the maximum value in min:typ:max expressions. Optional. The default is the typical value. Has no effect if you specified the min:typ:max selection at compile time.

• +mindelays
  Selects the minimum value in min:typ:max expressions. Optional. The default is the typical value. Has no effect if you specified the min:typ:max selection at compile time.

• +no_audtdc
  Turns off auto-detection of optimized cells with negative timing checks and auto-application of +delayed_timing_checks to those cells. Optional.

• +no_cancelled_e_msg
  Disables negative pulse warning messages. Optional. By default vsim issues a warning and then filters negative pulses on specify path delays. You can drive an X for a negative pulse using +show_cancelled_e.

• +no_neg_tchk
  Disables negative timing check limits by setting them to zero. Optional. By default negative timing check limits are enabled. This is just the opposite of Verilog-XL, where negative timing check limits are disabled by default, and they are enabled with the +neg_tchk option.

• +no_notifier
  Disables the toggling of the notifier register argument of all timing check system tasks. Optional. By default, the notifier is toggled when there is a timing check violation, and the notifier usually causes a UDP to propagate an X. This argument suppresses X propagation on timing violations for the entire design.

• +no_path_edge
  Causes ModelSim to ignore the input edge specified in a path delay. Optional. The result of this argument is that all edges on the input are considered when selecting the output delay. Verilog-XL always ignores the input edges on path delays.

• +no_pulse_msg
  Disables the warning message for specify path pulse errors. Optional. A path pulse error occurs when a pulse propagated through a path delay falls between the pulse rejection limit and pulse error limit set with the +pulse_r and +pulse_e options. A path pulse error results in a warning message, and the pulse is propagated as an X. The +no_pulse_msg option disables the warning message, but the X is still propagated.

• -no_risefall_delaynets
  Disables the rise/fall delay net delay negative timing check algorithm. Optional. This argument is provided to return ModelSim to its pre-6.0 behavior where violation regions must overlap in order to find a delay net solution. In 6.0 versions and later, ModelSim uses separate rise/fall delays, so violation regions need not overlap for a delay solution to be found.
• **+no_show_cancelled_e**
  Filters negative pulses on specify path delays so they don’t show on the output. Default. Use **+show_cancelled_e** to drive a pulse error state.

• **+no_tchk_msg**
  Disables error messages issued by timing check system tasks when timing check violations occur. Optional. Notifier registers are still toggled and may result in the propagation of Xs for timing check violations.

• **-nodpiexports**
  Instructs the command to not generate C wrapper code for DPI export task and function routines found at elaboration time. More specifically, the command does not generate the `exportwrapper.so` shared object file in `<work>/_dpi/`. For a description on when you should use this switch, refer to the section “Integrating Export Wrappers into an Import Shared Object” in the User’s Manual.

• **-noexcludehiz**
  Instructs ModelSim to include truth table rows that contain Hi-Z states in the coverage count. Without this argument, these rows are automatically excluded. Optional.

• **+nosdferror**
  Errors issued by the SDF annotator while loading the design prevent the simulation from continuing, whereas warnings do not. Changes SDF errors to warnings so that the simulation can continue. Optional.

• **+nosdfwarn**
  Disables warnings from the SDF annotator. Optional.

• **+nospecify**
  Disables specify path delays and timing checks. Optional.

• **+nowarnBSOB**
  Disables run-time warning messages for bit-selects in initial blocks that are out of bounds.

• **+nowarn<CODE>**
  Disables warning messages in the category specified by `<CODE>`. Optional. Warnings that can be disabled include the `<CODE>` name in square brackets in the warning message. For example:

  ```
  ** Warning: (vsim-3017) test.v(2): [TFMPC] - Too few port connections. Expected <m>, found <n>.
  ```

  This warning message can be disabled with **+nowarnTFMPC**.

• **+ntc_warn**
  Enables warning messages from the negative timing constraint algorithm. Optional. By default, these warnings are disabled.
This algorithm attempts to find a set of delays for the timing check delayed net arguments such that all negative limits can be converted to non-negative limits with respect to the delayed nets. If there is no solution for this set of limits, then the algorithm sets one of the negative limits to zero and recalculates the delays. This process is repeated until a solution is found. A warning message is issued for each negative limit set to zero.

- **-onfinish ask | stop | exit**
  
  Customizes the simulator shutdown behavior when it encounters $finish in the design:
  
  - **ask**
    
    - In batch mode, the simulation exits.
    - In GUI mode, a dialog box pops up and asks for user confirmation on whether to quit the simulation.
  
  - **stop** — stops simulation and leave the simulation kernal running
  
  - **exit** — exits out of the simulation without a prompt

  By default, the simulator exits in batch mode; prompts you in GUI mode. Edit the OnFinish variable in the modelsim.ini file to set the default operation of $finish.

- **-pli "<object list>"**
  
  Loads a space-separated list of PLI shared objects. Optional. The list must be quoted if it contains more than one object. This is an alternative to specifying PLI objects in the Veriuser entry in the modelsim.ini file, refer to modelsim.ini Variables. You can use environment variables as part of the path.

- **+<plusarg>**
  
  Arguments preceded with "+" are accessible by the Verilog PLI routine mc_scan_plusargs(). Optional.

- **+pulse_e/percent**
  
  Controls how pulses are propagated through specify path delays, where <percent> is a number between 0 and 100 that specifies the error limit as a percentage of the path delay. Optional.

  A pulse greater than or equal to the error limit propagates to the output in transport mode (transport mode allows multiple pending transitions on an output). A pulse less than the error limit and greater than or equal to the rejection limit (see +pulse_r/percent) propagates to the output as an X. If the rejection limit is not specified, then it defaults to the error limit. For example, consider a path delay of 10 along with a +pulse_e/80 option. The error limit is 80% of 10 and the rejection limit defaults to 80% of 10. This results in the propagation of pulses greater than or equal to 8, while all other pulses are filtered. Note that you can force specify path delays to operate in transport mode by using the +pulse_e/0 option.
• **+pulse_e_style_onedetect**
  Selects the "on detect" style of propagating pulse errors (see **+pulse_e**). Optional. A pulse error propagates to the output as an X, and the "on detect" style is to schedule the X immediately, as soon as it has been detected that a pulse error has occurred. "on event" style is the default for propagating pulse errors (see **+pulse_e_style_onevent**).

• **+pulse_e_style_onevent**
  Selects the "on event" style of propagating pulse errors (see **+pulse_e**). Default. A pulse error propagates to the output as an X, and the "on event" style is to schedule the X to occur at the same time and for the same duration that the pulse would have occurred if it had propagated through normally.

• **+pulse_r/<percent>**
  Controls how pulses are propagated through specify path delays, where <percent> is a number between 0 and 100 that specifies the rejection limit as a percentage of the path delay. Optional.
  A pulse less than the rejection limit is suppressed from propagating to the output. If the error limit is not specified by **+pulse_e** then it defaults to the rejection limit.

• **+sdf_nocheck_celltype**
  Disables the error check a for mismatch between the CELLTYPE name in the SDF file and the module or primitive name for the CELL instance. It is an error if the names do not match. Optional.

• **+show_cancelled_e**
  Drives a pulse error state ('X') for the duration of a negative pulse on a specify path delay. Optional. By default ModelSim filters negative pulses.

• **-sv_lib <shared_obj>**
  Specifies the name of the DPI shared object with no extension. Required for use with DPI import libraries. Refer to "DPI Use Flow" for additional information.

• **-sv_liblist <filename>**
  Specifies the name of a bootstrap file containing names of DPI shared objects to load. Optional.

• **-sv_root <dirname>**
  Specifies the directory name to be used as the prefix for DPI shared object lookups. Optional.

• **+transport_path_delays**
  Selects transport mode for path delays. Optional. By default, path delays operate in inertial mode (pulses smaller than the delay are filtered). In transport mode, narrow pulses are propagated through path delays. Note that this option affects path delays only, and not primitives. Primitives always operate in inertial delay mode.
• **+typdelays**
  Selects the typical value in min:typ:max expressions. Default. Has no effect if you specified the min:typ:max selection at compile time.

• **-v2k_int_delays**
  Causes interconnect delays to be visible at the load module port per the IEEE 1364-2001 spec. Optional. By default ModelSim annotates INTERCONNECT delays in a manner compatible with Verilog-XL. If you have $sdf_annotate() calls in your design that are not getting executed, add the Verilog task $sdf_done() after your last $sdf_annotate() to remove any zero-delay MIPDs that may have been created. May be used in tandem with the `+multisource_int_delays` argument (see above).

**Arguments, object**

The object arguments may be a `<library_name>.<design_unit>`, a `.mpf` file, a `.wlf` file, or a text file. Multiple design units may be specified for Verilog modules and mixed VHDL/Verilog configurations.

• `<library_name>.<design_unit>`
  Specifies a library and associated design unit; multiple library/design unit specifications can be made. Optional. If no library is specified, the `work` library is used. You cannot use the wildcard `*` for this argument. Environment variables can be used. `<design_unit>` may be one of the following:

  <configuration> Specifies the VHDL configuration to simulate.
  <module> … Specifies the name of one or more top-level Verilog modules to be simulated. Optional.
  <entity> [(<architecture>))] Specifies the name of the top-level VHDL entity to be simulated. Optional. The entity may have an architecture optionally specified; if omitted the last architecture compiled for the specified entity is simulated. An entity is not valid if a configuration is specified.¹

¹ Most UNIX shells require arguments containing () to be single-quoted to prevent special parsing by the shell. See the examples below.

• `<MPF_file_name>`
  Opens the specified project. Optional.

• `<WLF_file_name>`
  Opens the specified dataset. Optional.

• `<text_file_name>`
  Opens the specified text file in a Source window. Optional.
Examples

- Invoke **vsim** on the entity *cpu* and assigns values to the generic parameters *edge* and *VCC*.

  ```
  vsim -gedge="low high" -gVCC=4.75 cpu
  ```

  If working within the ModelSim GUI, you would enter the command as follows:

  ```
  vsim {-gedge="low high"} -gVCC=4.75 cpu
  ```

- Instruct ModelSim to view the results of a previous simulation run stored in the WLF file *sim2.wlf*. The simulation is displayed as a dataset named *test*. Use the **-wlf** option to specify the name of the WLF file to create if you plan to create many files for later viewing.

  ```
  vsim -view test=sim2.wlf
  ```

  For example:

  ```
  vsim -wlf my_design.i01 my_asic structure
  vsim -wlf my_design.i02 my_asic structure
  ```

  Annotate instance */top/u1* using the minimum timing from the SDF file *myasic.sdf*.

  ```
  vsim -sdfmin /top/u1=myasic.sdf
  ```

  Use multiple switches to annotate multiple instances:

  ```
  vsim -sdfmin /top/u1=sdf1 -sdfmin /top/u2=sdf2 top
  ```

- This example searches the libraries *mylib* for *top(only)* and *gatelib* for *cache_set*. If the design units are not found, the search continues to the work library. Specification of the architecture (*only*) is optional.

  ```
  vsim 'mylib.top(only)' gatelib.cache_set
  ```

- Invoke **vsim** on *test_counter* and run the simulation until a break event, then quit when it encounters a $finish task.

  ```
  vsim -do "set PrefMain(forceQuit) 1; run -all" work.test_counter
  ```
The `vsim<info>` commands return information about the current vsim executable.

- `vsimAuth`
  Returns the authorization level (PE/SE, VHDL/Verilog/PLUS).

- `vsimDate`
  Returns the date the executable was built, such as "Apr 10 2000".

- `vsimId`
  Returns the identifying string, such as "ModelSim 6.1".

- `vsimVersion`
  Returns the version as used by the licensing tools, such as "1999.04".

- `vsimVersionString`
  Returns the full vsim version string.

This same information can be obtained using the `-version` argument of the `vsim` command.


**vsim_break**

Stop (interrupt) the current simulation before it runs to completion. To stop a simulation and then resume it, use this command in conjunction with `run -continue`.

**Syntax**

`vsim_break`

**Arguments**

None.

**Example**

- Interrupt a simulation, then restart it from the point of interruption.

  ```
  vsim_break
  run -continue
  ```
vsource

The `vsource` command specifies an alternative file to use for the current source file.

This command is used when the current source file has been moved. The alternative source mapping exists for the current simulation only.

**Syntax**

```
vsource [<filename>]
```

**Arguments**

- `<filename>`
  
  Specifies a relative or full pathname. Optional. If filename is omitted, the source file for the current design context is displayed.

**Examples**

```
vsource design.vhd
vsource /old/design.vhd
```
A number of `wave` commands are available to manipulate the Wave window. The following tables summarize the available options for manipulating cursors, for zooming, and for adjusting the wave display view in the Wave window:

### Table 2-7. Wave Window Commands for Cursor

<table>
<thead>
<tr>
<th>Cursor Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>wave cursor active</code></td>
<td>Sets the active cursor to the specified cursor or, if no cursor is specified, reports the active cursor</td>
</tr>
<tr>
<td><code>wave cursor add</code></td>
<td>Adds a new cursor at specified time and returns the number of the newly added cursor</td>
</tr>
<tr>
<td><code>wave cursor time</code></td>
<td>Moves or reports the time of the specified cursor or, if no cursor is specified, the time of the active cursor</td>
</tr>
<tr>
<td><code>wave cursor delete</code></td>
<td>Deletes the specified cursor or, if no cursor is specified, the active cursor</td>
</tr>
<tr>
<td><code>wave cursor see</code></td>
<td>Positions the wave display such that the specified or active cursor appears at the specified percent from the left edge of the display – 0% is the left edge, 100% is the right edge.</td>
</tr>
</tbody>
</table>

### Table 2-8. Wave Window Commands for Zooming

<table>
<thead>
<tr>
<th>Zooming Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>wave zoom in</code></td>
<td>Zoom in the wave display by the specified factor. The default factor is 2.0.</td>
</tr>
<tr>
<td><code>wave zoom out</code></td>
<td>Zoom out the wave display by the specified factor. The default factor is 2.0.</td>
</tr>
<tr>
<td><code>wave zoom full</code></td>
<td>Zoom the wave display to show the full simulation time.</td>
</tr>
<tr>
<td><code>wave zoom last</code></td>
<td>Return to last zoom range.</td>
</tr>
<tr>
<td><code>wave zoom range</code></td>
<td>Sets left and right edge of wave display to the specified start time and end time. If times are not specified, reports left and right edge times.</td>
</tr>
</tbody>
</table>

### Table 2-9. Wave Window Commands for Controlling Display

<table>
<thead>
<tr>
<th>Display view Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>wave interrupt</code></td>
<td>Immediately stops wave window drawing</td>
</tr>
<tr>
<td><code>wave refresh</code></td>
<td>Cleans wave display and redraws waves</td>
</tr>
</tbody>
</table>
Table 2-9. Wave Window Commands for Controlling Display (cont.)

<table>
<thead>
<tr>
<th>Display view Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>wave cursor see</td>
<td>Positions the wave display such that the specified or active cursor appears at the specified percent from the left edge of the display – 0% is the left edge, 100% is the right edge.</td>
</tr>
<tr>
<td>wave seetime</td>
<td>Positions the wave display such that the specified time appears at the specified percent from the left edge of the display – 0% is the left edge, 100% is the right edge.</td>
</tr>
</tbody>
</table>

Table 2-10. Wave Window Commands for Expanded Time Display

<table>
<thead>
<tr>
<th>Display view Commands</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>wave expand mode</td>
<td>Selects the expanded time display mode: Delta Time, Event Time, or off.</td>
</tr>
<tr>
<td>wave expand all</td>
<td>Expands simulation time into delta time steps if Delta Time mode is currently selected (WLFCollapseMode = 1) or into event time steps if Event Time mode is currently selected (WLFCollapseMode = 0) over the full range of the simulation from time 0 to the current time.</td>
</tr>
<tr>
<td>wave expand cursor</td>
<td>Expands simulation time into delta time steps if Delta Time mode is currently selected (WLFCollapseMode = 1) or into event time steps if Event Time mode is currently selected (WLFCollapseMode = 0) at the simulation time of the active cursor.</td>
</tr>
<tr>
<td>wave expand range</td>
<td>Expands simulation time into delta time steps if Delta Time mode is currently selected (WLFCollapseMode = 1) or into event time steps if Event Time mode is currently selected (WLFCollapseMode = 0) over a time range specified by a start time and an end time.</td>
</tr>
<tr>
<td>wave collapse all</td>
<td>Collapses simulation time over the full range of the simulation from time 0 to the current time.</td>
</tr>
<tr>
<td>wave collapse cursor</td>
<td>Collapses simulation time at the time of the active cursor.</td>
</tr>
<tr>
<td>wave collapse range</td>
<td>Collapses simulation time over a specific simulation time range.</td>
</tr>
</tbody>
</table>

Syntax

```
wave cursor active [-window <win>] [<cursor-num>]
wave cursor add [-window <win>] [-time <time>] [-name <name>] [-lock <0|1>]
wave collapse all [-window <win>]
wave collapse cursor [-window <win>] [<cursor-num>]
```
wave collapse range [-window <win>] <start-time> <end-time>
wave cursor configure [<cursor-num>] [-window <win>] [option [value]]
wave cursor time [-window <win>] [-time <time>] [<cursor-num>]
wave cursor delete [-window <win>] [<cursor-num>]
wave expand all [-window <win>]
wave expand cursor [-window <win>] [<cursor-num>]
wave expand mode [-window <win>] [off | deltas | events]
wave expand range [-window <win>] <start-time> <end-time>
wave interrupt [-window <win>]
wave refresh [-window <win>]
wave cursor see [-window <win>] [-at <percent>] [<cursor-num>]
wave seetime  [-window <win>] [-at <percent>] <time>
wave zoom in [-window <win>] [<factor>]
wave zoom out [-window <win>] [<factor>]
wave zoom full [-window <win>]
wave zoom last [-window <win>]
wave zoom range [-window <win>] [<start-time>] [<end-time>]

Arguments

- [-at <percent>]
  Positions the display such that the time or cursor is the specified <percent> from the left edge of the wave display. 0% is the left edge; 100% is the right edge. Optional. Default is 50%.

- [<cursor-num>]
  Specifies a cursor number. Optional. If not specified, the active cursor is used.

- [<factor>]
  A number that specifies how much you want to zoom into or out of the wave display. Optional. Default value is 2.0.

- [-lock <0|1>]
  Specify the lock state of the cursor. Optional. Default is '0', unlocked.

- [-name <name>]
  Specify the name of the cursor. Optional. Default is "Cursor <n>" where <n> is the cursor number.
• off | deltas | events
  Specifies the expanded time display mode for the Wave window. Optional. Default is off.

• <option> [<value>]
  Specify a value for the designated option. Currently supported options are -name, -time, and -lock. Optional. If no option is specified, current value of all options are reported.

• [<start-time>] [<end-time>]
  start-time and end-time are times that specify an expand, collapse, or zoom range. If neither number is specified, the command returns the current range. If only one time is specified, then the range is set to start at 0 and end at specified time.

• [-time <time>]
  Specifies a cursor time. Optional.

• [-window <win>]
  All commands default to the active Wave window unless this argument is used to specify a different Wave window. Optional.

**Examples**

• Either of these commands creates a zoom range with a start time of 20 ns and an end time of 100 ns.
  
  ```
  wave zoom range 20ns 100ns
  wave zoom range 20 100
  ```

• Return the name of cursor 2:
  
  ```
  wave cursor configure 2 -name
  ```

• Name cursor 2, "reference cursor" and return that name with:
  
  ```
  wave cursor configure 2 -name {reference cursor}
  ```

• Return the values of all wave cursor configure options for cursor 2:
  
  ```
  wave cursor configure 2
  ```
When

The **when** command instructs ModelSim to perform actions when the specified conditions are met.

For example, you can use the **when** command to break on a signal value or at a specific simulator time. Use the **nowhen** command to deactivate **when** commands.

**Syntax**

```
when [[-fast] [-id <id#>] [-label <label>] {<when_condition_expression>} {<command>} ]
```

**Description**

The **when** command uses a **when_condition_expression** to determine whether or not to perform the action. Conditions can include VHDL signals and Verilog nets and registers. The **when_condition_expression** uses a simple restricted language (that is not related to Tcl), which permits only four operators and operands that may be either HDL object names, `signame'event`, or constants. ModelSim evaluates the condition every time any object in the condition changes, hence the restrictions.

Here are some additional points to keep in mind about the **when** command:

- The **when** command creates the equivalent of a VHDL process or a Verilog always block. It does not work like a looping construct you might find in other languages such as C.
- Virtual signals, functions, regions, types, etc. cannot be used in the **when** command. Neither can simulator state variables other than $now.
- With no arguments, **when** will list the currently active when statements and their labels (explicit or implicit).

**Syntax**

```
when [[-fast] [-id <id#>] [-label <label>] {<when_condition_expression>} {<command>} ]
```

**Embedded Commands Allowed with the -fast Argument**

You can use any Tcl command as a `<command>`, along with any of the following **vsim** commands:

- bp, bd
- change
- disablebp, enablebp
- echo
- examine
- force, noforce
• log, nolog
• stop
• when, nowhen

**Embedded Commands Not Allowed with the -fast Argument**

- Any do commands
- Any Tk commands or widgets
- References to U/I state variables or tcl variables
- Virtual signals, functions, or types

**Using Global Tcl Variables with the -fast Argument**

Embedded commands that use global Tcl variables for passing a state between the when command and the user interface need to declare the state using the Tcl uivar command. For example, the variable `i` below is visible in the GUI. From the command prompt, you can display it (by entering `echo $i`) or modify it (for example, by entering `set i 25`).

```tcl
set i 10
when -fast {clk == '0'} {
    uivar i
    set i [expr {$i - 1}]
    if {$i <= 0} {
        force reset 1 0, 0 250
    }
}
when -fast {reset == '0'} {
    uivar i
    set i 10
}
```

**Additional Restrictions on the -fast Argument**

Accessing channels (such as files, pipes, sockets) that were opened outside of the embedded command will not work. For example:

```tcl
set fp [open mylog.txt w]
when -fast {bus} {
    puts $fp "bus change: [examine bus]"
}
```

The channel that `$fp` refers to is not available in the simulator, only in the user interface. Even using the uivar command does not work here because the value of `$fp` has no meaning in the context of the -fast argument.

The following method of rewriting this example opens the channel, writes to it, then closes it within the `when` command:
when -fast {bus} {
    set fp [open mylog.txt a]
    puts $fp "bus change: [examine bus]"
    close $fp
}

The following example is a little more sophisticated method of doing the same thing:

when -fast {$now == 0ns} {
    set fp [open mylog.txt w]
}
when -fast {bus} {
    puts $fp "bus change: [examine bus]"
}
when -fast {$now == 1000ns} {
    close $fp
}

The general principle is that any embedded command done using the -fast argument is global to all other commands used with the -fast argument. Here, {$now == 0ns} is a way to define Tcl processes that the -fast commands can use. These processes have the same restrictions that when bodies have, but the advantage is again speed as a proc will tend to execute faster than code in the when body itself.

It is recommended not to use virtual signals and expressions.

**Arguments**

- **-fast**
  
  Causes the embedded <command> to execute within the simulation kernel, which provides faster execution and reduces impact on simulation runtime performance. Optional.
  Limitations on using the -fast argument are described above (in “Embedded Commands Not Allowed with the -fast Argument”). Disallowed commands still work, but they slow down the simulation.

- **-label <label>**
  
  Used to identify individual when commands. Optional.

- **-id <id#>**
  
  Attempts to assign this id number to the when command. Optional. If the id number you specify is already used, ModelSim will return an error.

**Note**

Id numbers for when commands are assigned from the same pool as those used for the bp command. So even if you have not specified a given id number for a when command, that number may still be used for a breakpoint.

- **{<when_condition_expression>}**

  Specifies the conditions to be met for the specified <command> to be executed. Required if a command is specified. The condition is evaluated in the simulator kernel and can be an
object name, in which case the curly braces can be omitted. The command will be executed when the object changes value. The condition can be an expression with these operators:

<table>
<thead>
<tr>
<th>Name</th>
<th>Operator</th>
</tr>
</thead>
<tbody>
<tr>
<td>equals</td>
<td>==, =</td>
</tr>
<tr>
<td>not equal</td>
<td>!=, /=</td>
</tr>
<tr>
<td>greater than</td>
<td>&gt;</td>
</tr>
<tr>
<td>less than</td>
<td>&lt;</td>
</tr>
<tr>
<td>greater than or equal</td>
<td>&gt;=</td>
</tr>
<tr>
<td>less than or equal</td>
<td>&lt;=</td>
</tr>
<tr>
<td>AND</td>
<td>&amp;&amp;, AND</td>
</tr>
<tr>
<td>OR</td>
<td></td>
</tr>
</tbody>
</table>

The operands may be object names, signame'event, or constants. Subexpressions in parentheses are permitted. The command will be executed when the expression is evaluated as TRUE or 1.

The formal BNF syntax is:

```
condition ::= Name | { expression }
expression ::= expression AND relation
              | expression OR relation
relation ::= Name = Literal
           | Name /= Literal
           | Name ' EVENT
           | ( expression )
Literal ::= '<char>' | "<bitstring>" | <bitstring>
```

The "=" operator can occur only between a Name and a Literal. This means that you cannot compare the value of two signals, i.e., Name = Name is not possible.

Tcl variables can be used in the condition expression but you must replace the curly braces ({}) with double quotes (""). This works like a macro substitution where the Tcl variables are evaluated once and the result is then evaluated as the when condition. Condition expressions are evaluated in the vsim kernel, which knows nothing about Tcl variables. That's why the condition expression must be evaluated in the GUI before it is sent to the vsim kernel. See below for an example of using a Tcl variable.

The ">", "<", ">=", and "<=" operators are the standard ones for vector types, not the overloaded operators in the std_logic_1164 package. This may cause unexpected results when comparing objects that contain values other than 1 and 0. ModelSim does a lexical comparison (position number) for values other than 1 and 0. For example:
when

0000 < 1111 ## This evaluates to true
H000 < 1111 ## This evaluates to false
001X >= 0010 ## This also evaluates to false

• {<command>}

The command(s) for this argument are evaluated by the Tcl interpreter within the ModelSim GUI. Any ModelSim or Tcl command or series of commands are valid with one exception—the run command cannot be used with the when command. Required if a when expression is specified. The command sequence usually contains a stop command that sets a flag to break the simulation run after the command sequence is completed. Multiple-line commands can be used.

Note

If you want to stop the simulation using a when command, you must use a stop command within your when statement. DO NOT use an exit command or a quit command. The stop command acts like a breakpoint at the time it is evaluated.

Examples

• The when command below instructs the simulator to display the value of object c in binary format when there is a clock event, the clock is 1, and the value of b is 01100111. Finally, the command tells ModelSim to stop.

```tcl
when -label when1 {clk’event and clk='1' and b = "01100111"} {
    echo "Signal c is [exa -bin c]"
    stop
}
```

• The commands below show an example of using a Tcl variable within a when command. Note that the curly braces ({{}}) have been replaced with double quotes (""").

```tcl
set clkb_path /tb/ps/dprb_0/udprb/ucar_reg/uint_ram/clkb;
when -label when1 "$clkb_path'event and $clkb_path ='1'" {
    echo "Detected Clk edge at path $clkb_path"
}
```

• The when command below is labeled a and will cause ModelSim to echo the message “b changed” whenever the value of the object b changes.

```tcl
when -label a b {echo "b changed"}
```

• The multi-line when command below does not use a label and has two conditions. When the conditions are met, ModelSim runs an echo command and a stop command.

```tcl
when {b = 1
    and c /= 0 } {
    echo "b is 1 and c is not 0"
    stop
}
```

• In the example below, for the declaration "wire [15:0] a;", the when command will activate when the selected bits match a 7:
when {a(3:1) = 3'7} {echo "matched at time " $now}

- In the example below, we want to sample the values of the address and data bus on the first falling edge of *clk* after *sstrb* has gone high.

```python
# ::strobe is our state variable
set ::strobe Zero
# This signal breakpoint only fires when sstrb changes to a '1'
when -label checkStrobe (/top/sstrb == '1') {
    # Our state Zero condition has been met, move to state One
    set ::strobe One
}
# This signal breakpoint fires each time clk goes to '0'
when (/top/clk == '0') {
    if {$::strobe eq "One"} {
        # Our state One condition has been met
        # Sample the busses
        echo Sample paddr=[examine -hex /top/paddr] :: sdata=[examine -hex /top/sdata]
        # reset our state variable until next rising edge of sstrb
        (back to
            state Zero)
        set ::strobe Zero
    }
}
```

**Ending the simulation with the stop command**

Batch mode simulations are often structured as "run until condition X is true," rather than "run for X time" simulations. The multi-line **when** command (shown below) sets a done condition, and ModelSim runs an **echo** command and a **stop** command when the condition is reached.

The simulation will not stop (even if a **quit -f** command is used) unless you enter a **stop** command. To exit the simulation and quit ModelSim, use an approach like the following:

```python
onbreak {resume}
when {/(done_condition == '1') {
    echo "End condition reached"
    if [batch_mode] {
        set DoneConditionReached 1
        stop
    }
}
run 1000 us
if {$DoneConditionReached == 1} {
    quit -f
}
```

This example stops 100ns after a signal transition:
when {a = 1} {
    # If the 100ns delay is already set then let it go.
    if {([when -label a_100] == "")} {
        when -label a_100 { $now = 100 } {
            # delete this breakpoint then stop
            nowhen a_100
            stop
        }
    }
}

**Time-based breakpoints**

You can build time-based breakpoints into a `when` statement with the following syntax.

For absolute time (indicated by `@`) use:

```tcl
when {$now = @1750 ns} {stop}
```

You can also use:

```tcl
when {errorFlag = '1' OR $now = 2 ms} {stop}
```

This example adds 2 ms to the simulation time at which the `when` statement is first evaluated, then stops. The white space between the value and time unit is required for the time unit to be understood by the simulator.

You can also use variables, as shown in the following example:

```tcl
set time 1000
when "$now = $time" {stop}
```

The quotes instruct Tcl to expand the variables before calling the command. So, the `when` command sees:

```tcl
when "$now = 1000" stop
```

Note that "$now" has the '$' escaped. This prevents Tcl from expanding the variable, because if it did, you would get:

```tcl
when "0 = 1000" stop
```

**See also**

`bp`, `disablebp`, `enablebp`, `nowhen`
where

The **where** command displays information about the system environment. This command is useful for debugging problems where ModelSim cannot find the required libraries or support files.

The command displays two results on consecutive lines:

- **current directory**
  
  This is the current directory that ModelSim was invoked from, or that was specified on the ModelSim command line.

- **current project file**
  
  This is the `.mpf` file ModelSim is using. All library mappings are taken from here when a project is open. If the design is not loaded through a project, this line displays the `modelsim.ini` file in the current directory.

**Syntax**

`where`

**Arguments**

- None.

**Examples**

- Design is loaded through a project:

  ```
  VSIM> where
  #  Current directory is: D:\Client
  #  Project is: D:/Client/monproj.mpf
  ```

- Design is loaded with no project (indicates the `modelsim.ini` file is under the `mydesign` directory):

  ```
  VSIM> where
  #  Current directory is: C:\Client\testcase\mydesign
  #  Project is: modelsim.ini
  ```
wlf2log

The **wlf2log** command translates a ModelSim WLF file (`vsim.wlf`) to a QuickSim II logfile. The command reads the `vsim.wlf` WLF file generated by the `add list`, `add wave`, or `log` commands in the simulator and converts it to the QuickSim II logfile format.

### Syntax

```
```

### Arguments

- **-bits**
  - Forces vector nets to be split into 1-bit wide nets in the log file. Optional.
- **-fullname**
  - Shows the full hierarchical pathname when displaying signal names. Optional.
- **-help**
  - Displays a list of command options with a brief description for each. Optional.
- **-inout**
  - Lists only the inout ports. Optional. This may be combined with the `-input`, `-output`, or `-internal` switches.
- **-input**
  - Lists only the input ports. Optional. This may be combined with the `-output`, `-inout`, or `-internal` switches.
- **-internal**
  - Lists only the internal signals. Optional. This may be combined with the `-input`, `-output`, or `-inout` switches.
- **-l <instance_path>**
  - Lists the signals at or below the specified HDL instance path within the design hierarchy. Optional.
- **-lower**
  - Shows all logged signals in the hierarchy. Optional. When invoked without the `-lower` switch, only the top-level signals are displayed.

### Note

This command should be invoked only after you have stopped the simulation using `quit -sim` or `dataset close sim`.

---

**Commands**

**wlf2log**
-o <outfile>
Directs the output to be written to the file specified by <outfile>. Optional. The default destination for the logfile is standard out.

-output
Lists only the output ports. Optional. This may be combined with the -input, -inout, or -internal switches.

-quiet
Disables error message reporting. Optional.

<wlffile>
Specifies the ModelSim WLF file that you are converting. Required.
**wlf2vcd**

The *wlf2vcd* command translates a ModelSim WLF file to a standard VCD file. Complex data types that are unsupported in the VCD standard (records, memories, etc.) are not converted.

**Note**

This command should be invoked only after you have stopped the simulation using `quit -sim` or `dataset close sim`.

**Syntax**

```
wlf2vcd [-help] [-o <outfile>] [-quiet] <wlffile>
```

**Arguments**

- `-help`
  
  Displays a list of command options with a brief description for each. Optional.
- `-o <outfile>`
  
  Specifies a filename for the output. By default, the VCD output goes to stdout. Optional.
- `-quiet`
  
  Disables warning messages that are produced when an unsupported type (e.g., records) is encountered in the WLF file. Optional.
- `<wlffile>`
  
  Specifies the ModelSim WLF file that you are converting. Required.
**wlfman**

This command allows you to get information about and manipulate saved WLF files.

The command performs four functions depending on which mode you use:

- **wlfman info** returns file information, resolution, versions, and so forth about the source WLF file.

- **wlfman items** generates a list of HDL objects (i.e., signals) from the source WLF file and outputs it to stdout. When redirected to a file, the output is called an object_list_file, and it can be read in by **wlfman filter**. The object_list_file is a list of objects, one per line. Comments start with a '#' and continue to the end of the line. Wildcards are legal in the leaf portion of the name. Here is an example:

```
/top/foo       # signal foo
/top/u1/*      # all signals under u1
/top/u1        # same as line above
-r /top/u2     # recursively, all signals under u2
```

Note that you can produce these files from scratch but be careful with syntax. **wlfman items** always creates a legal object_list_file.

- **wlfman filter** reads in a WLF file and, optionally, an object_list_file, and writes a new WLF file containing filtered information from those sources. You determine the filtered information with the arguments you specify.

- **wlfman profile** generates a report of the estimated percentage of file space that each signal is taking in the specified WLF file. This command can identify signals that account for a large percentage of the WLF file size (e.g., a logged memory that uses a zero-delay integer loop to initialize the memory). You may be able to drastically reduce WLF file size by not logging those signals.

- **wlfman merge** combines two WLF files with different signals into one WLF file. It does not combine wlf files containing the same signals at different runtime ranges (i.e., mixedhdl_0ns_100ns.wlf & mixedhdl_100ns_200ns.wlf).

- **wlfman optimize** copies the data from the WLF file to the output WLF file, adding or replacing the indexing and optimization information.

The different modes are intended to be used together. For example, you might run **wlfman profile** and identify a signal that accounts for 50% of the WLF file size. If you don’t actually need that signal, you can then run **wlfman filter** to remove it from the WLF file.

**Syntax**

```
wlfman info <source_wlffile> [-v]
wlfman items <source_wlffile> [-n] [-v]
```
Commands

**wlfman**

`wlfman profile <source_wlffile> [-rank] [-top <number>]`

`wlfman merge -o <out_wlffile> [ <wlffile1> <wlffile2> ... ] [-compress | -nocompress] [-index | -noindex] [-opt | -noopt]`

`wlfman optimize -o <out_wlffile> <source_wlffile> [-opt | -noopt]`

**Arguments**

- **-o <out_wlffile>**
  (required) Specifies the name of the output WLF file. The output WLF file will contain all objects specified by the preceding arguments. Output WLF files are always written in the latest WLF version regardless of the source WLF file version.

- **<source_wlffile>**
  (required) Specifies the WLF file from which you want information.

- **<wlffile1> <wlffile2> ...**
  (required) Specifies the WLF files whose objects you want to copy into one WLF file. Specified as a space separated list.

- **-begin <time>**
  (optional) Specifies the simulation time at which to start reading information from the source WLF file where the default is to include the entire length of time recorded in `<source_wlffile>`.

- **-compress | -nocompress**
  (optional) Controls compression of the output WLF file.
    - `compress` — Enables compression. (default)
    - `nocompress` — Disables compression.

- **-end <time>**
  (optional) Specifies the simulation time at which you want to end reading information from `<source_wlffile>`.

- **-f <object_list_file>**
  (optional) Specifies an object_list_file created by `wlfman items` to include in `<outwolffile>`.

- **-index | -noindex**
  (optional) Controls indexing when writing the output WLF file. Indexing makes viewing wave data faster, however performance during optimization will be slower because indexing and optimization require significant memory and CPU resources. Disabling indexing makes viewing wave data slower unless the display is near the start of the WLF file. Disabling indexing also disables optimization of the WLF file but may provide a significant performance boost when archiving WLF files. Indexing and optimization information can be added back to the file using the `wlfman optimize` command.
-index — Enables indexing. (default)
-noindex — Disables indexing and optimization.

- n
  (optional) Lists regions only (no signals).

- opt | -noopt
  (optional) Controls optimization of the output WLF file.
    - opt — Enables WLF file optimization. (default)
    - noopt — Disables WLF file optimization.

- r <object>
  (optional) Specifies an object (region) to recursively include in the output. If <object> is a signal, the output would be the same as using -s.

- rank
  (optional) Sorts the wlfman profile report by percentage of the total file space used by each signal.

- s <symbol>
  (optional) Specifies an object to include in the output. By default all objects are included.

- t <resolution>
  (optional) Specifies the time resolution of the new WLF file. By default the resolution is the same as the source WLF file.

- top <number>
  (optional) Filters the wlfman profile report so that only the top <number> signals in terms of file space percentage are displayed.

- v
  (optional) Produces verbose output that lists the object type next to each object.

Examples

- The output from this command would look something like this:
  
  wlfman profile -rank top_vh.wlf

  Returns:
#Repeated ID #'s mean those signals share the same
#space in the wlf file.

<table>
<thead>
<tr>
<th>ID</th>
<th>Transitions</th>
<th>File %</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2192</td>
<td>33 %</td>
<td>/top_vh/pdata</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/processor/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/pdata</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__0/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__1/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__2/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__3/s/data</td>
</tr>
<tr>
<td>2</td>
<td>1224</td>
<td>18 %</td>
<td>/top_vh/ptrans</td>
</tr>
<tr>
<td>3</td>
<td>1216</td>
<td>18 %</td>
<td>/top_vh/sdata</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>/top_vh/cache/sdata</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>/top_vh/memory/data</td>
</tr>
<tr>
<td>4</td>
<td>675</td>
<td>10 %</td>
<td>/top_vh/strans</td>
</tr>
<tr>
<td>5</td>
<td>423</td>
<td>6 %</td>
<td>/top_vh/cache/gen__3/s/data_out</td>
</tr>
<tr>
<td>6</td>
<td>135</td>
<td>3 %</td>
<td>/top_vh/paddr</td>
</tr>
</tbody>
</table>

• wlfman profile -top 3 top_vh.wlf

The output from this command would look something like this:

<table>
<thead>
<tr>
<th># ID</th>
<th>Transitions</th>
<th>File %</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2192</td>
<td>33 %</td>
<td>/top_vh/pdata</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/processor/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/pdata</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__0/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__1/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__2/s/data</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>/top_vh/cache/gen__3/s/data</td>
</tr>
<tr>
<td>2</td>
<td>1224</td>
<td>18 %</td>
<td>/top_vh/ptrans</td>
</tr>
<tr>
<td>3</td>
<td>1216</td>
<td>18 %</td>
<td>/top_vh/sdata</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>/top_vh/cache/sdata</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>/top_vh/memory/data</td>
</tr>
</tbody>
</table>

Related Topics

• Recording Simulation Results With Datasets
• WLF File Parameter Overview
wlfrecover

The `wlfrecover` tool attempts to "repair" WLF files that are incomplete due to a crash or the file being copied prior to completion of the simulation. You can run the tool from the VSIM> or ModelSim> prompt or from a shell.

Syntax

```
  wlfrecover <filename> [-force] [-q]
```

Arguments

- `<filename>`
  Specifies the WLF file to repair. Required.
- `-force`
  Disregards file locking and attempts to repair the file. Optional.
- `-q`
  Hides all messages unless there is an error while repairing the file. Optional.
The `write format` command records the names and display options of the HDL objects currently being displayed in the Analysis, List, Memory, Message Viewer, Test Browser, and Wave windows.

The `write format restart` command creates a single `.do` file that will recreate all debug windows, all file/line breakpoints, and all signal breakpoints created using the `when` command. If the `ShutdownFile modelsim.ini` variable is set to this `.do` filename, it will call the write format restart command upon exit.

The file created is primarily a list of `add list` or `add wave` commands, though a few other commands are included (see "Output" below). This file may be invoked with the `do` command to recreate the window format on a subsequent simulation run.

When you load a format file, ModelSim verifies the existence of the datasets required by that file. ModelSim displays an error message if the requisite datasets do not all exist. To force the execution of the format file even if all datasets are not present, use the `-force` switch with your `do` command. For example:

```
VSIM> do format.do -force
```

Note that this will result in error messages for signals referencing nonexistent datasets. Also, `-force` is recognized by the format file not the `do` command.

**Syntax**

```
write format analysis | list | memory | msgviewer | testbrowser | wave | restart <filename>
```

**Arguments**

- `analysis | list | memory | msgviewer | testbrowser | wave | restart`
  Specifies that the contents of the designated window are recorded in a `.do` file, `<filename>`. If restart is designated, all windows and breakpoints are recorded in the `.do` file. Required.

- `<filename>`
  Specifies the name of the output file where the data is to be written. Required.

**Examples**

- Save the current data in the List window in a file named `alu_list.do`.
  
  ```
  write format list alu_list.do
  ```

- Save the current data in the Wave window in a file named `alu_wave.do`.
  
  ```
  write format wave alu_wave.do
  ```

**Output**

- Below is an example of a saved Wave window format file.
onerror {resume}
quietly WaveActivateNextPane {} 0
add wave -noupdate -format Logic /cntr_struct/ld
add wave -noupdate -format Logic /cntr_struct/rst
add wave -noupdate -format Logic /cntr_struct/clk
add wave -noupdate -format Literal /cntr_struct/d
add wave -noupdate -format Literal /cntr_struct/q
TreeUpdate [SetDefaultTree]
quietly WaveActivateNextPane
add wave -noupdate -format Logic /cntr_struct/p1
add wave -noupdate -format Logic /cntr_struct/p2
add wave -noupdate -format Logic /cntr_struct/p3
TreeUpdate [SetDefaultTree]
WaveRestoreCursors (0 ns)
WaveRestoreZoom (0 ns) {1 us}
configure wave -namecolwidth 150
configure wave -valuecolwidth 100
configure wave -signalnamewidth 0
configure wave -justifyvalue left

In the example above, five signals are added with the -noupdate argument to the default window. The TreeUpdate command then refreshes all five waveforms. The second WaveActivateNextPane command creates a second pane which contains three signals. The WaveRestoreCursors command restores any cursors you set during the original simulation, and the WaveRestoreZoom command restores the Zoom range you set. These four commands are used only in saved Wave format files; therefore, they are not documented elsewhere.

See also
  add list, add wave
write list

The **write list** command records the contents of the List window in a list output file. This file contains simulation data for all HDL objects displayed in the List window: VHDL signals and variables and Verilog nets and registers.

**Syntax**

```
write list [-events] <filename>
```

**Arguments**

- `-events`
  
  Specifies to write print-on-change format. Optional. Default is tabular format.

- `<filename>`
  
  Specifies the name of the output file where the data is to be written. Required.

**Examples**

- Save the current data in the List window in a file named `alu.lst`.
  
  ```
  write list alu.lst
  ```

**See also**

- `write tssi`
write preferences

The **write preferences** command saves the current GUI preference settings to a Tcl preference file. Settings saved include Wave, Objects, and Locals window column widths; Wave, Objects, and Locals window value justification; and Wave window signal name width.

**Syntax**

```
write preferences <preference file name>
```

**Arguments**

- `<preference file name>`
  Specifies the name for the preference file. Optional. If the file is named `modelsim.tcl`, ModelSim will read the file each time `vsim` is invoked. To use a preference file other than `modelsim.tcl` you must specify the alternative file name with the `MODELSIM_TCL` environment variable.

**See also**

You can modify variables by editing the preference file with the ModelSim `notepad`:

```
notepad <preference file name>
```
write report

The `write report` command prints a summary of the design being simulated including a list of all design units (VHDL configurations, entities, and packages, and Verilog modules) with the names of their source files. The summary includes a list of all source files used to compile the given design.

The Simulation Report contains the following information:

- Design Simulated — directory path of the design’s top-level module
- Number of signals/nets in the design
- Number of processes in the design
- Simulator Parameters, including:
  - Current directory
  - Project file directory
  - Simulation time resolution
- List of design units used, including:
  - Module name
  - Architecture, if applicable
  - Library directory
  - Source file
  - Timescale
  - Occurrences

**Syntax**

```
write report [ -capacity [ -l | -s ] [ -assertions | -classes | -cvg | -qdas | -solver ] ] |
[ -l | -s ] [ -tcl ] <filename>
```

**Arguments**

- `<filename>`
  Specifies the name of the output file where the data is to be written. Optional. If the `<filename>` is omitted, the report is written to the Transcript window.
- `-capacity`
  Reports data on memory usage of various types of SystemVerilog constructs in the design. Optional. ModelSim collects memory usage data for assertions, classes, covergroups, dynamic objects, and the solver. Each of these design object types has a switch that you can specify along with -capacity in order to display its memory data. To display memory data for all object types, specify -capacity -l.
-assertions
Reports memory usage data for SystemVerilog assertions and cover directives.

-classes
Reports memory usage data for the current number of objects allocated, the current memory allocated for class object, the peak memory allocated and peak time.

-cvg
Reports memory usage data for the number of covergroups, cross, bins and memory allocated.

-qdas
Reports memory usage data for queues, dynamic arrays, and associative arrays.

-solver
Reports memory usage data for calls to randomize() and memory usage.

-l
Generates more detailed information about the design, including a list of sparse memories or the memory capacity for all object types. Default.

-s
Generates a short list of design information. Optional.

-tcl
Generates a Tcl list of design unit information. Optional. This argument cannot be used with a filename.

Examples

- Save information about the current design in a file named *alu_rpt.txt*.
  
  ```
  write report alu_rpt.txt
  ```

- Display a short list of information regarding the memory capacity for covergroups in the design during the simulation so far.
  
  ```
  write report -capacity -s cvg
  ```

- Display information on all of the calls to randomize() made during simulation so far, along with the memory usage of those calls, number of calls, and callsite information.
  
  ```
  write report -capacity -solver
  ```

Example Output

```
## SIMULATION REPORT Generated on Mon Aug 10 12:56:15 2009
##
## Design simulated: <directory>\dataflow\work.top(fast)
```
Commands

write report

## Number of signals/nets in design: 89
## Number of processes in design: 74
##
## Simulator Parameters:
##
## Current directory: <directory>\dataflow
## Project file: <directory>\win32/../modelsim.ini
## Simulation time resolution: 1ns
##
## List of Design units used:
##
## Module: top
## Architecture: fast
## Library: <directory>\dataflow\work
## Source File: top.v
## Timescale: 1ns / 1ns
## Occurrences: 1
##
## Module: proc
## Architecture: fast
## Library: <directory>\dataflow\work
## Source File: proc.v
## Timescale: 1ns / 1ns
## Occurrences: 1

...
write timing

The write timing command displays path delays and timing check limits, unadjusted for delay net delays, for the specified instance.

Syntax

write timing [-recursive] [-file <filename>] [<instance_name1>…<instance_nameN>] [-simvalues]

Arguments

- -recursive
  Generates timing information for the specified instance and all instances underneath it in the design hierarchy. Optional.
- -file <filename>
  Specifies the name of the output file where the data is to be written. Optional. If the -file argument is omitted, timing information is written to the Transcript window.
- <instance_name1>…<instance_nameN>
  The name(s) of the instance(s) for which timing information will be written. Required.
- -simvalues
  Displays optimization-adjusted values for delay net delays. Optional.

Examples

- Write timing about /top/u1 and all instances underneath it in the hierarchy to the file timing.txt.
  
  write timing -r -f timing.txt /top/u1

- Write timing information about the designated instances to the Transcript window.
  
  write timing /top/u1 /top/u2 /top/u3 /top/u8
write transcript

The **write transcript** command writes the contents of the Transcript window to the specified file. The resulting file can be used to replay the transcribed commands as a DO file (macro).

The command cannot be used in batch mode. In batch mode use the standard Transcript file or redirect stdout.

**Syntax**

```
write transcript [<filename>]
```

**Arguments**

- `<filename>`
  
  Specifies the name of the output file where the data is to be written. Optional. If the `<filename>` is omitted, the transcript is written to a file named `transcript`.

**See also**

- `do`
write tssi

The **write tssi** command records the contents of the List window in a "TSSI format" file.

The file contains simulation data for all HDL objects displayed in the List window that can be converted to TSSI format (VHDL signals and Verilog nets). A signal definition file is also generated.

The List window needs to be using symbolic radix in order for **write tssi** to produce useful output.

**Syntax**

```
write tssi <filename>
```

**Arguments**

- `<filename>`
  
  Specifies the name of the output file where the data is to be written. Required.

**Description**

If the `<filename>` has a file extension (e.g., `listfile.lst`), then the definition file is given the same file name with the extension .def (e.g., `listfile.def`). The values in the listfile are produced in the same order that they appear in the List window. The directionality is determined from the port type if the object is a port, otherwise it is assumed to be bidirectional (mode INOUT).

Objects that can be converted to SEF are VHDL enumerations with 255 or fewer elements and Verilog nets. The enumeration values U, X, 0, 1, Z, W, L, H and - (the enumeration values defined in the IEEE Standard 1164 **std_ulogic** enumeration) are converted to SEF values according to the table below. Other values are converted to a question mark (?) and cause an error message. Though the **write tssi** command was developed for use with **std_ulogic**, any signal which uses only the values defined for **std_ulogic** (including the VHDL standard type **bit**) will be converted.

<table>
<thead>
<tr>
<th><strong>std_ulogic State Characters</strong></th>
<th><strong>SEF State Characters</strong></th>
<th><strong>Bidirectional</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>N</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>N</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>D</td>
<td>L</td>
</tr>
<tr>
<td>1</td>
<td>U</td>
<td>H</td>
</tr>
<tr>
<td>Z</td>
<td>Z</td>
<td>T</td>
</tr>
<tr>
<td>W</td>
<td>N</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>D</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>U</td>
<td>H</td>
</tr>
</tbody>
</table>
Bidirectional logic values are not converted because only the resolved value is available. The TSSI TDS ASCII In Converter and ASCII Out Converter can be used to resolve the directionality of the signal and to determine the proper forcing or expected value on the port. Lowercase values x, z, w, l, and h are converted to the same values as the corresponding capitalized values. Any other values will cause an error message to be generated the first time an invalid value is detected on a signal, and the value will be converted to a question mark (?)

Note
The TDS ASCII In Converter and ASCII Out Converter are part of the TDS software. ModelSim outputs a vector file, and TSSI tools determine whether the bidirectional signals are driving or not.

See also

<table>
<thead>
<tr>
<th>std_ultimate State Characters</th>
<th>SEF State Characters</th>
<th>Bidirectional</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td>-</td>
<td>N</td>
<td>X</td>
</tr>
</tbody>
</table>

tssi2mti
**write wave**

The **write wave** command records the contents of the Wave window in PostScript format. The output file can then be printed on a PostScript printer.

**Syntax**

```
write wave[-width <real_num>] [-height <real_num>]
[-margin <real_num>] [-start <time>] [-end <time>] [-perpage <time>] [-landscape]
[-portrait] <filename>
```

**Arguments**

- `-width <real_num>`
  Specifies the paper width in inches. Optional. Default is 8.5.
- `-height <real_num>`
  Specifies the paper height in inches. Optional. Default is 11.0.
- `-margin <real_num>`
  Specifies the margin in inches. Optional. Default is 0.5.
- `-start <time>`
  Specifies the start time (on the waveform timescale) to be written. Optional.
- `-end <time>`
  Specifies the end time (on the waveform timescale) to be written. Optional.
- `-perpage <time>`
  Specifies the time width per page of output. Optional.
- `-landscape`
  Use landscape (horizontal) orientation. Optional. This is the default orientation.
- `-portrait`
  Use portrait (vertical) orientation. Optional. The default is landscape (horizontal).
- `<filename>`
  Specifies the name of the PostScript output file. Required.

**Examples**

- Save the current data in the Wave window in a file named *alu.ps*.
  ```
  write wave alu.ps
  ```
- Write two separate pages to *top.ps*. The first page contains data from 600ns to 700ns, and the second page contains data from 701ns to 800ns.
  ```
  write wave -start 600ns -end 800ns -perpage 100ns top.ps
  ```
Commands

*write wave*

To make the job of creating a PostScript waveform output file easier, use the *File > Print Postscript* menu selection in the Wave window.
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