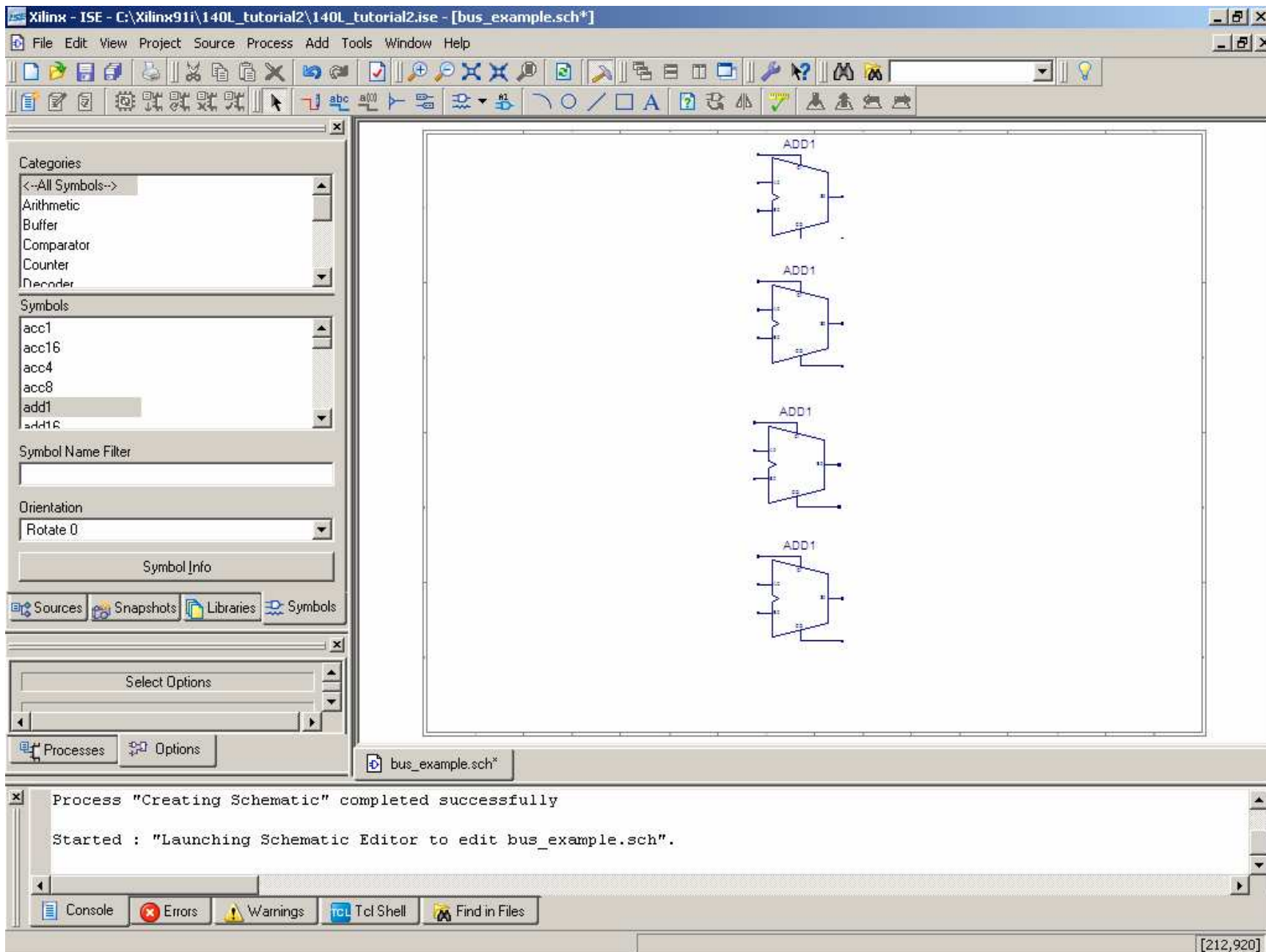
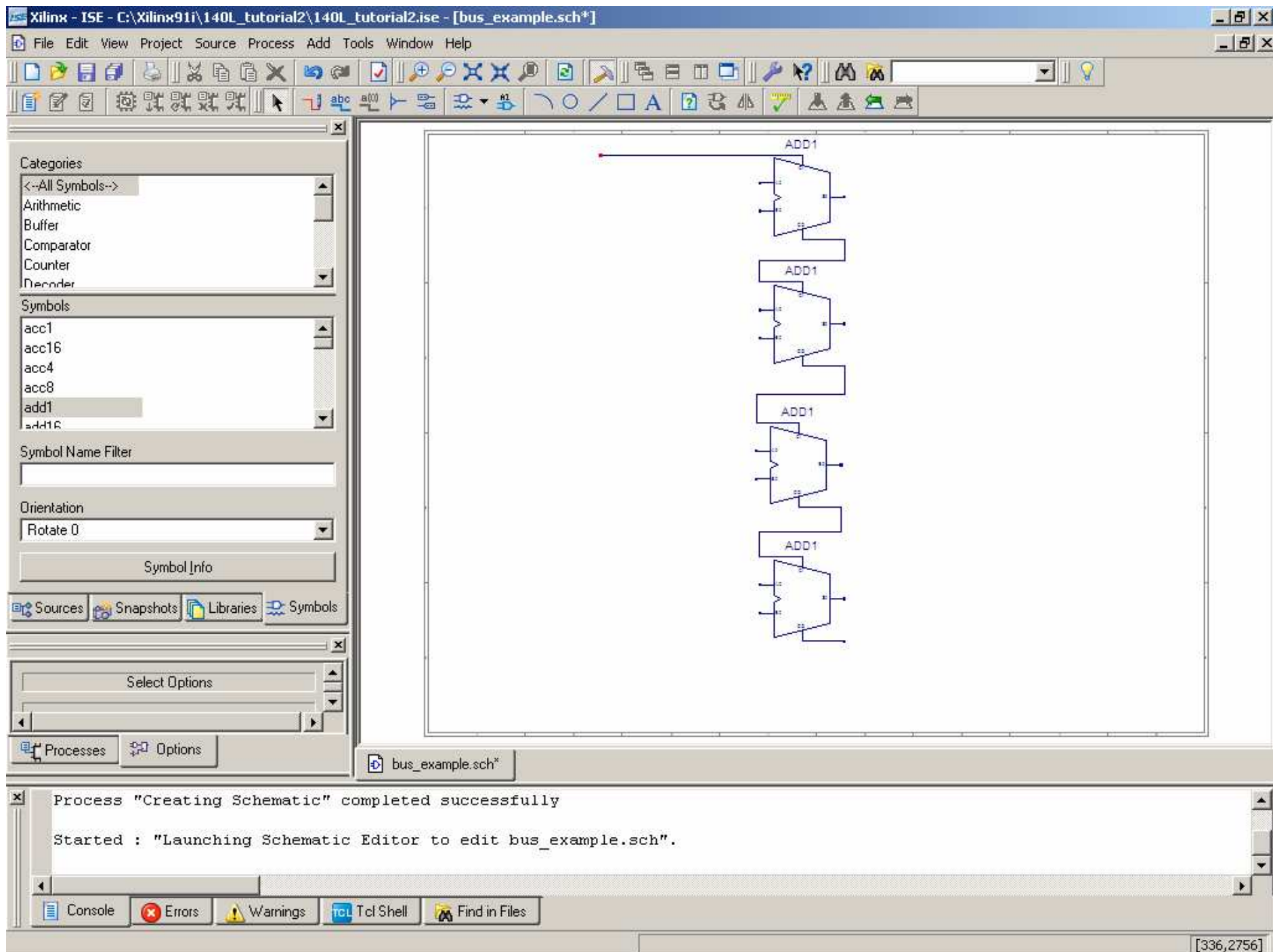
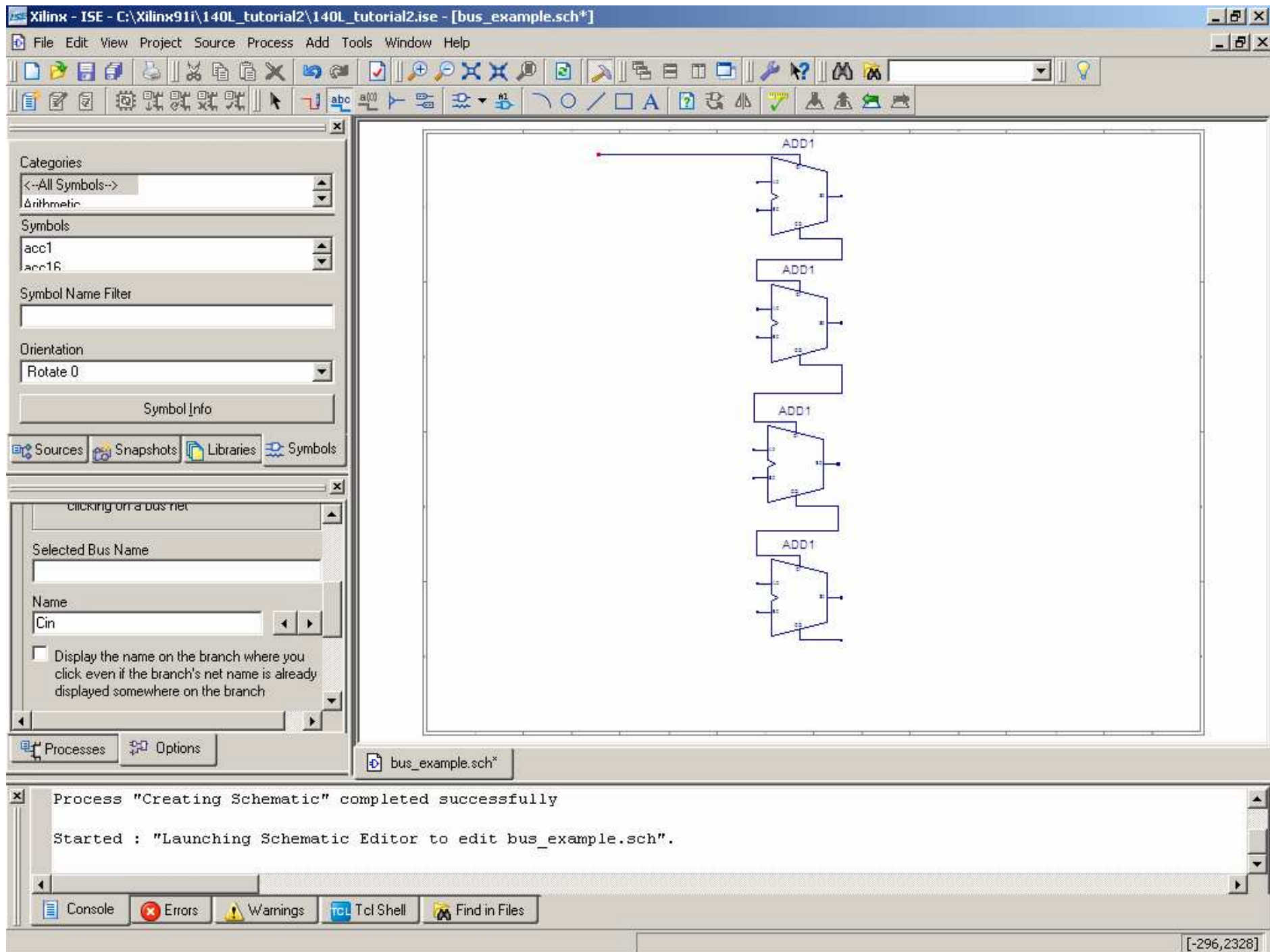




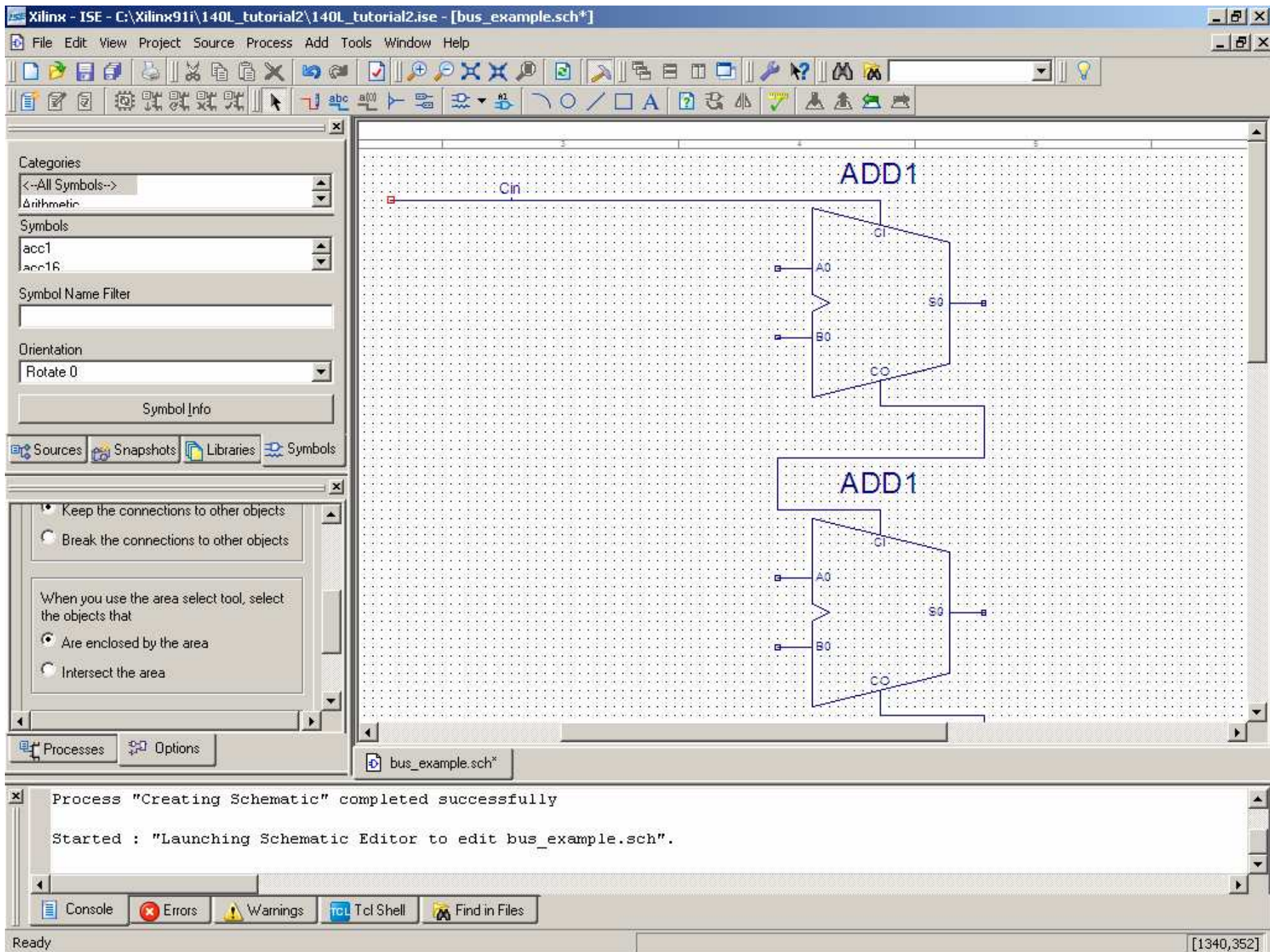
Assuming you know how to create a new project and add a new source. Now, put four “add1” (full-adder) in this new schematic editor.



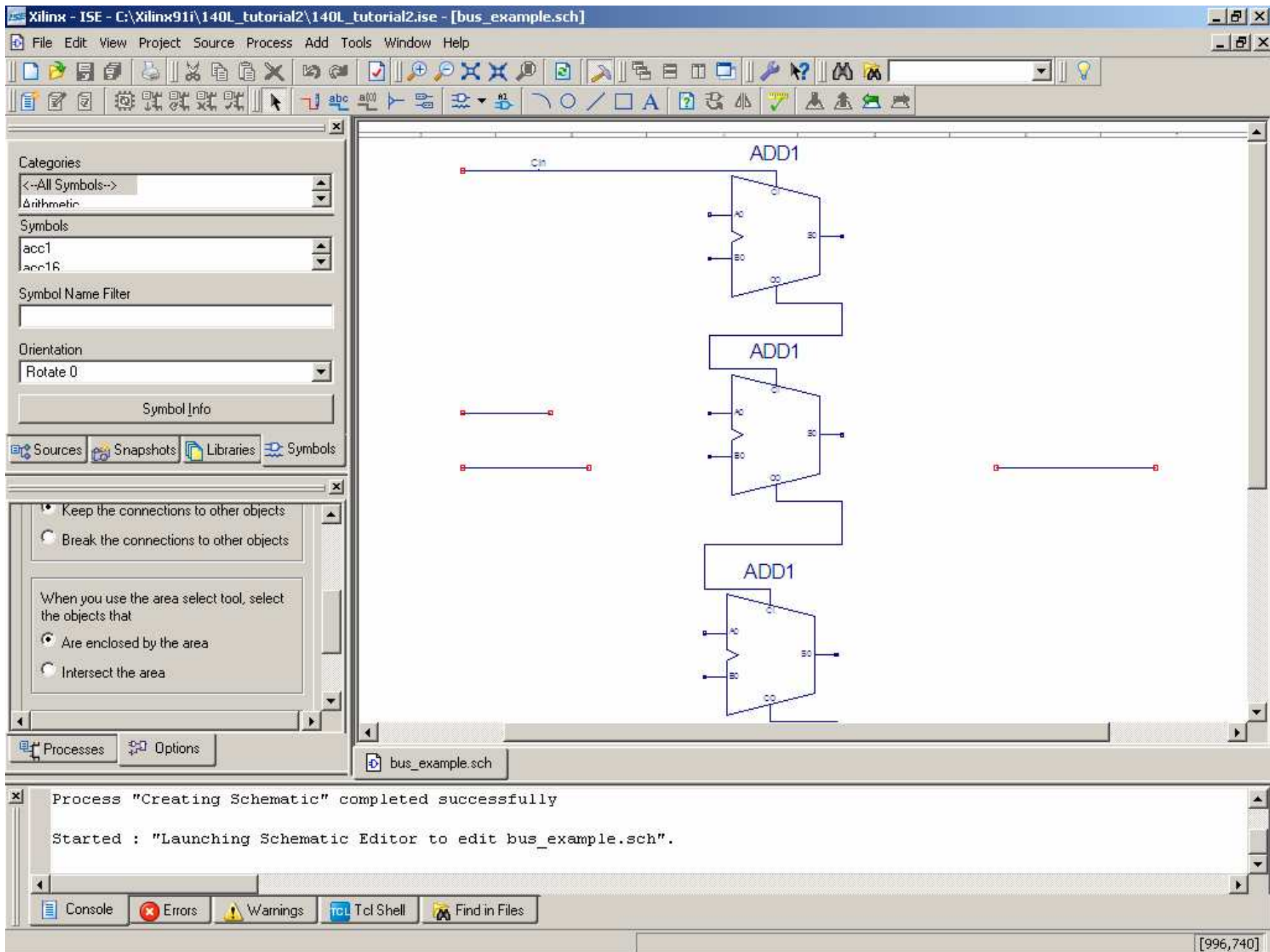
Use wire tool  to connect each CO port to the next CI port with single wire. And draw single wires to the first CI input and the last CO output.



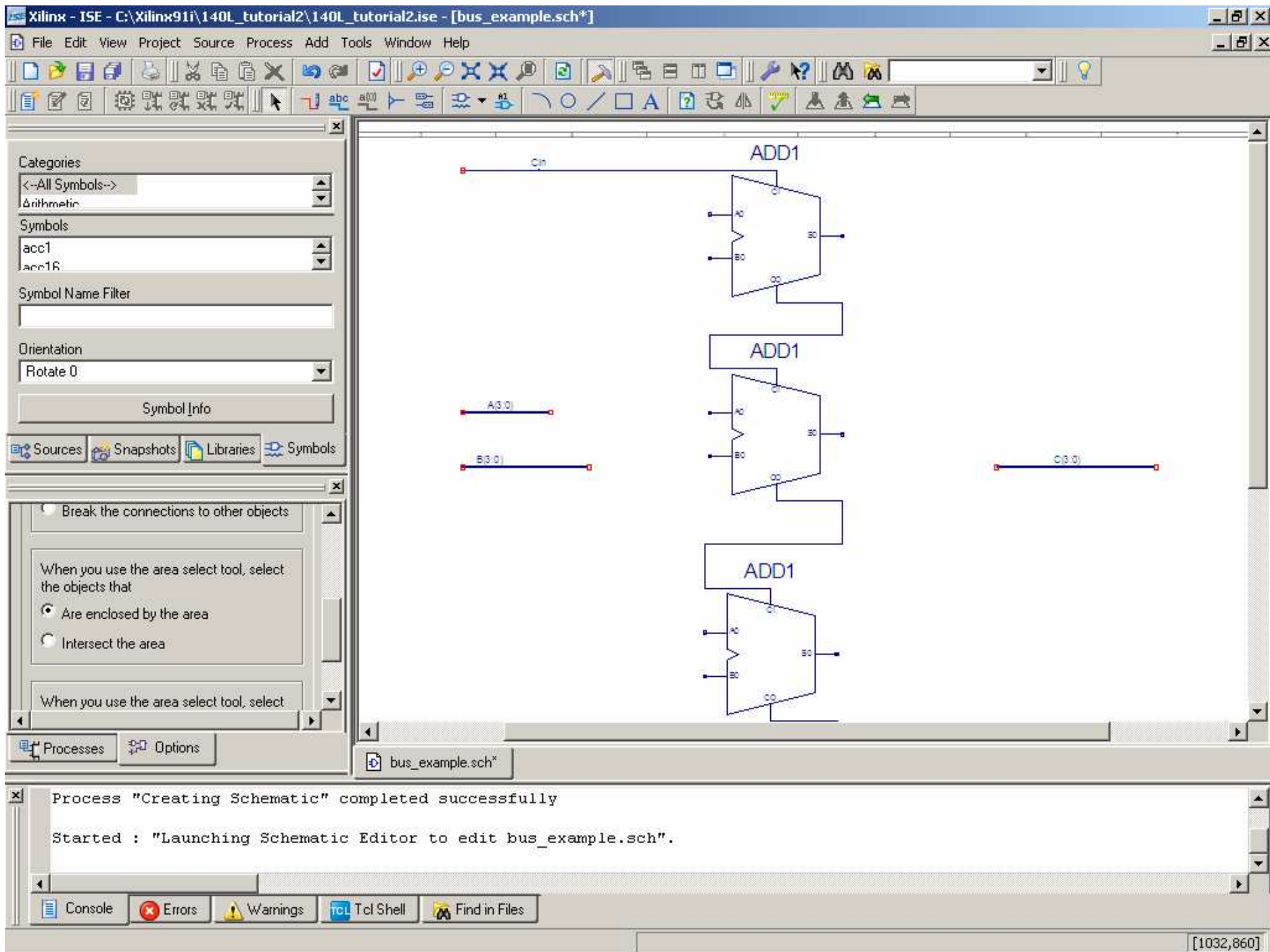
Click on the  tool bar, and input "Cin" to the Name field in the Options windows on the bottom-left. Click on the top input wire to name it as "Cin". And name the bottom output wire as "Cout". Note that you may need to scroll down in option-window to see all available options.



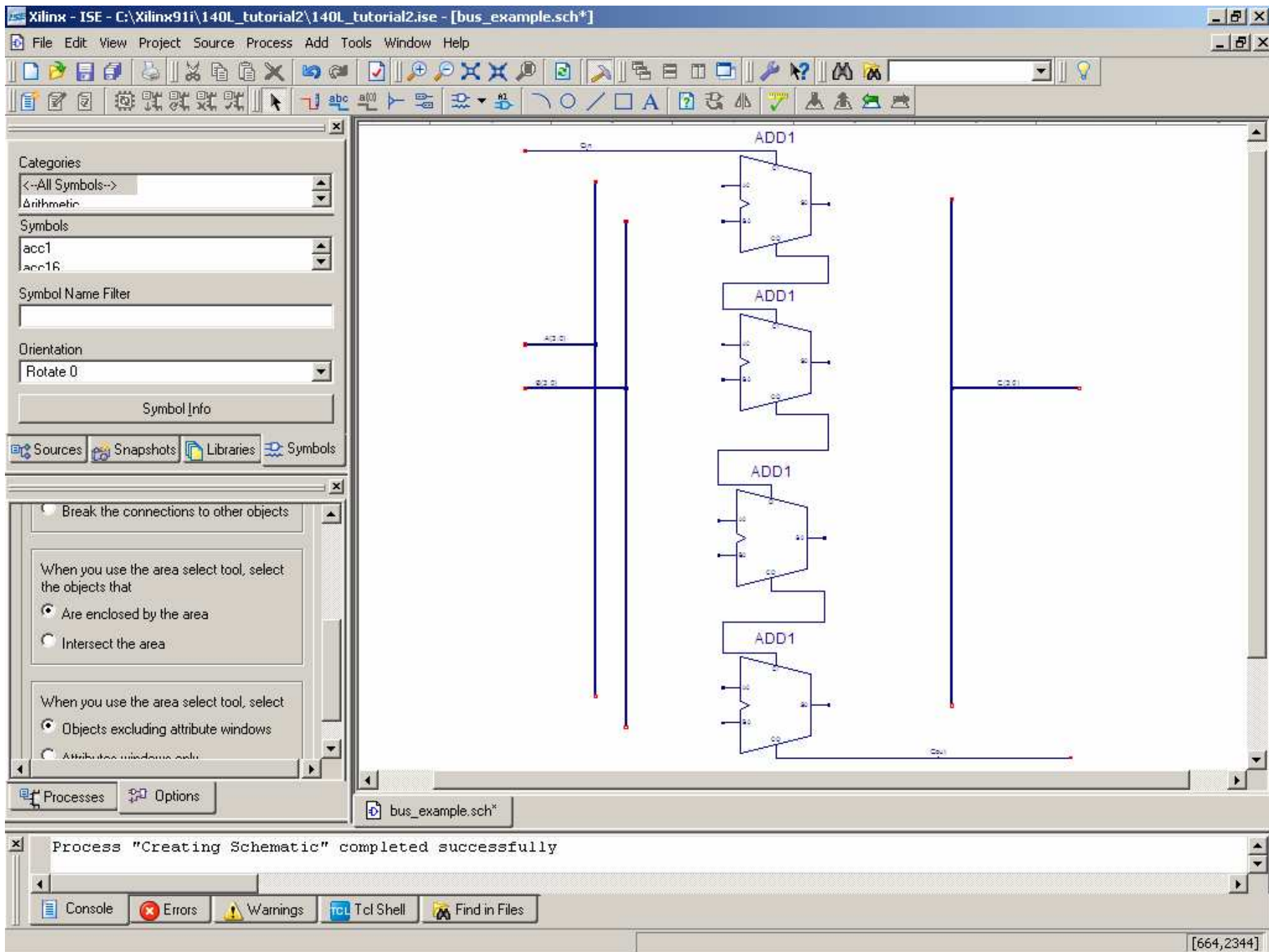
Zoom in to make sure the wires are named correctly (Cin shown above).



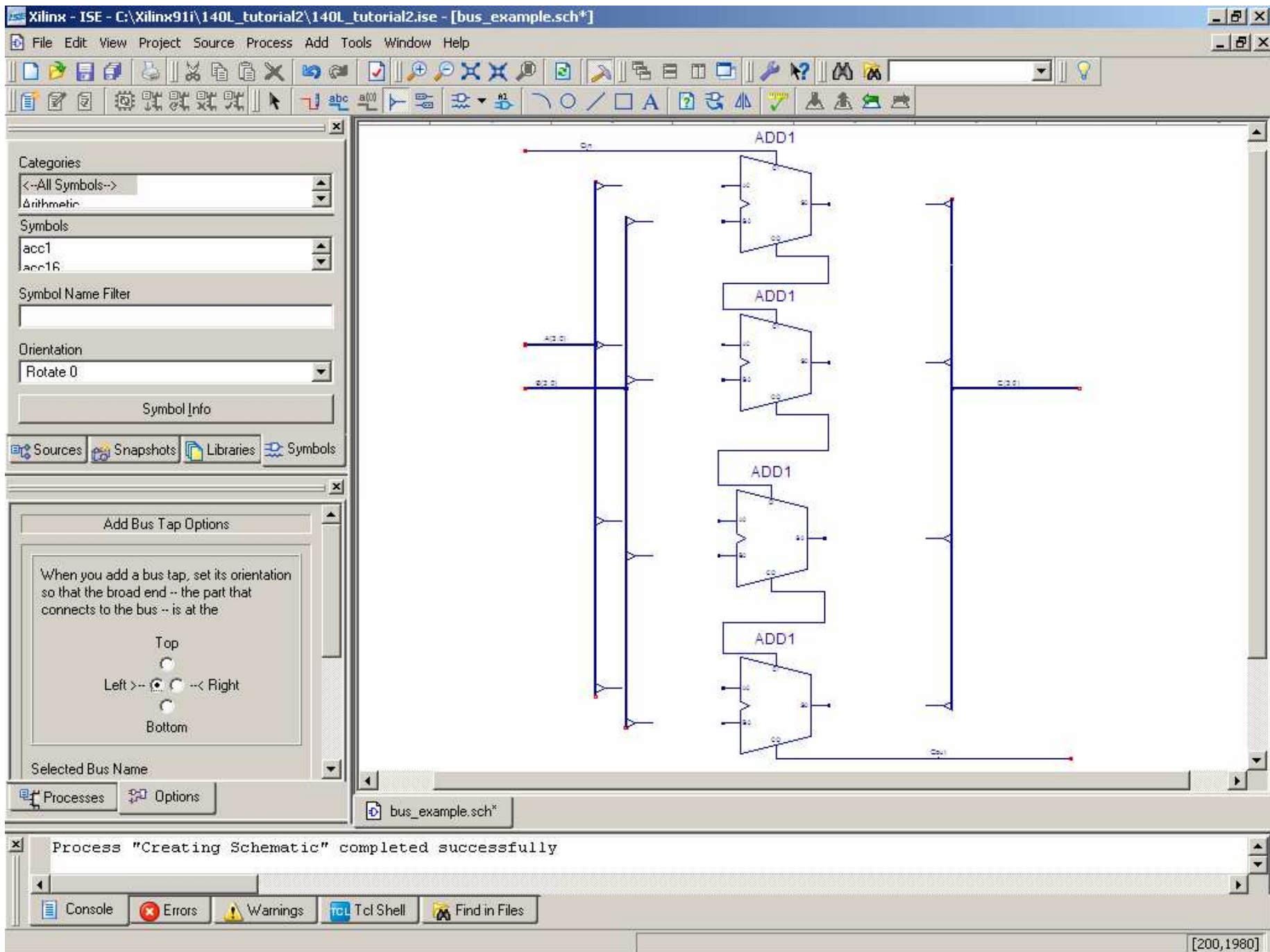
Draw three single wires as shown in the graph.



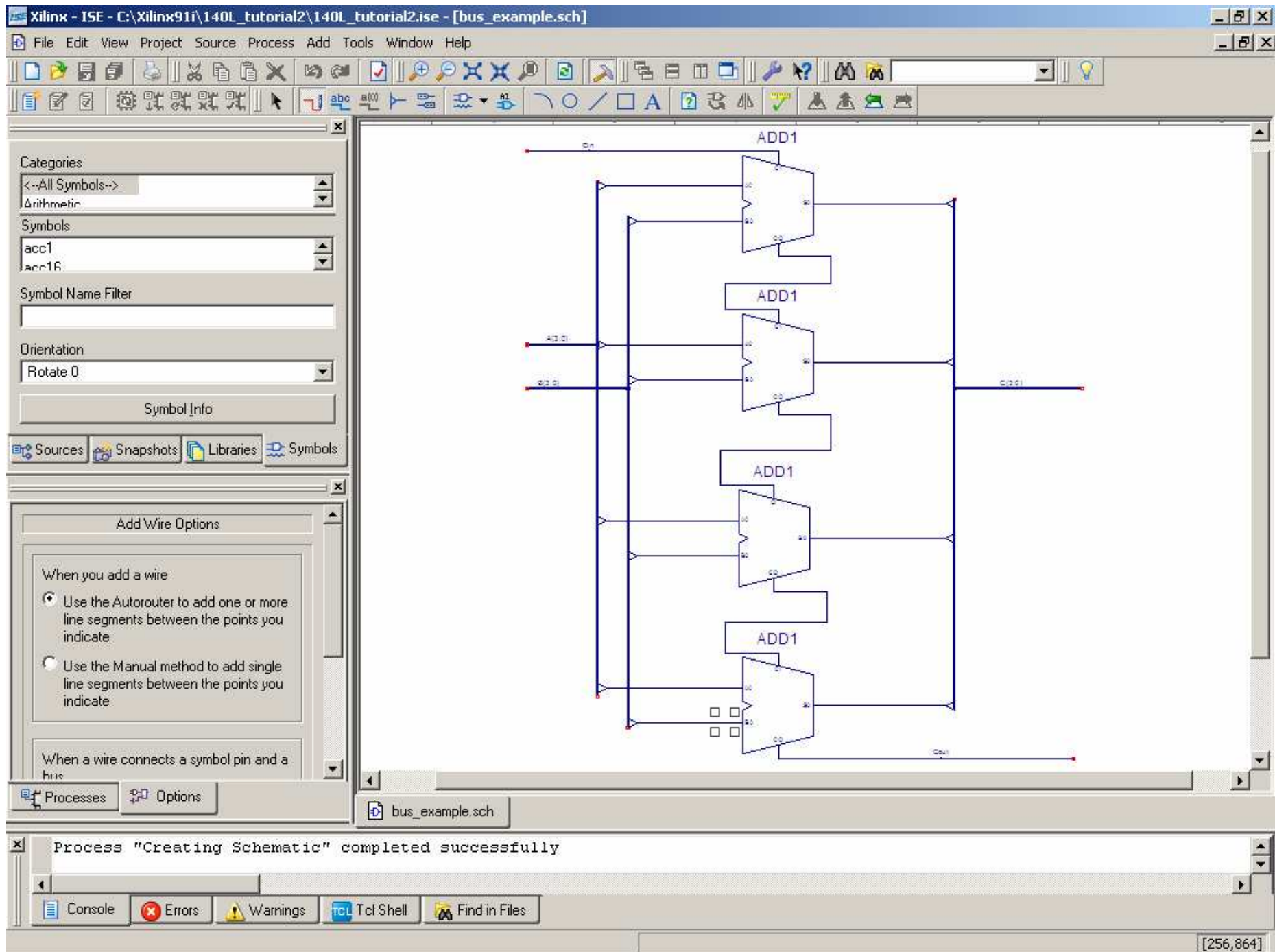
Using the same tool , name these wires as “A[3:0]”, “B[3:0]” and “C[3:0]”, as shown in the graph. Note that they become buses after naming.



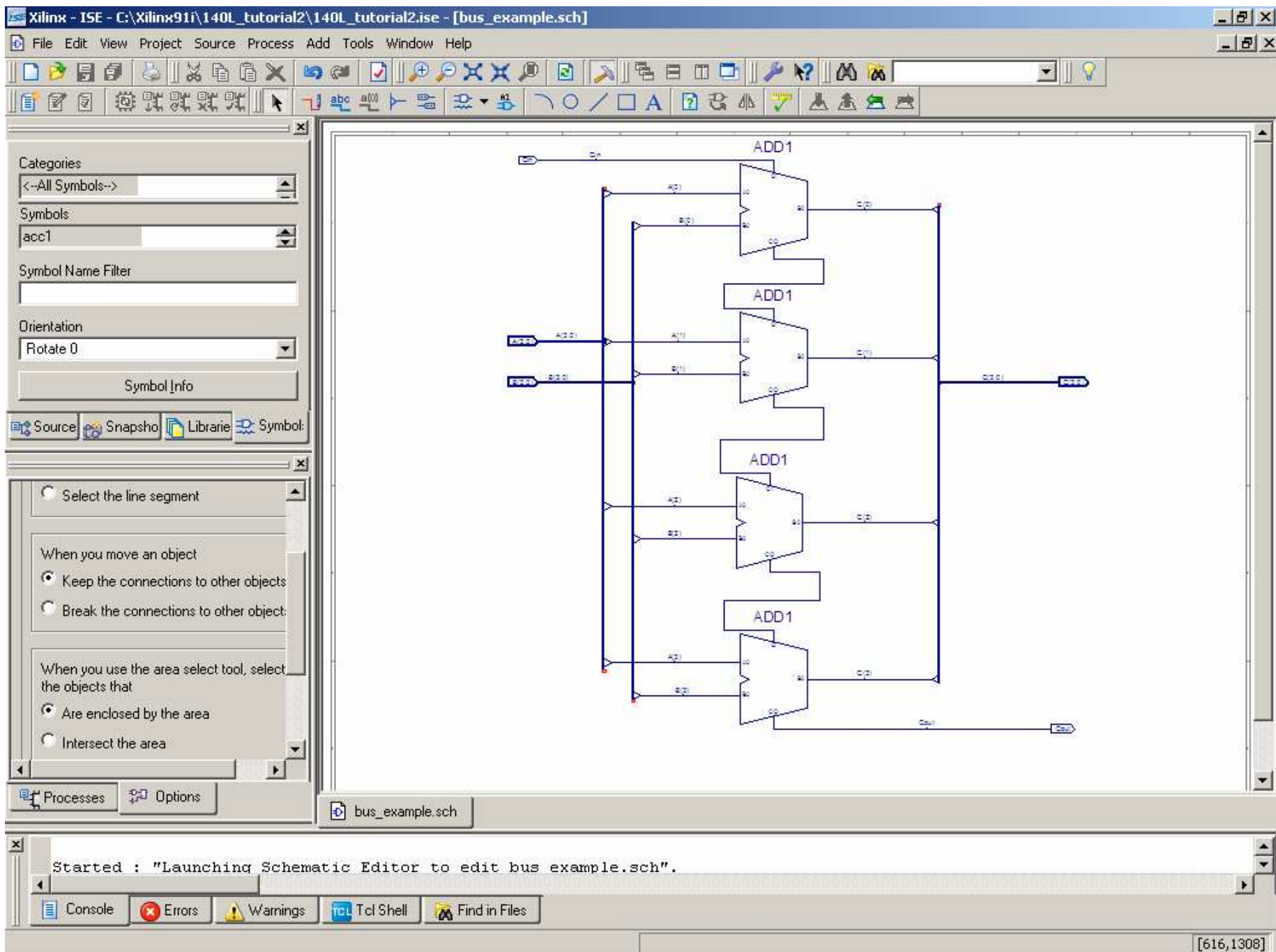
Extend these buses just as you would with regular wire (as shown above).



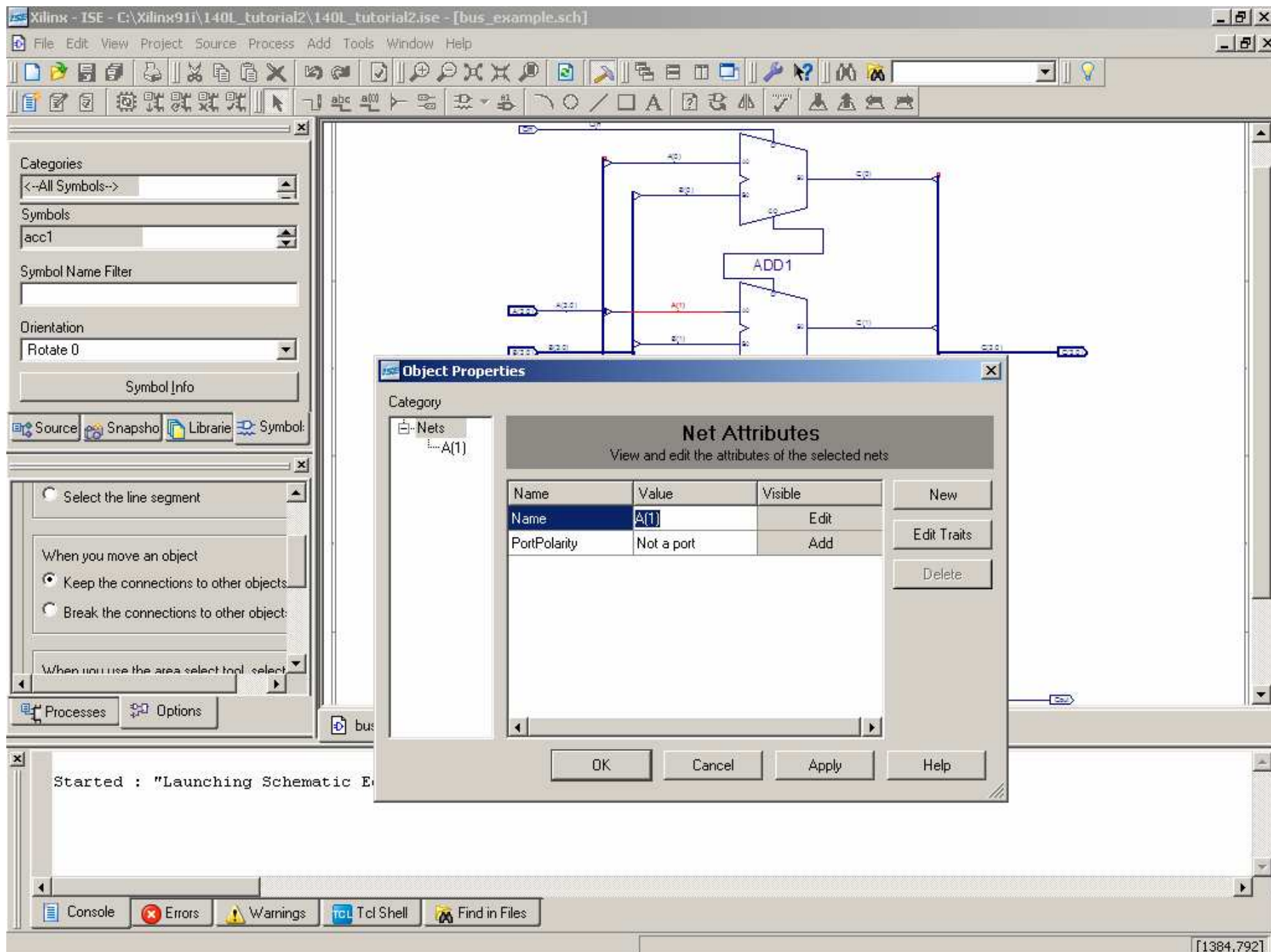
Put bus taps by using , as shown in the graph. The flat end must be aligned with the bus you want to connect. And you can change the tap orientation in the Options window.



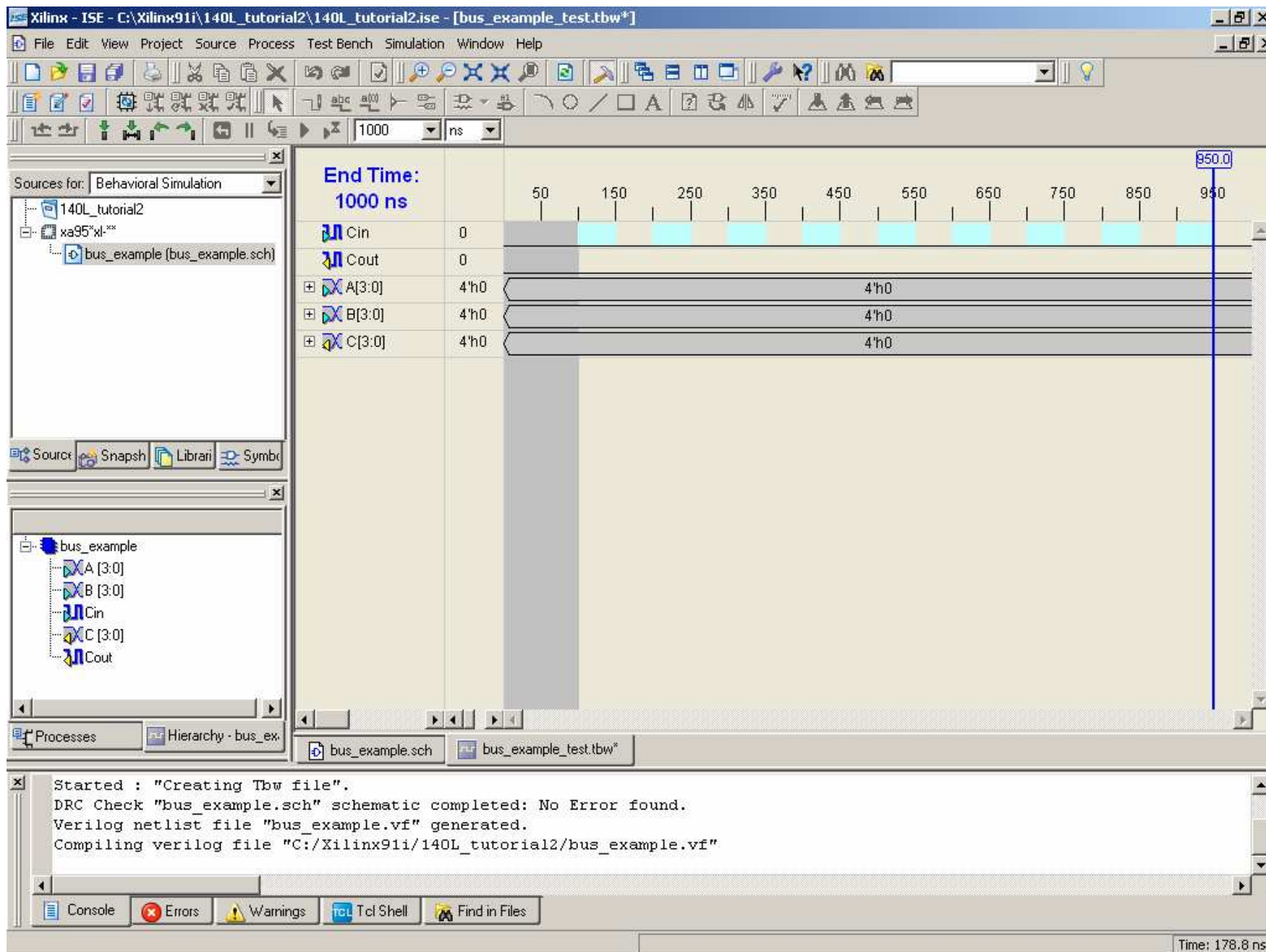
Connect each tap to a port of ADD1 as shown above.



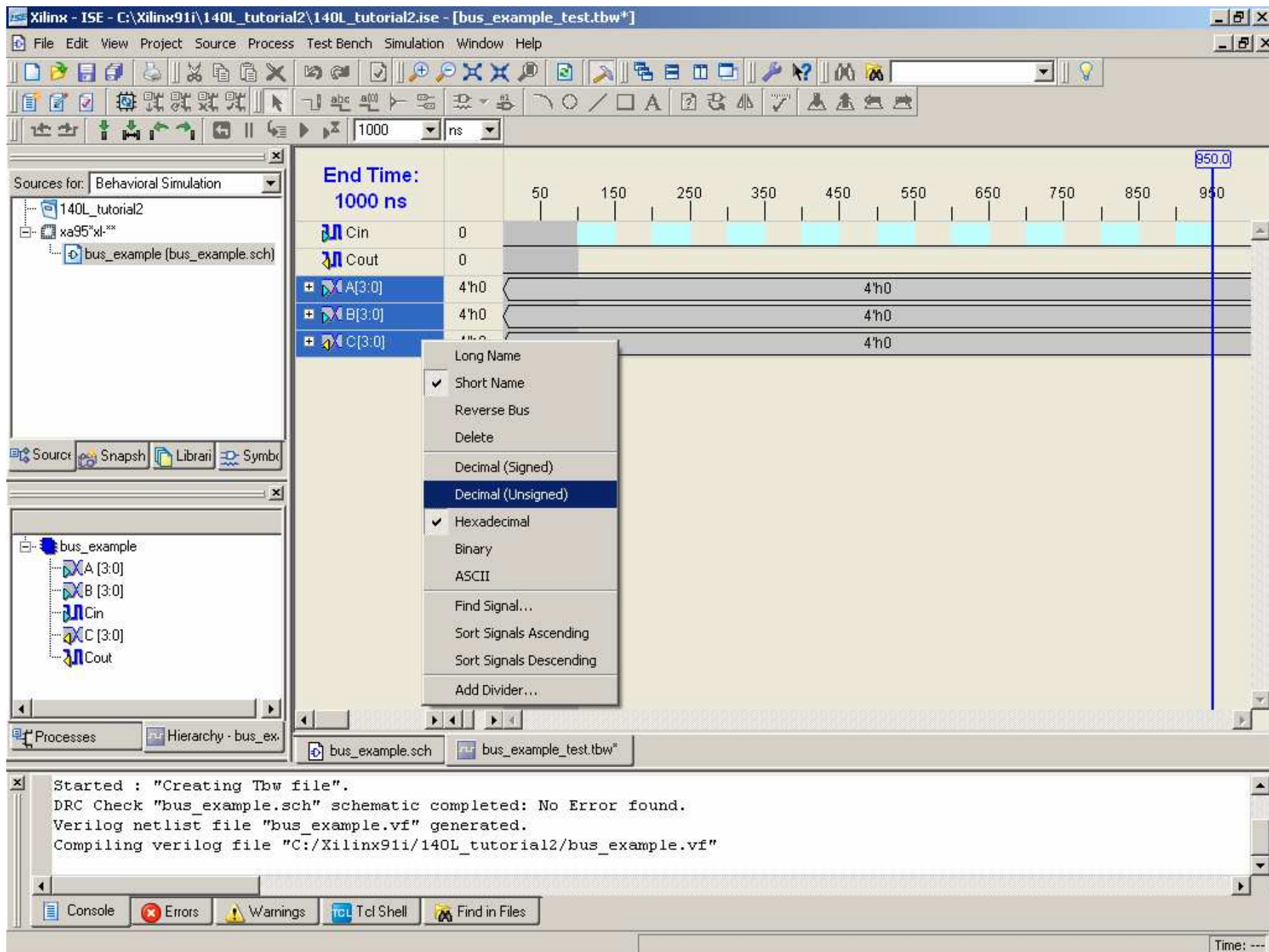
Now, add the ports to each of the input & output. Note, all you need to do is select the  then click on each of the bus you wish to connect the port to. The port will inherit the name of the bus/wire. Name the each single wire as shown in the graph (i.e, A(0), B(0), A(1), B(1)...). Note that conceptually bus tap doesn't connect wires, but extends some wires from a bus. Therefore the branch must be a subset of the source bus, and they must have the same name.



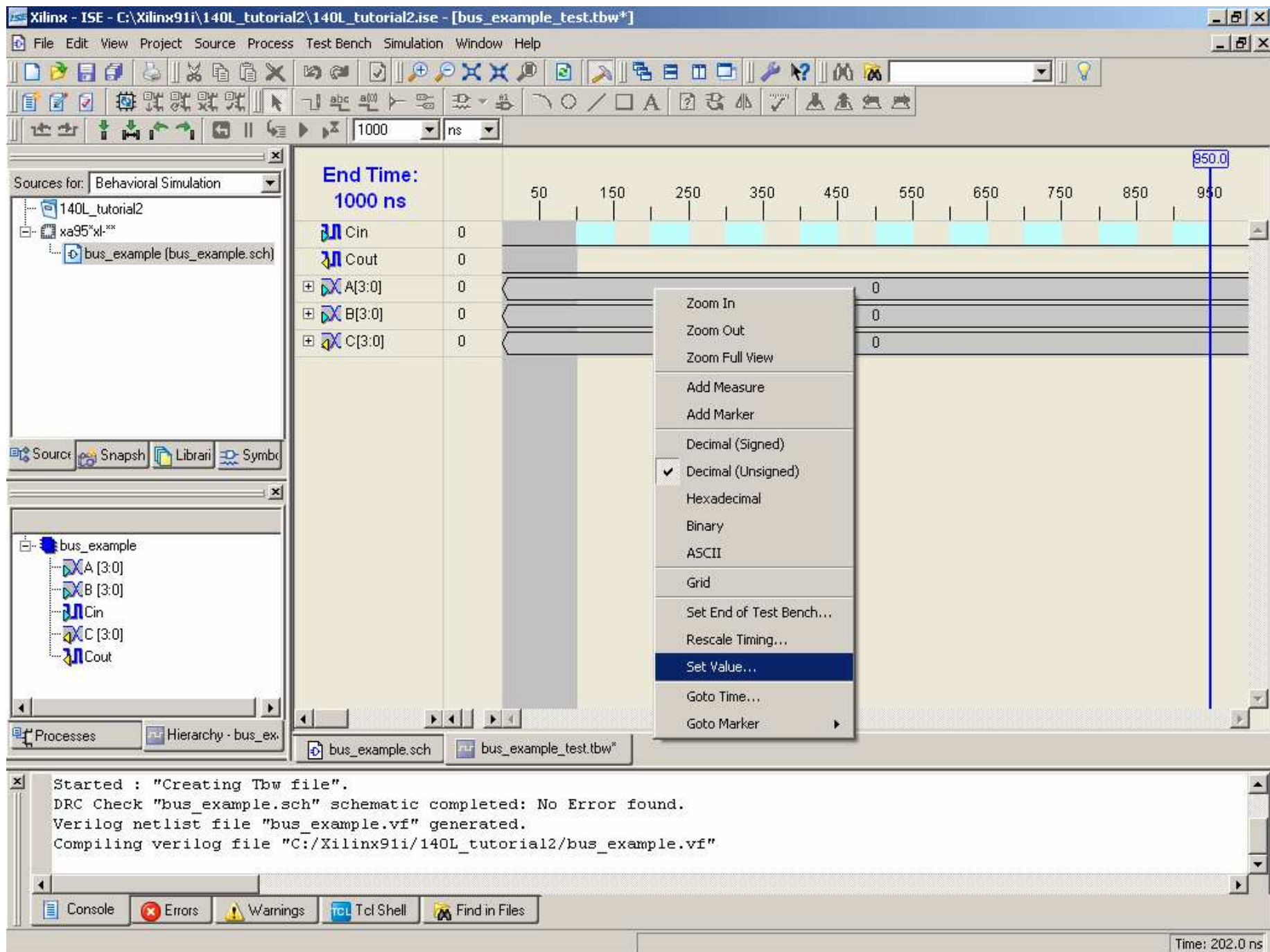
To verify a bus tap, double click the bus tap, an object properties window will pop up. Check the names of connected nets.



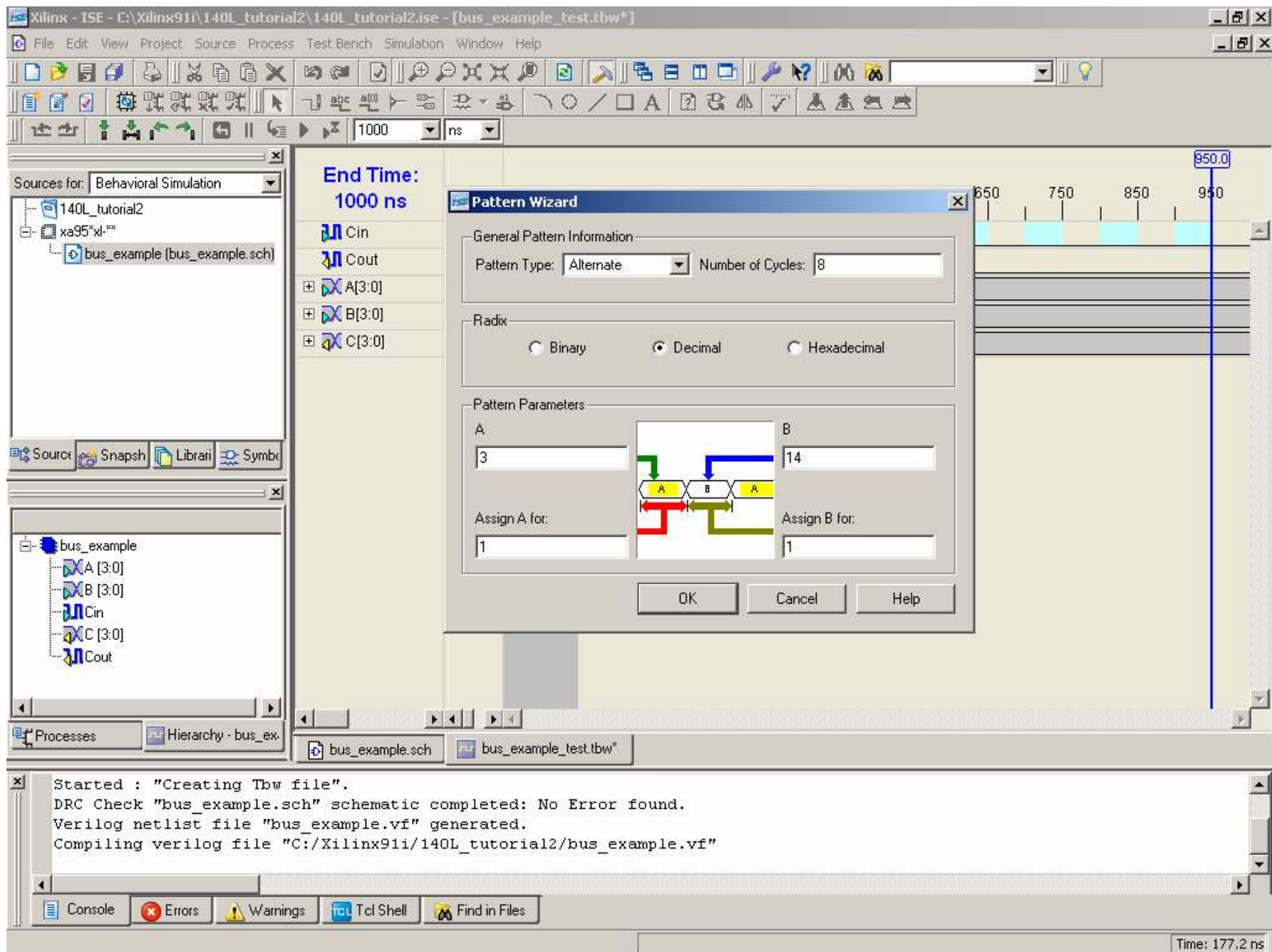
Now, follow the same steps as you did to create a test-bench in lab1 and you should come to this screen.



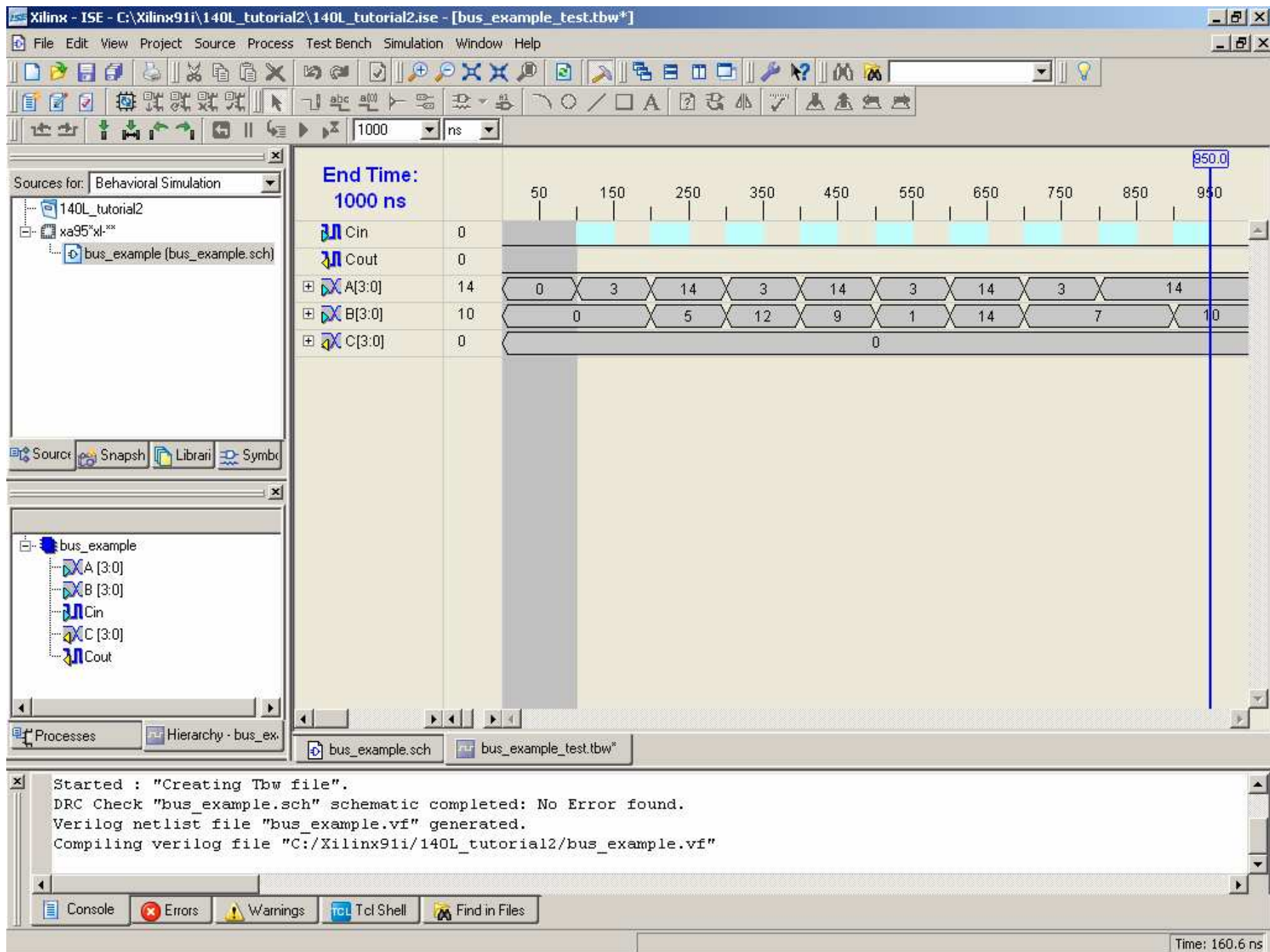
Highlight the input buses and right click to set the value as Decimal (Unsigned) value.



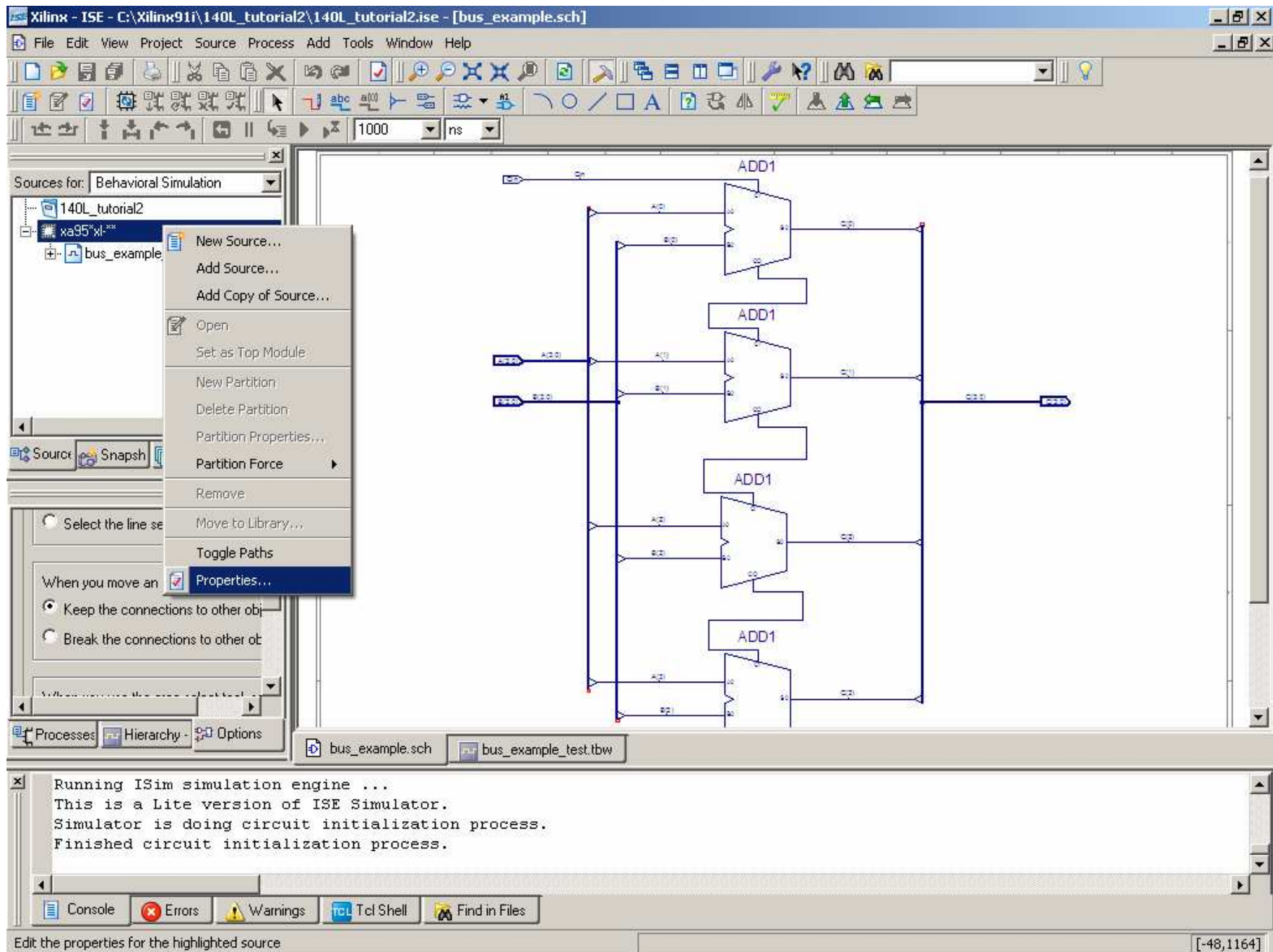
Right click on bus "A", and select "set value..." in the pop-up menu.



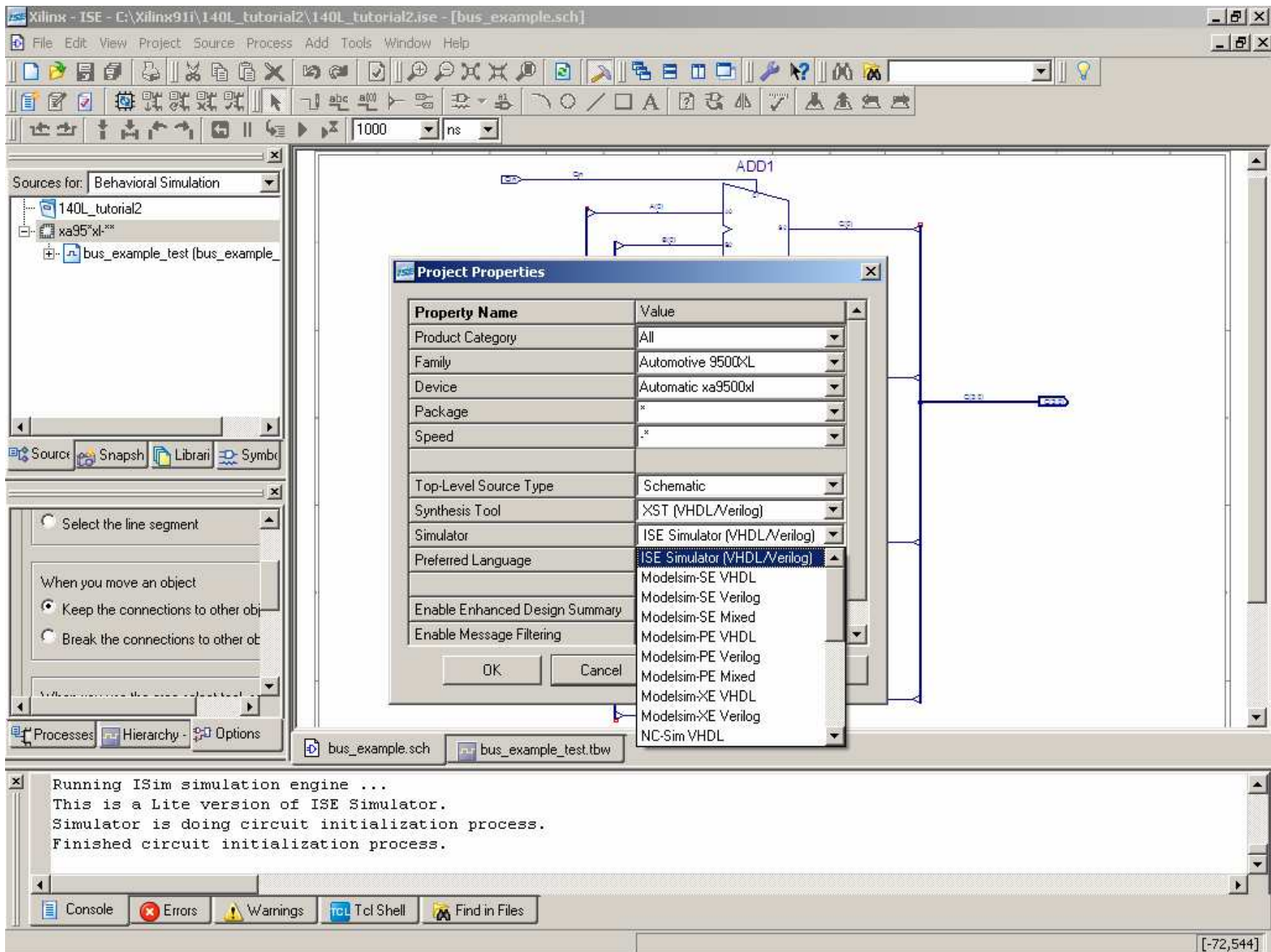
In the “Set Value” screen, click “pattern wizard” button. You will see the “pattern wizard” window. You can set alternate, count, shift and random value to a bus. At this step, we set bus “A” to alternate, as shown.



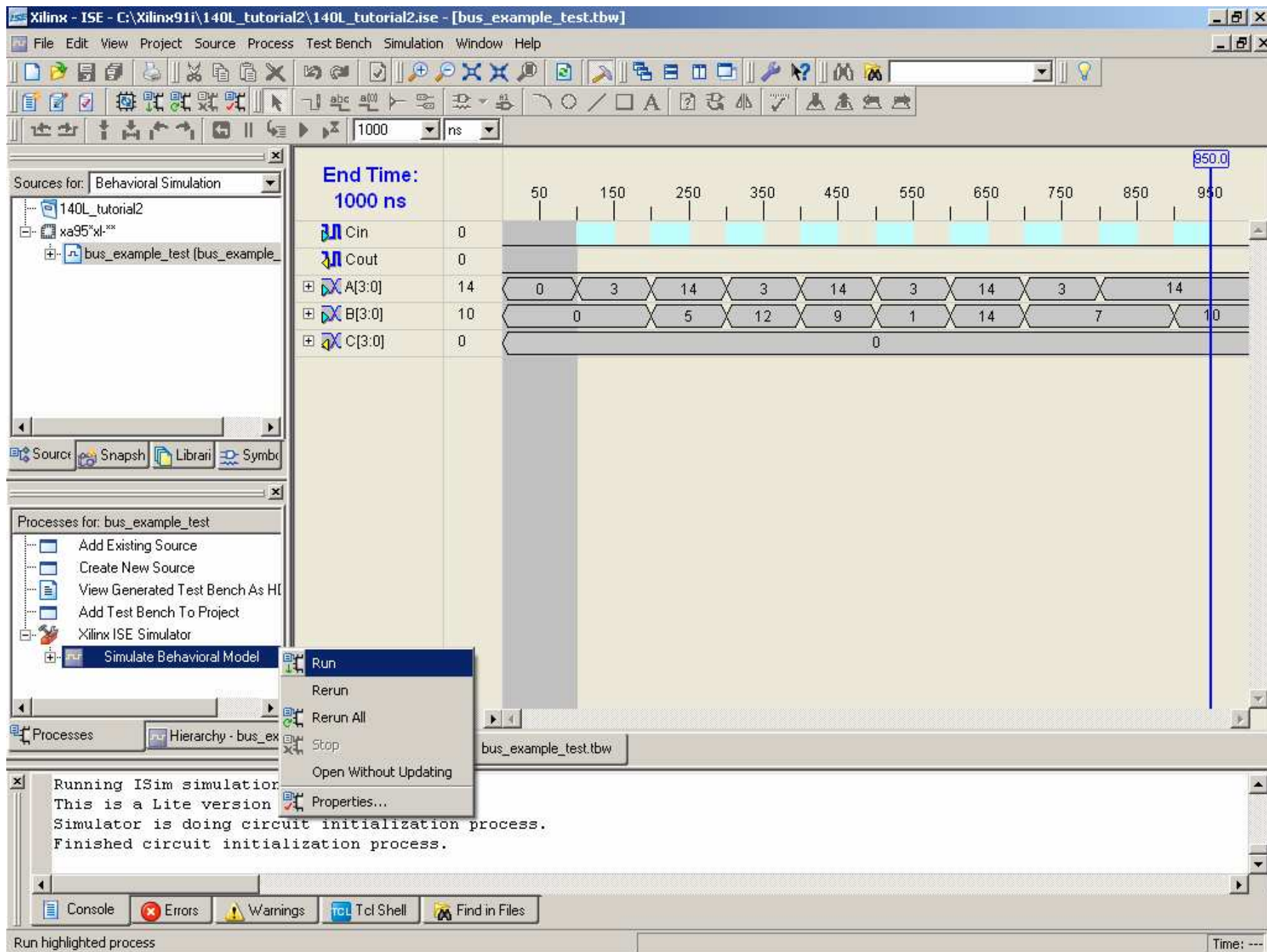
For B[3:0], use the “Random” option the in Pattern Wizard window and you should see some random value assigned as shown above. Save you work.



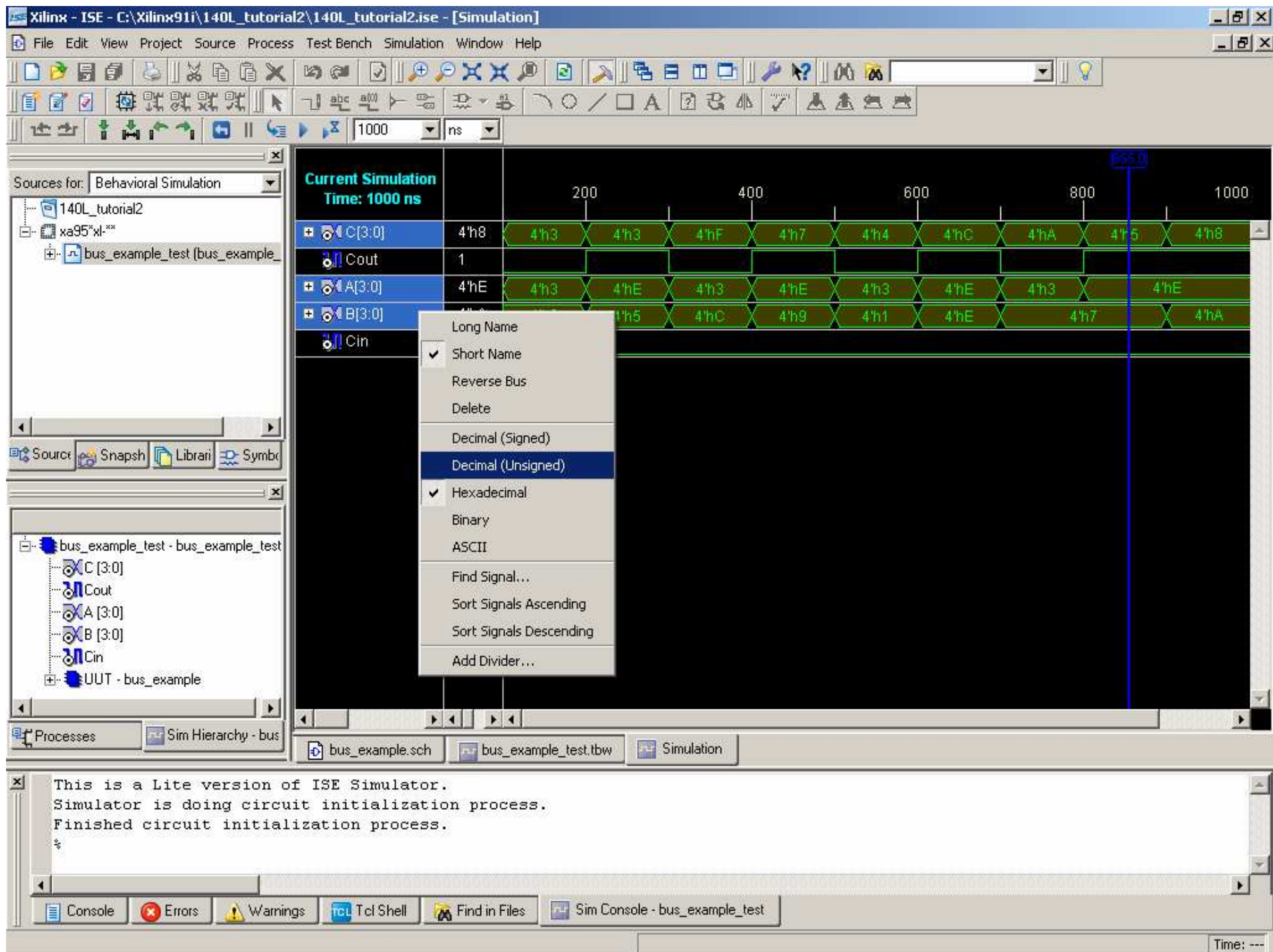
Let's use a different simulator this time. Take a look at the Device's property as shown above.



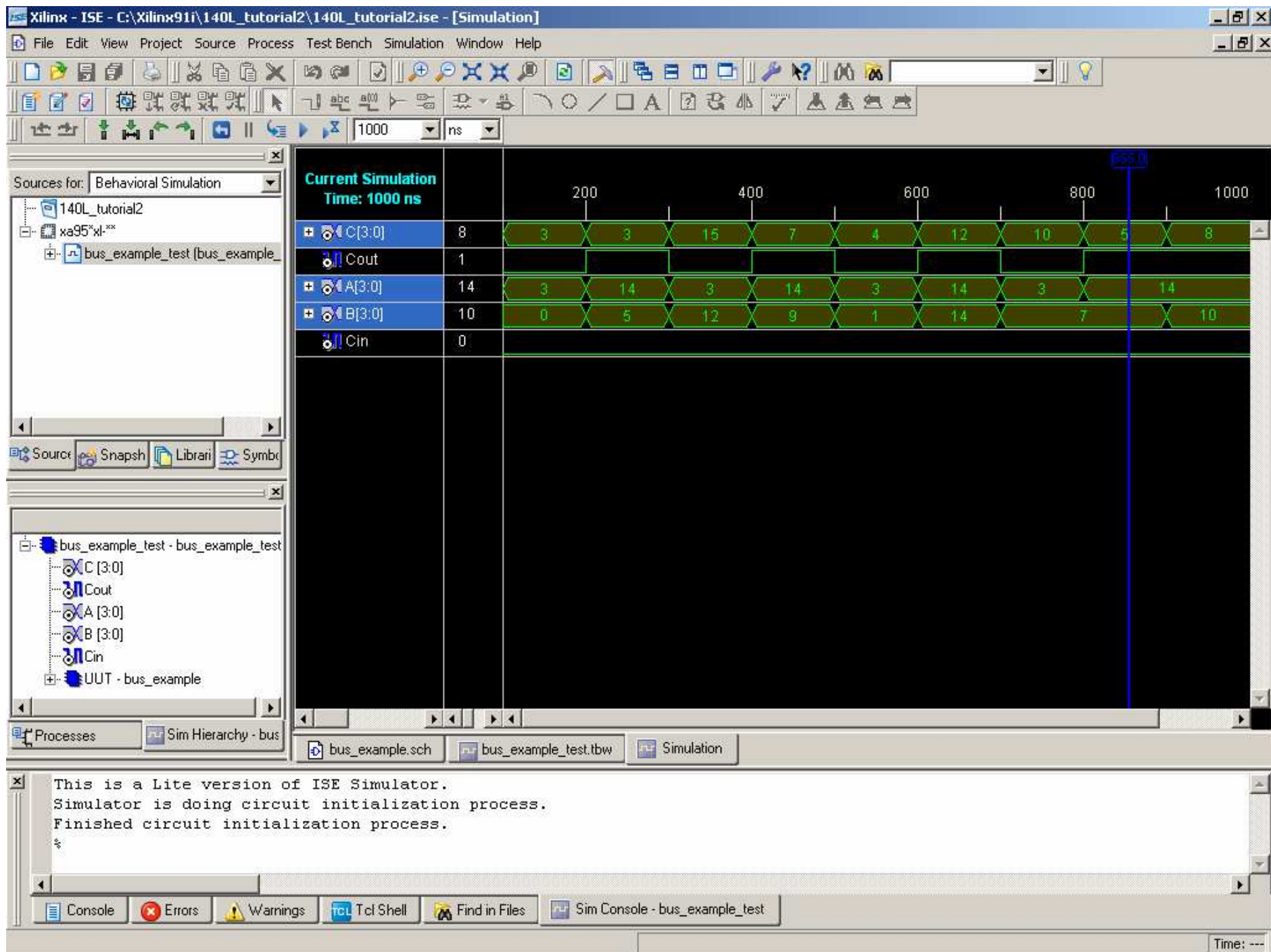
Be sure to select “ISE Simulator (VHDL/Verilog)” as Simulator. And, you can choose either VHDL or Verilog as the preferred language.



Now, run the simulation.



You can choose to see the result in many different formats. Let's take a look at the result in Decimal.



If you see this screen, you are ready for lab 2. Good luck! You may choose to use either ModelSim or ISE Simulator for your lab assignments. As you can see, ISE Simulator is easier to work with but with less features compare to ModelSim.