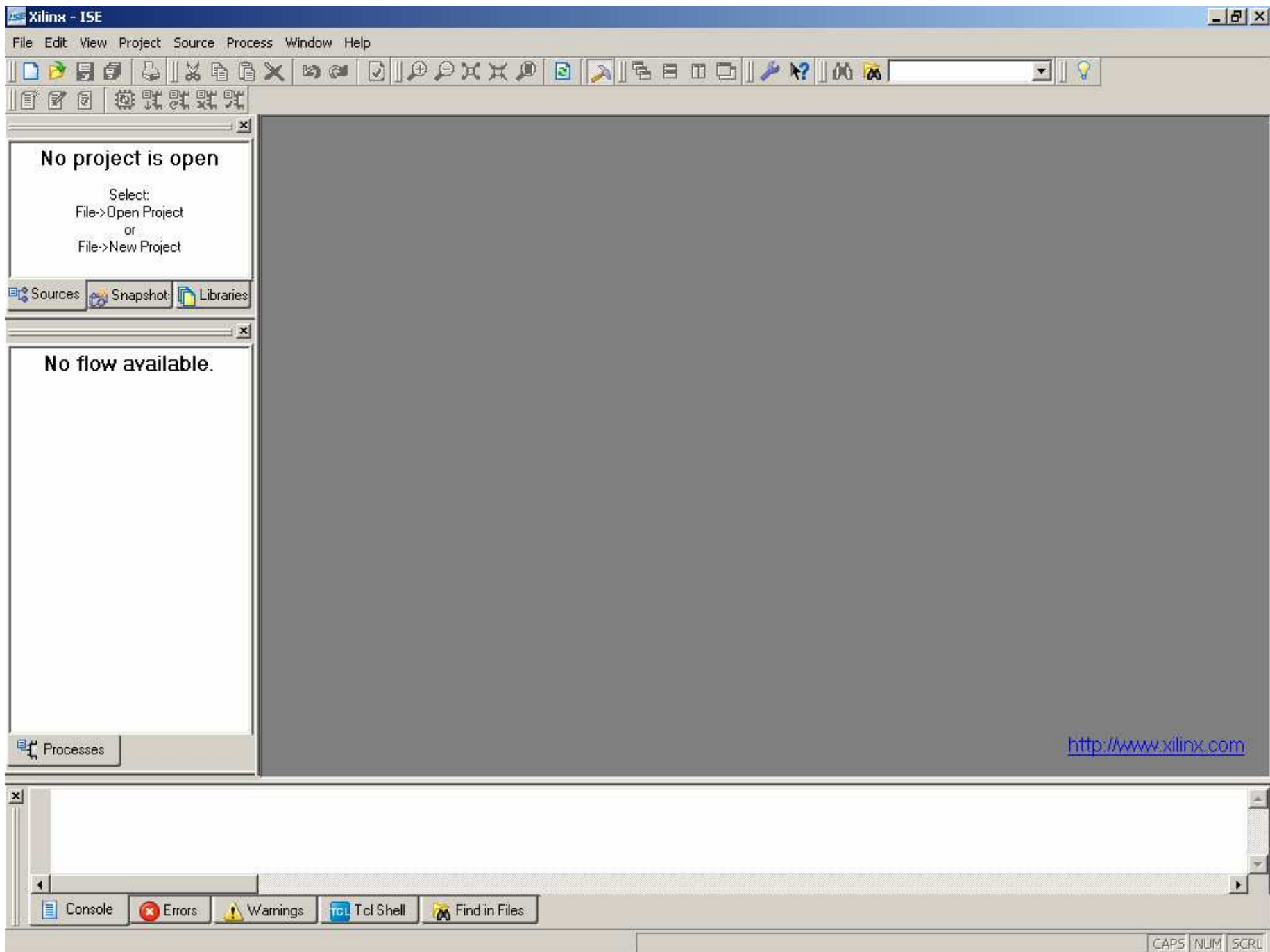
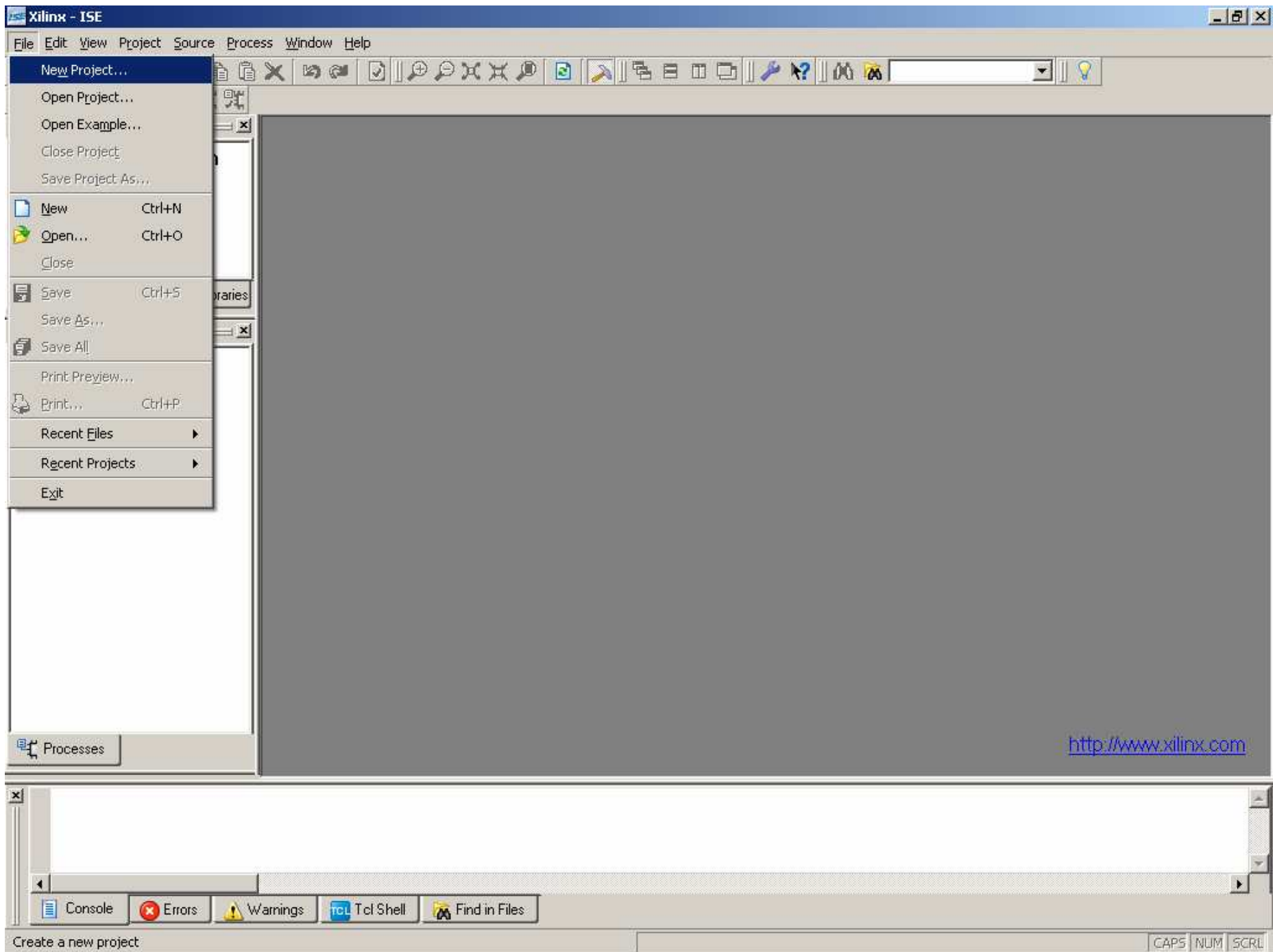
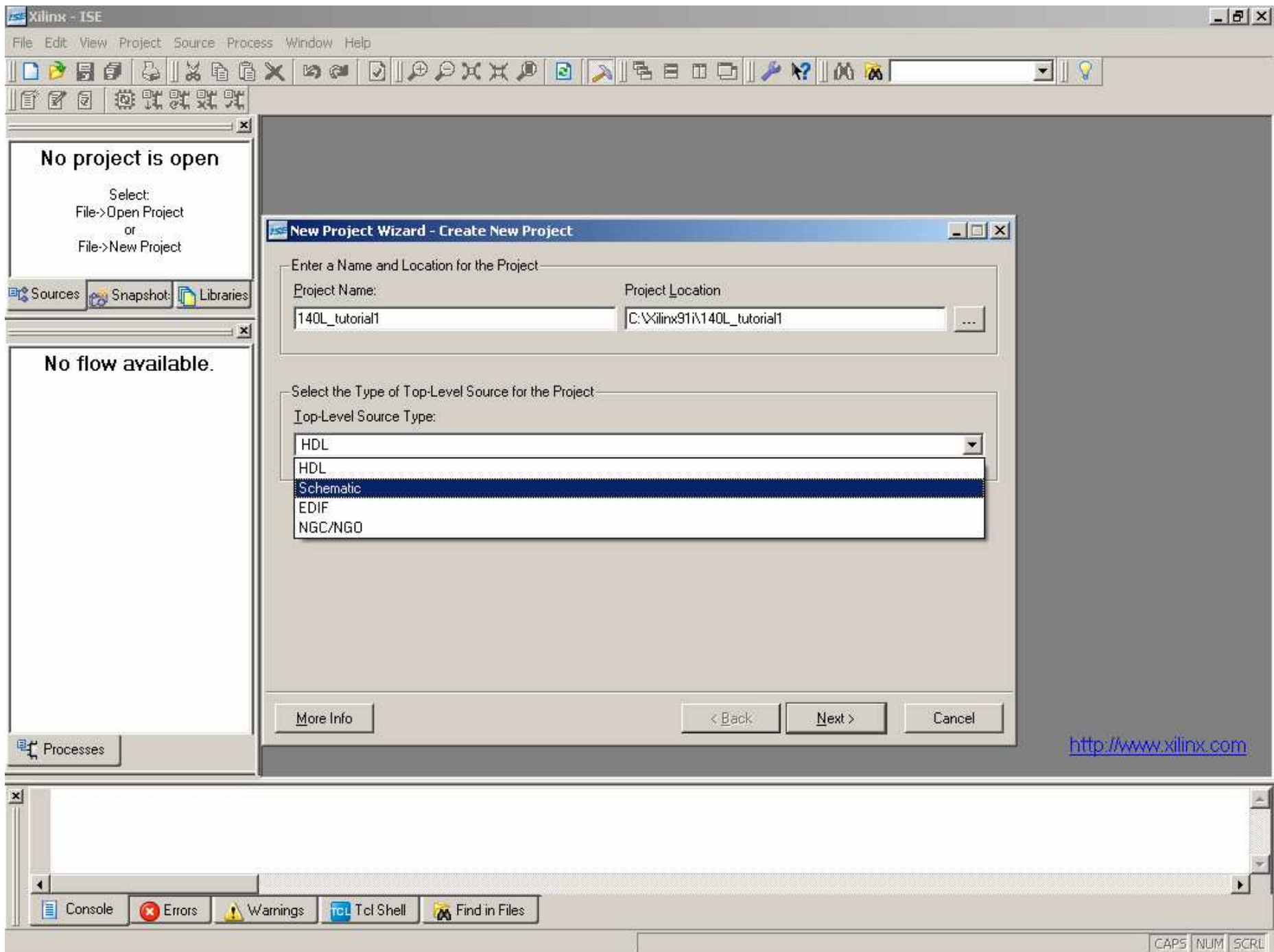




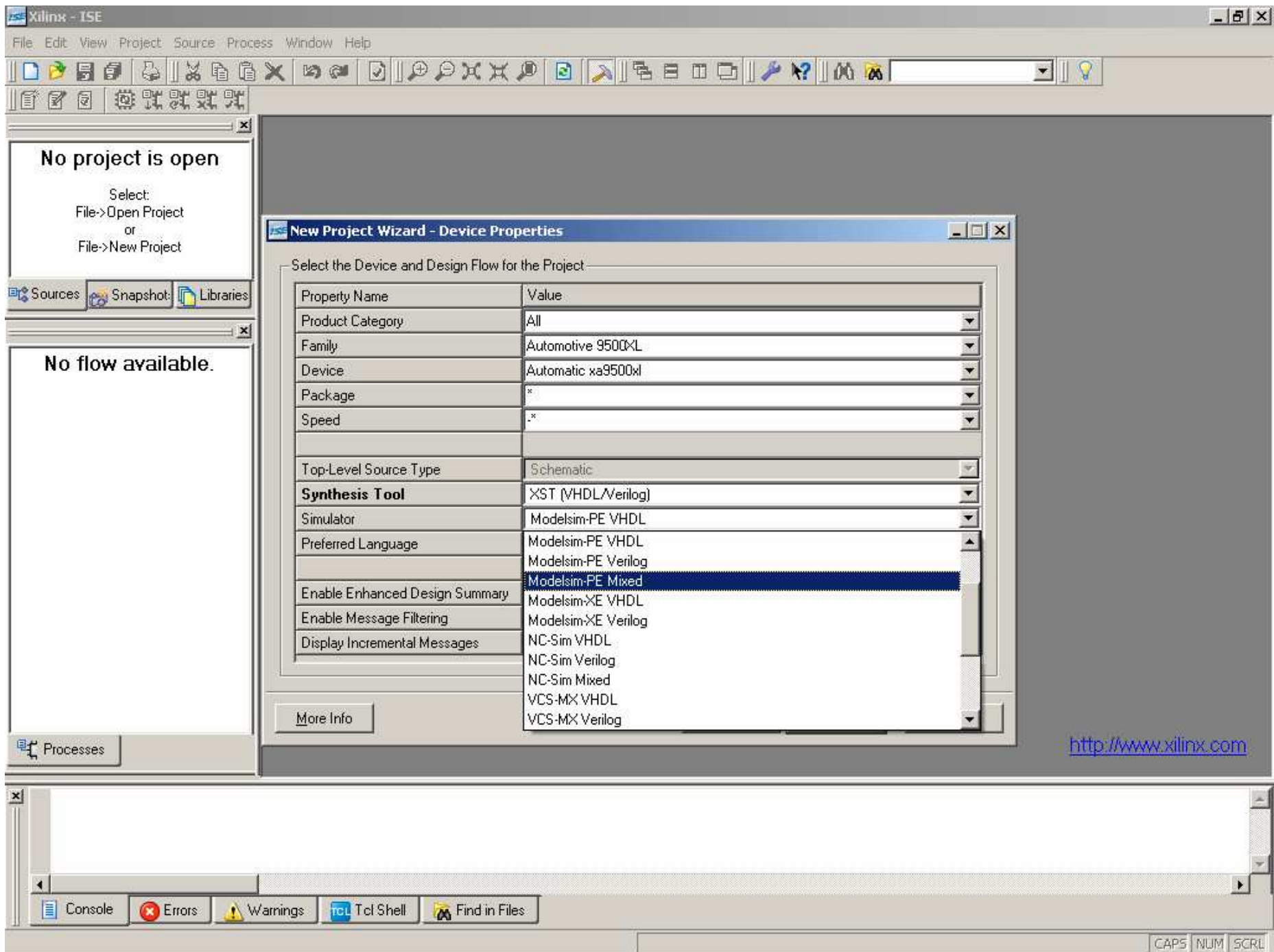
After opening the Programs> Xilinx ISE 9.1i > Project Navigator, you will come to this screen as start-up.



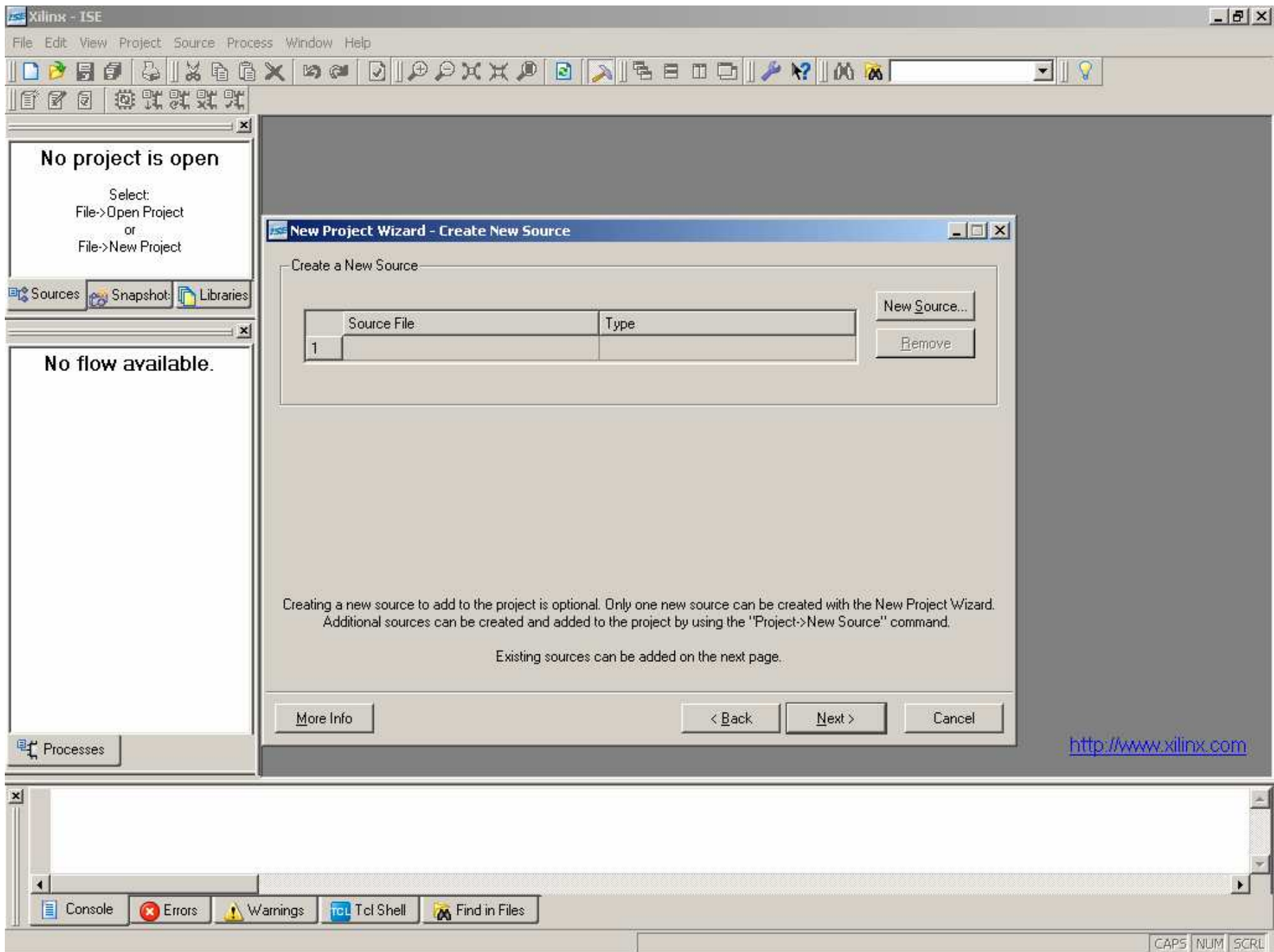
Start with a new project.



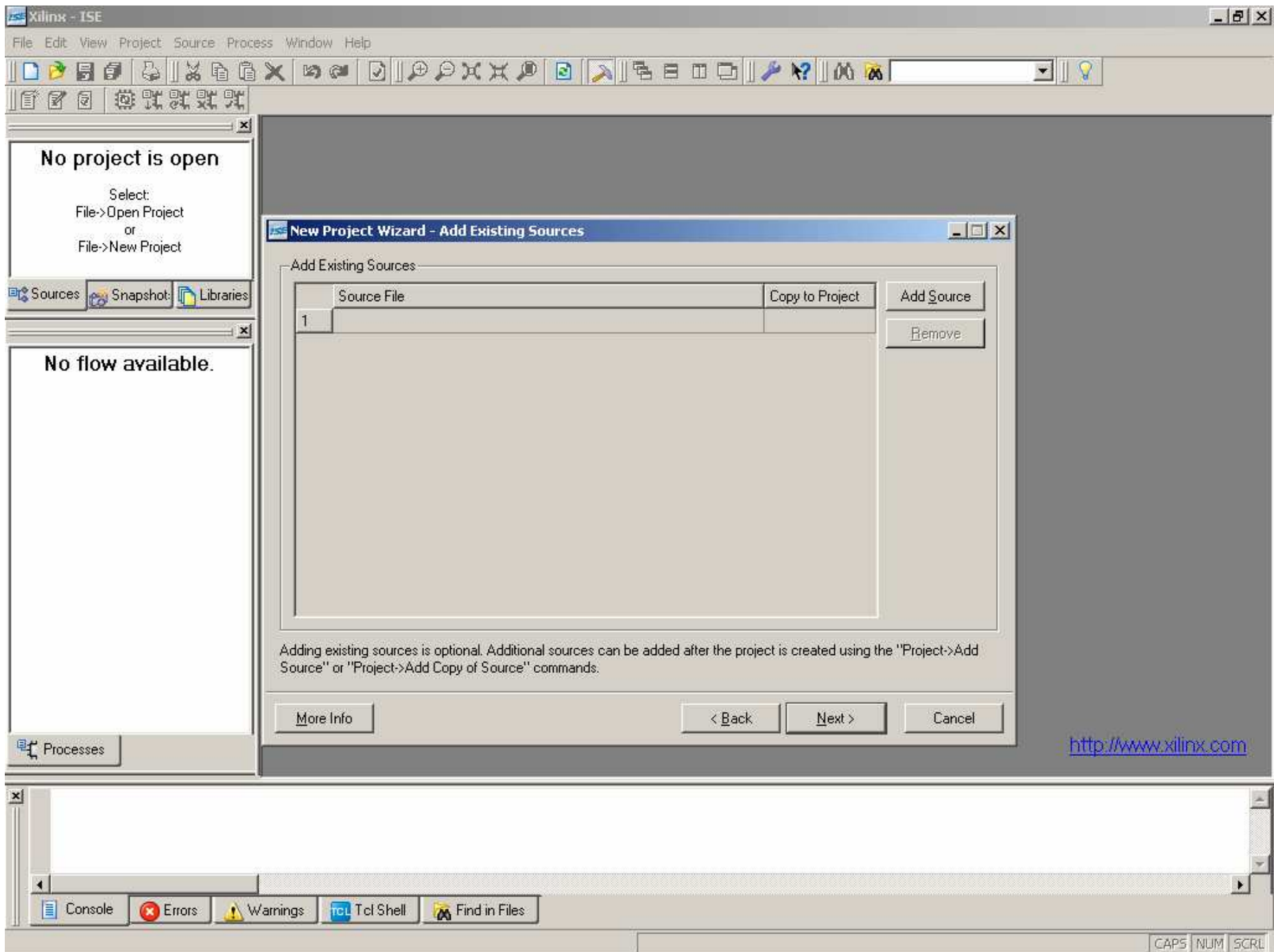
Enter a project name and be sure to select “Schematic” as the Top-Level Source Type and click Next.



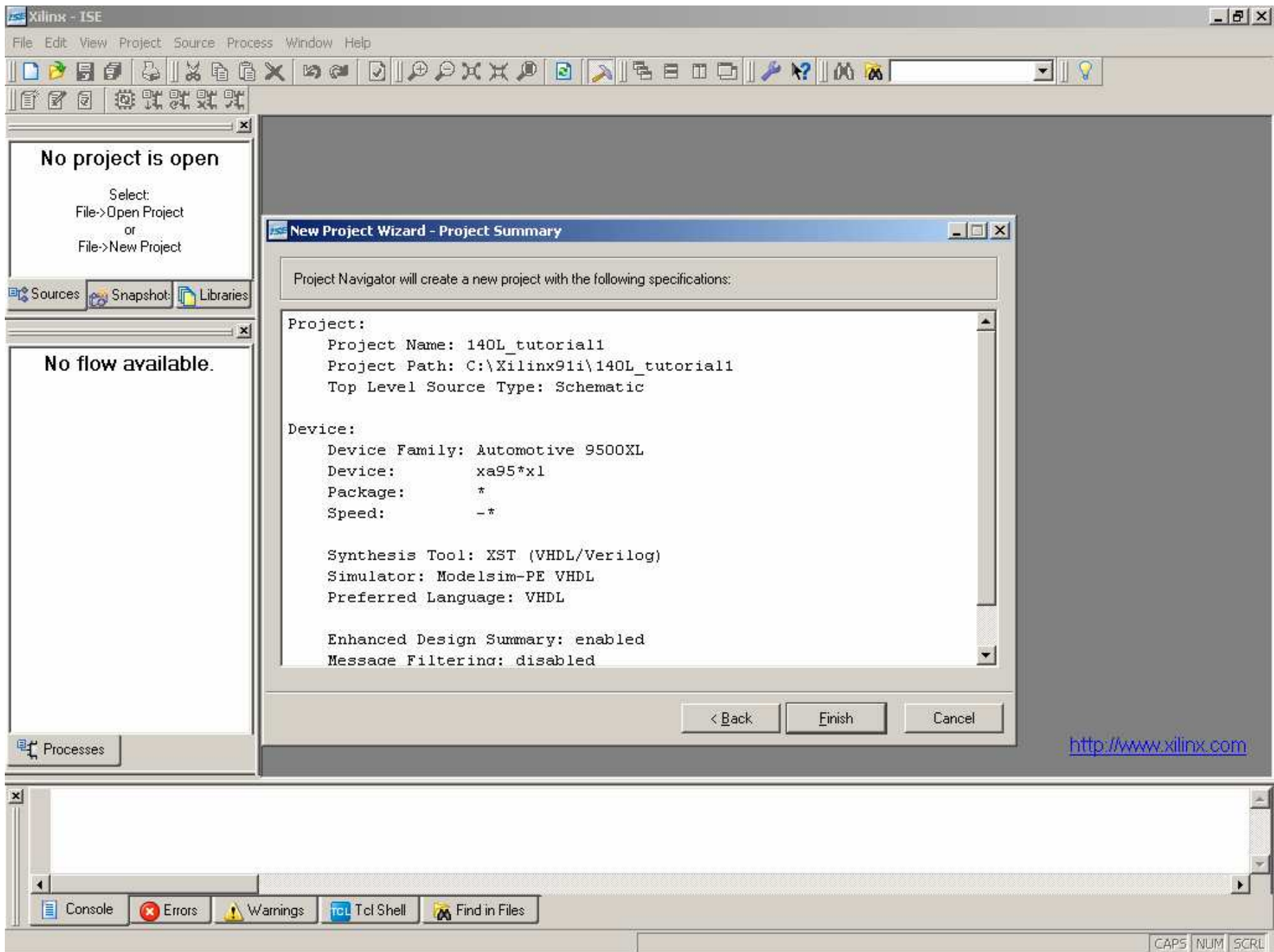
Make sure your Simulator is the **ModelSim-PE Mixed** otherwise your simulation may not work. Leave everything else as default for now. You may change these setting later also. Click Next to continue.



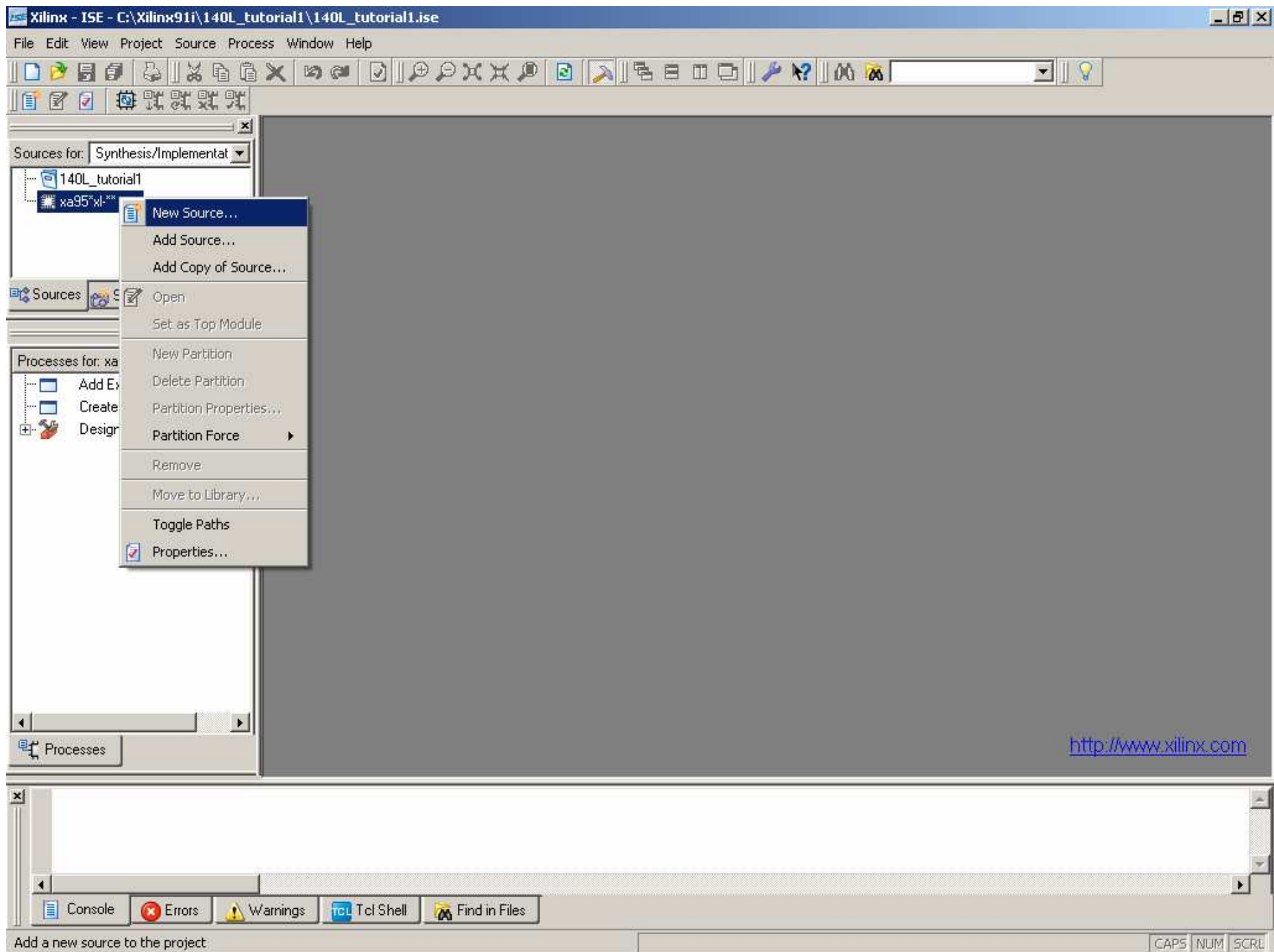
You don't need to create any new files at this time because you can add files later. Click Next to continue.



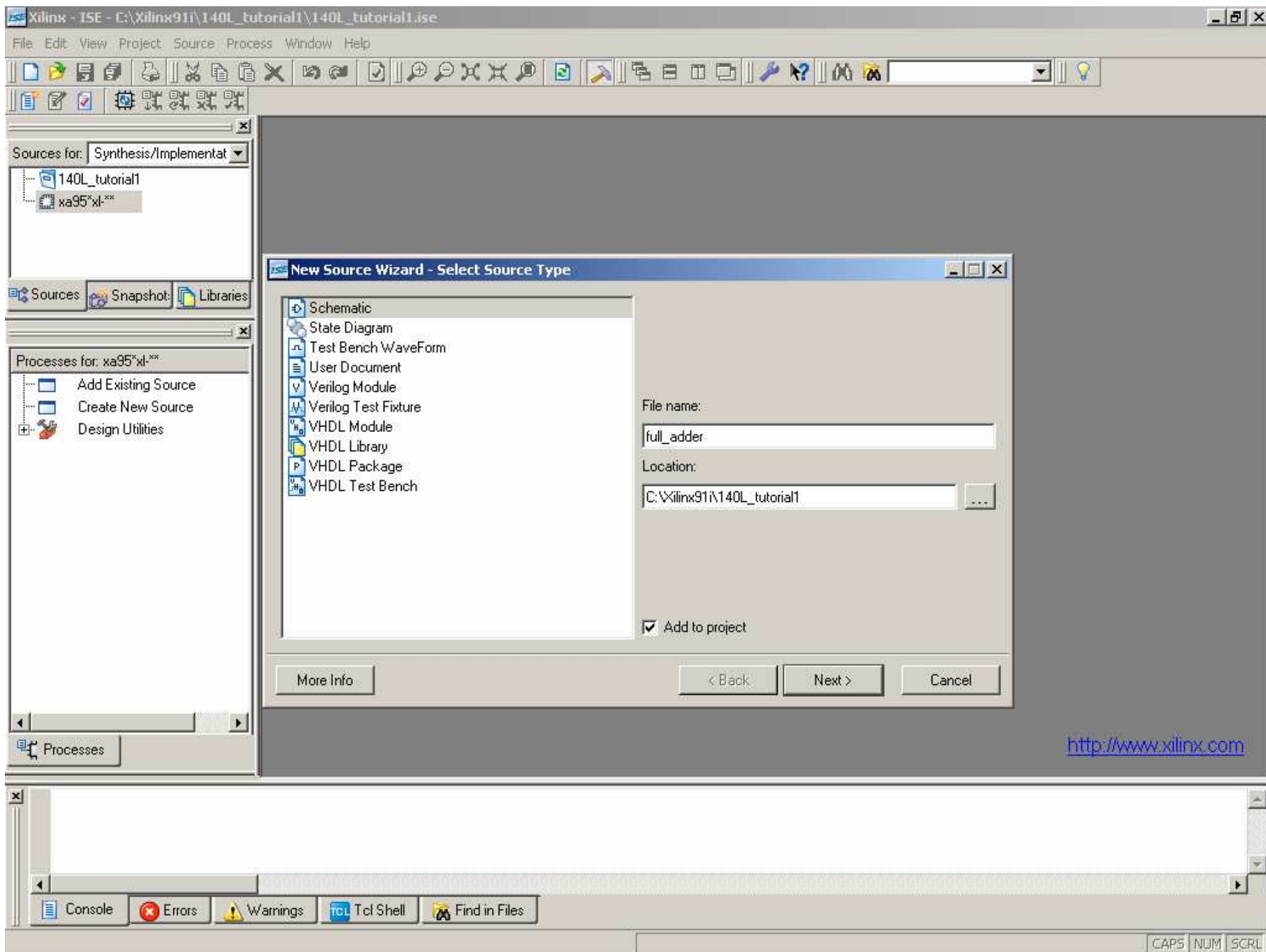
You don't need to add existing files either. So click Next to continue.



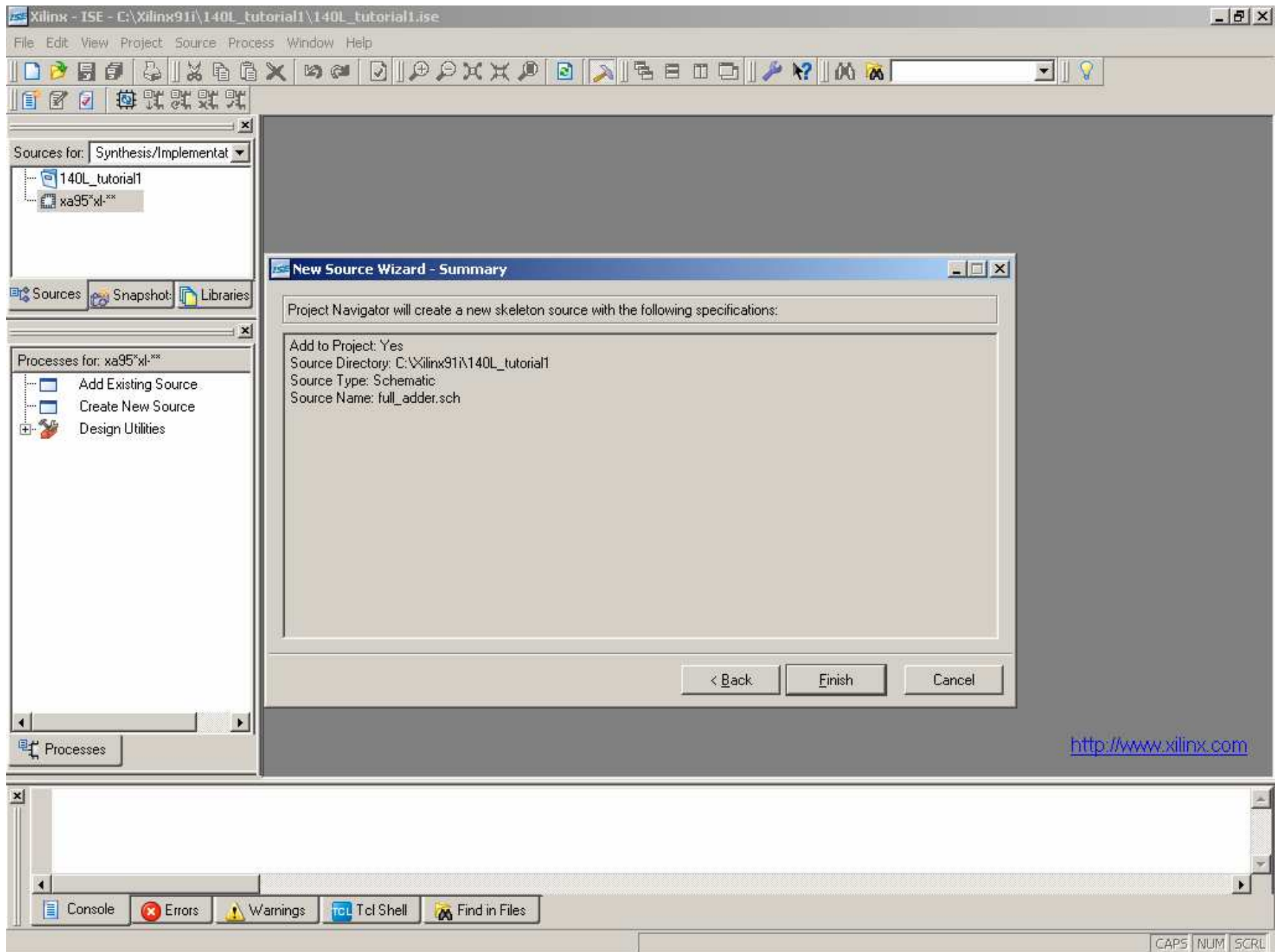
This is a quick summary of what you are creating for the project. Click Finish.



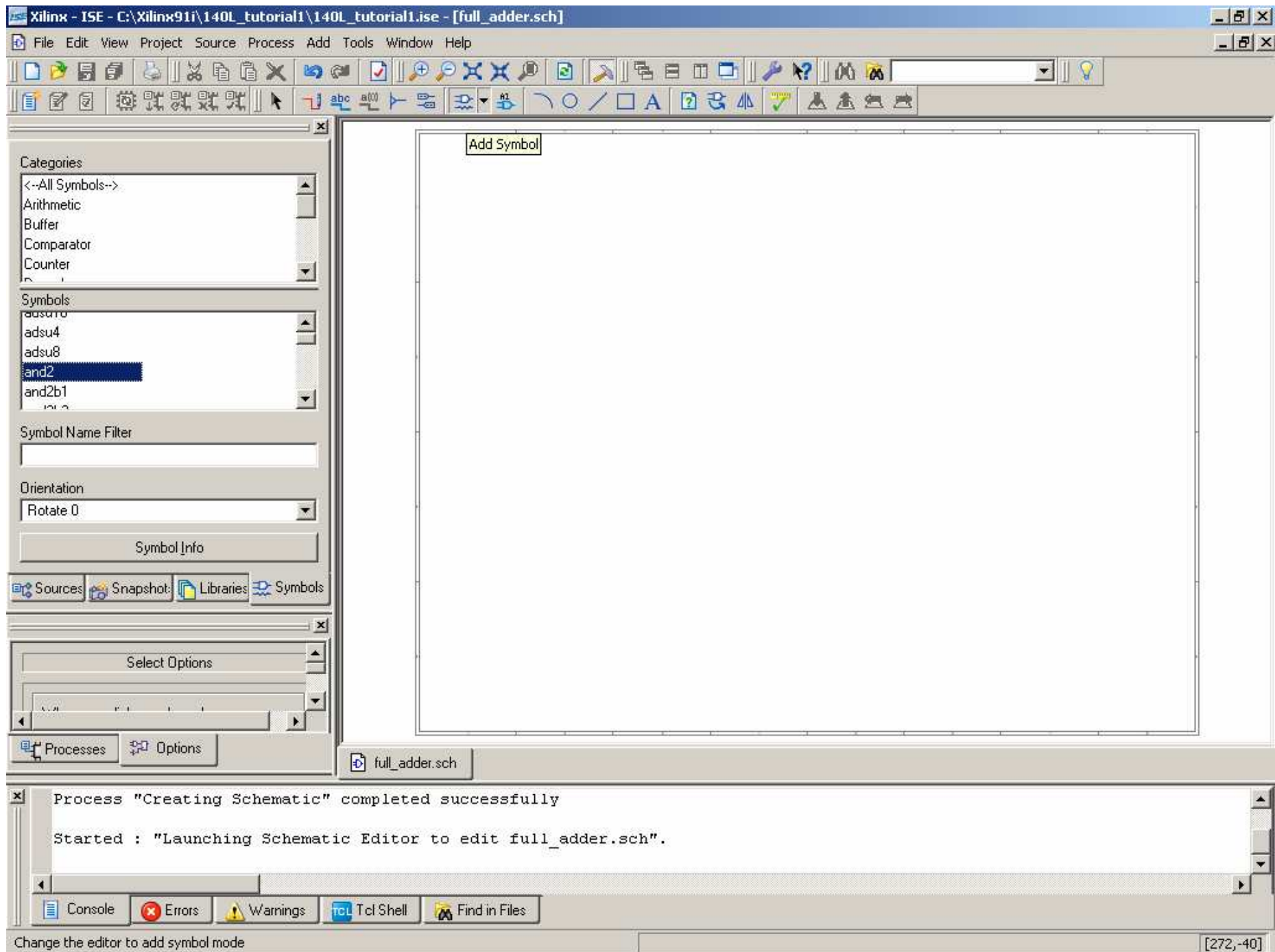
Now, you can add a new Source. Let's build a simple full-adder.



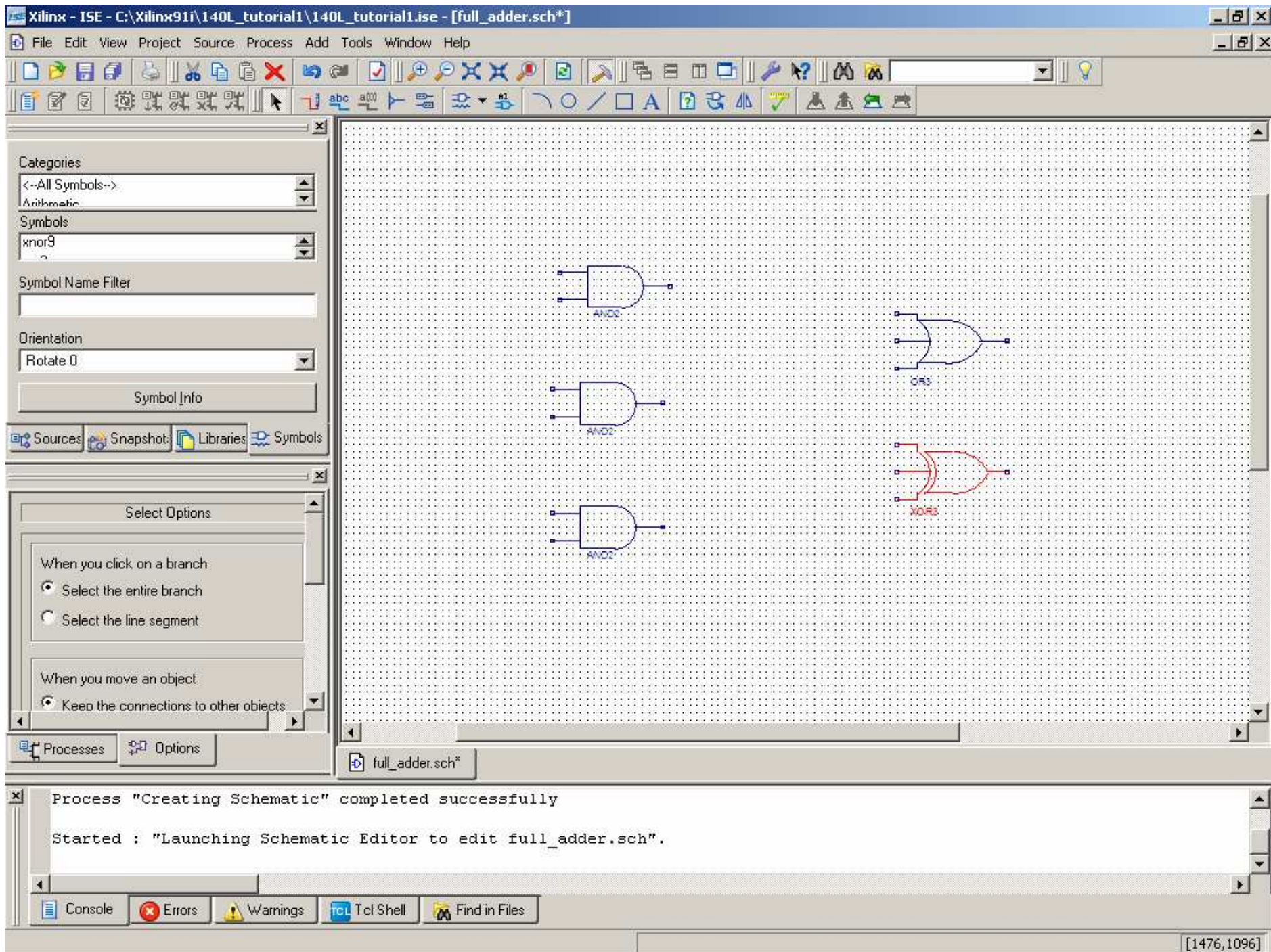
Be sure to select “Schematic” from the left-window list. Enter a file name called “full_adder” and click Next.



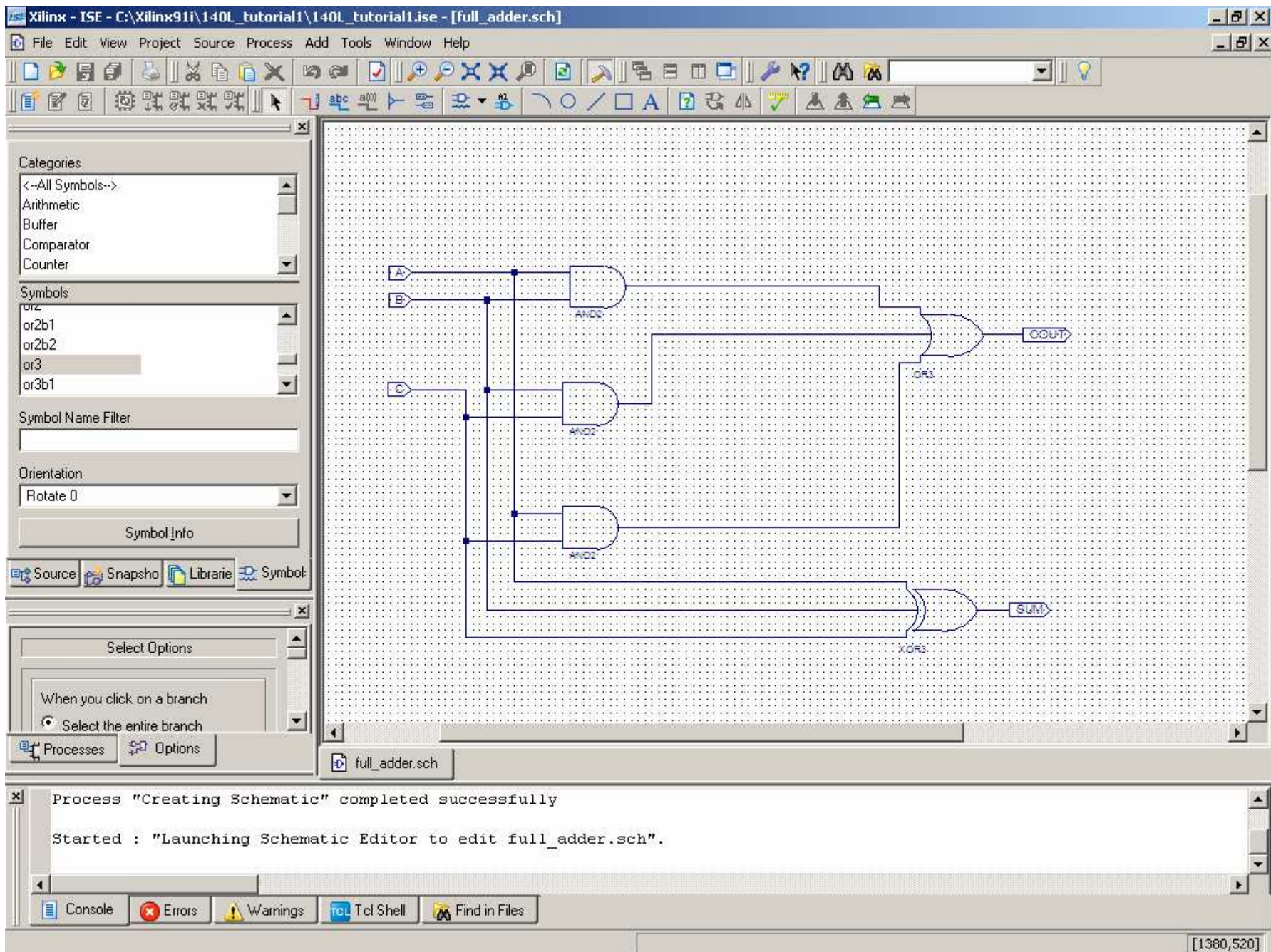
A quick summary is displayed. Click Finish.



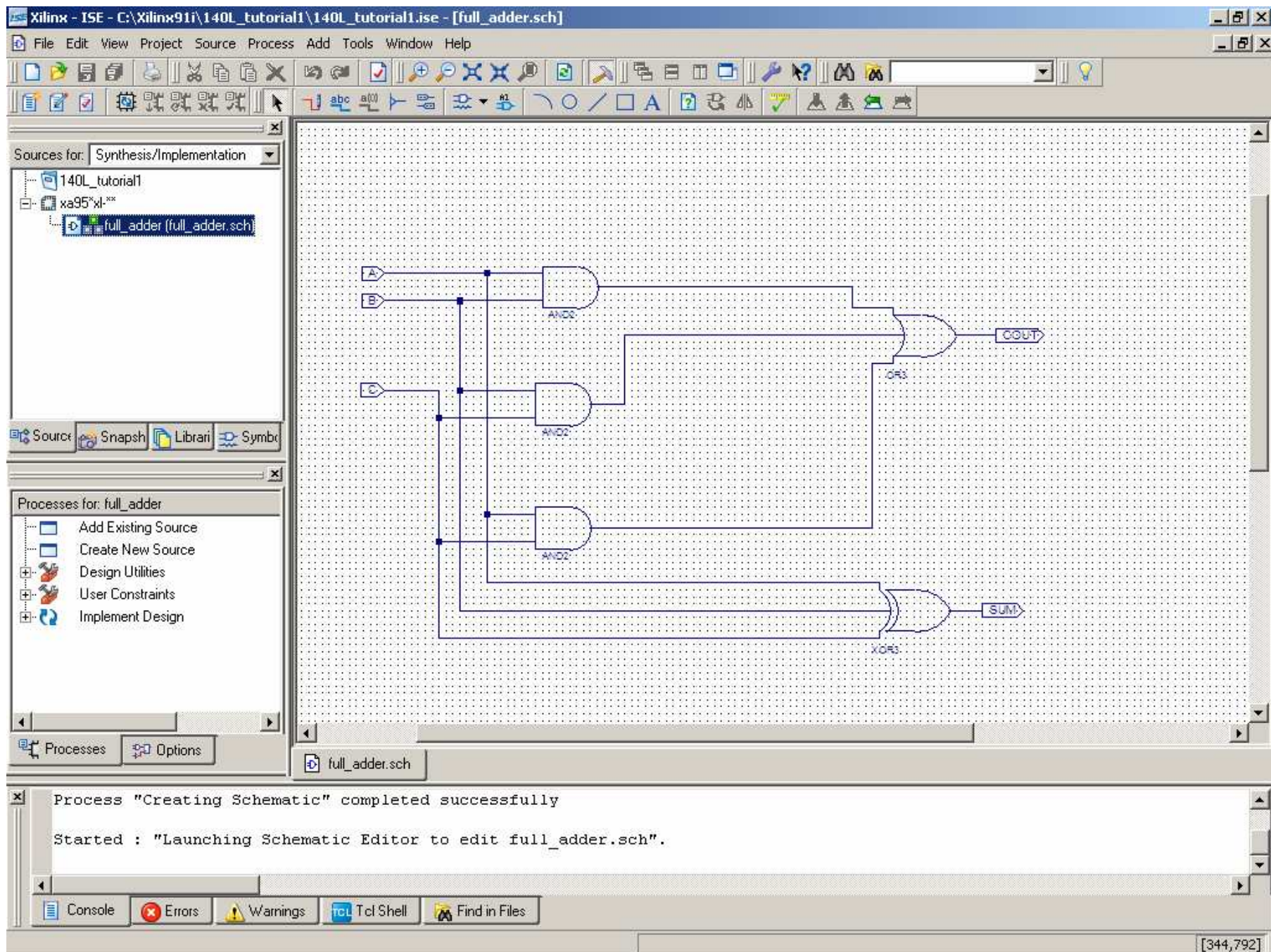
A screen with a blank schematic will appear. Now mouse over the tool bar with a “and-gate” looking symbol. The “Add Symbol” tag will appear. Click on this button. Adjust size of the left pane so you can see the “Symbols” list and select the “and2” gate.



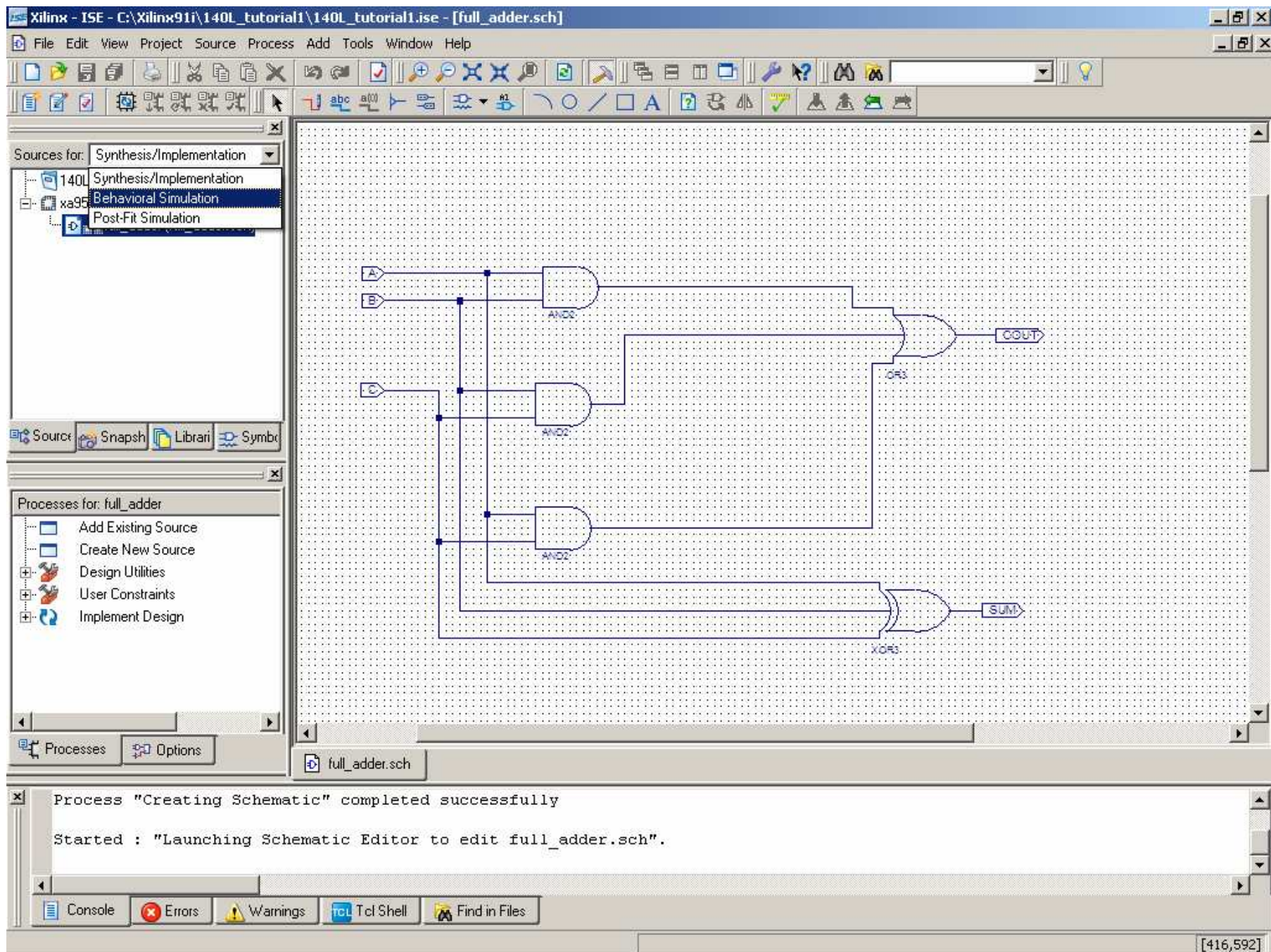
Put three “and2” gates on the schematic area and one “or3” and one “xor3”. You can zoom in and out of this schematic editor with the zoom button in the toolbar.



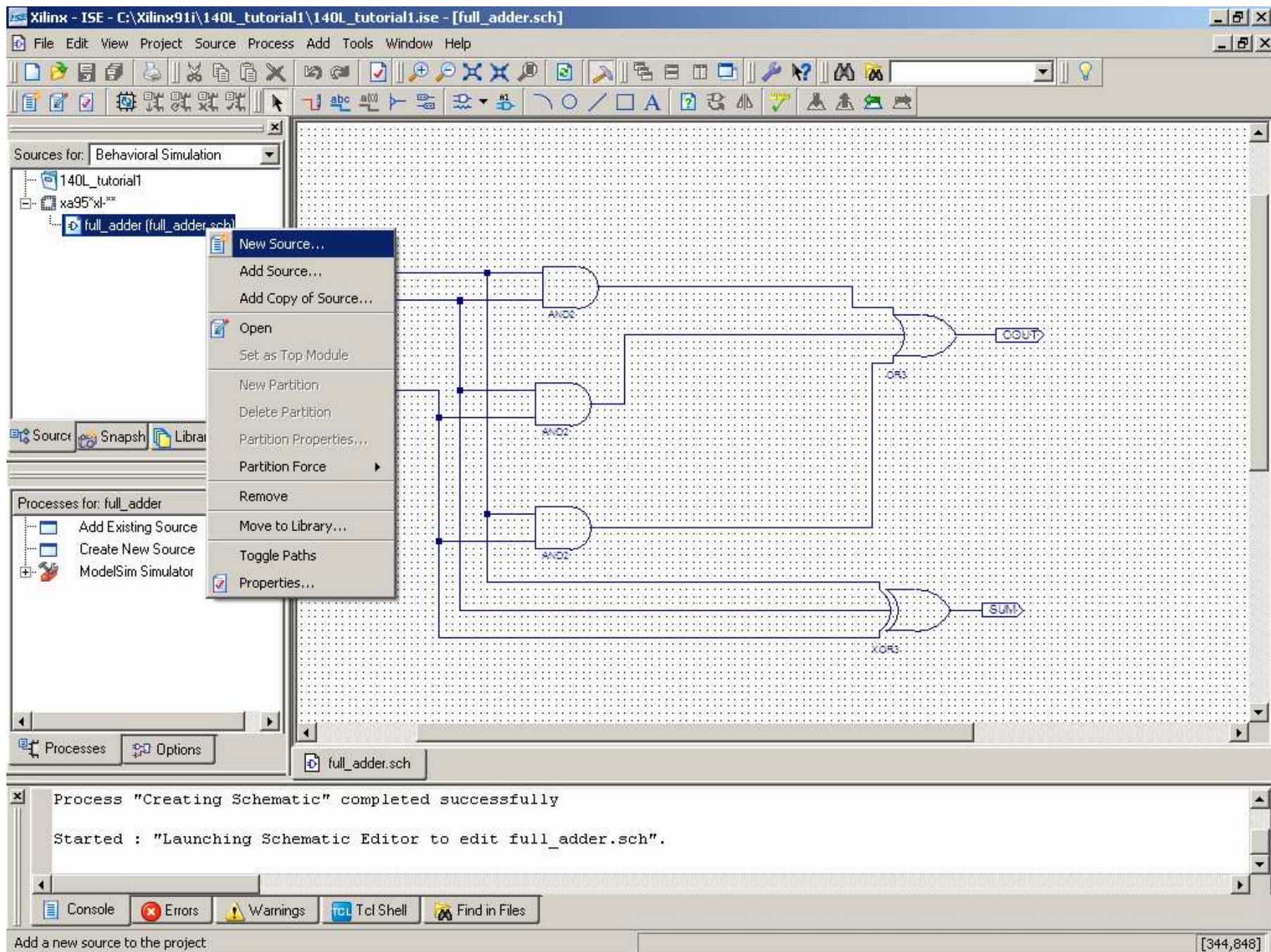
Then, use the “Add Wire” tool (next to the arrow pointer) to add wires. And use the “Add I/O Marker” to add inputs and outputs. To connect wire, you can click once at the begin point and double-click on the end point. Do a little experiment here to see different way to connect wires. You can also right click on the I/O port to rename. Try to create the full-adder schematic as shown above. And save your work!



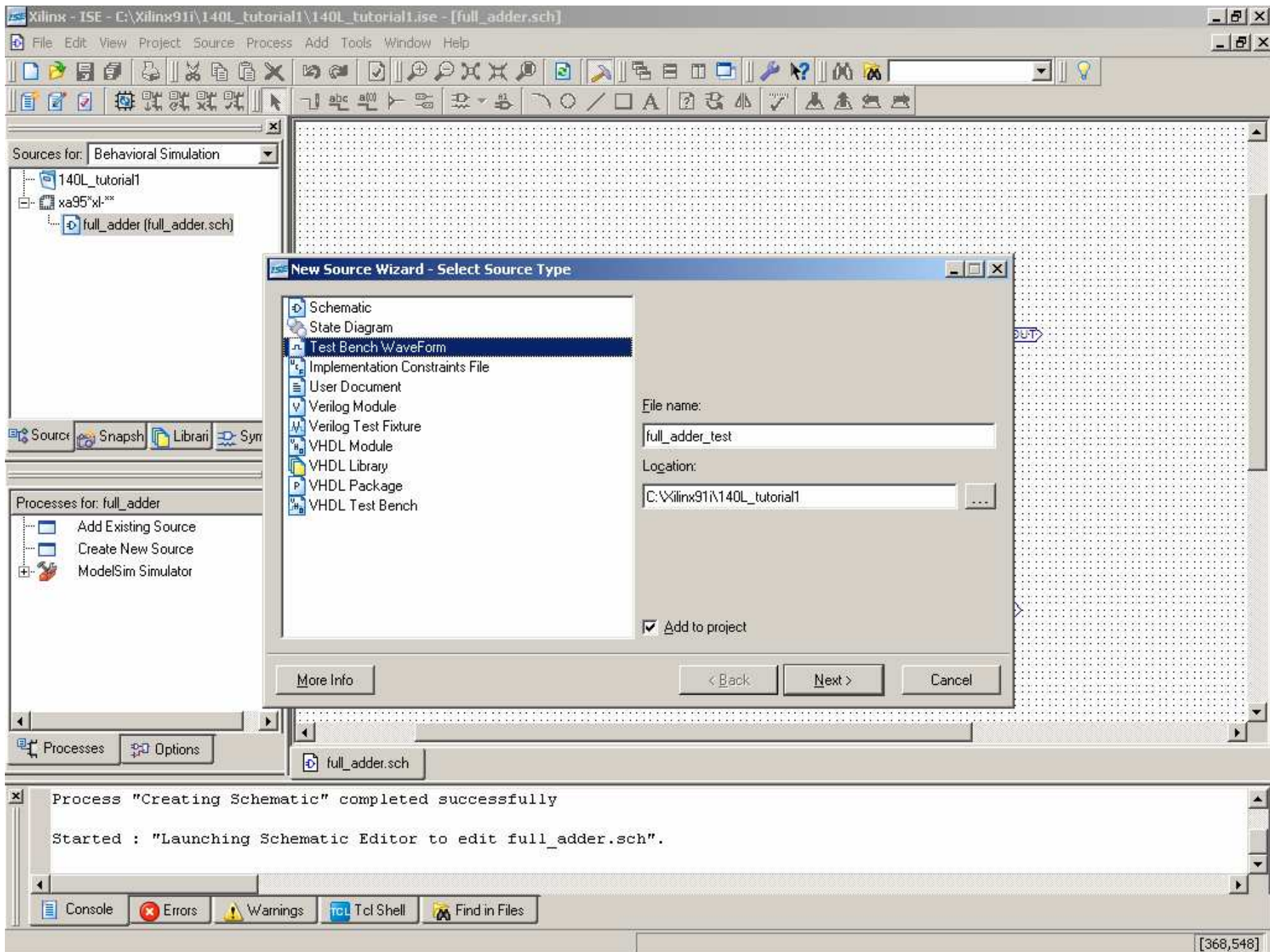
Now, re-adjust the left-pane window so that you see the “Source” pane on the top and the “Processes” pane on the bottom.



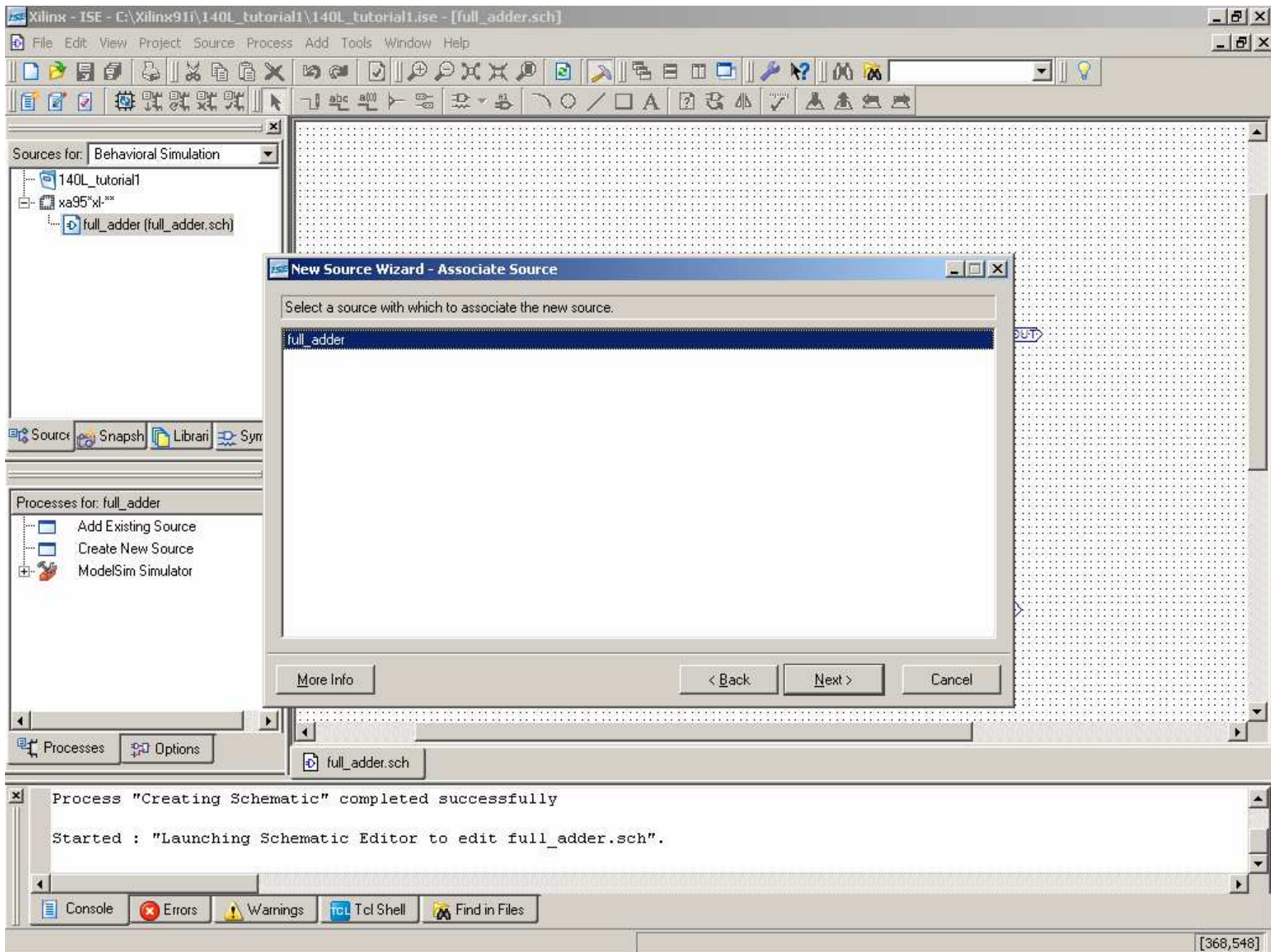
Select the “Behavioral Simulation” from the top-left-pane. Notice the bottom bottom-left pane options changes. You are now ready to test your circuit.



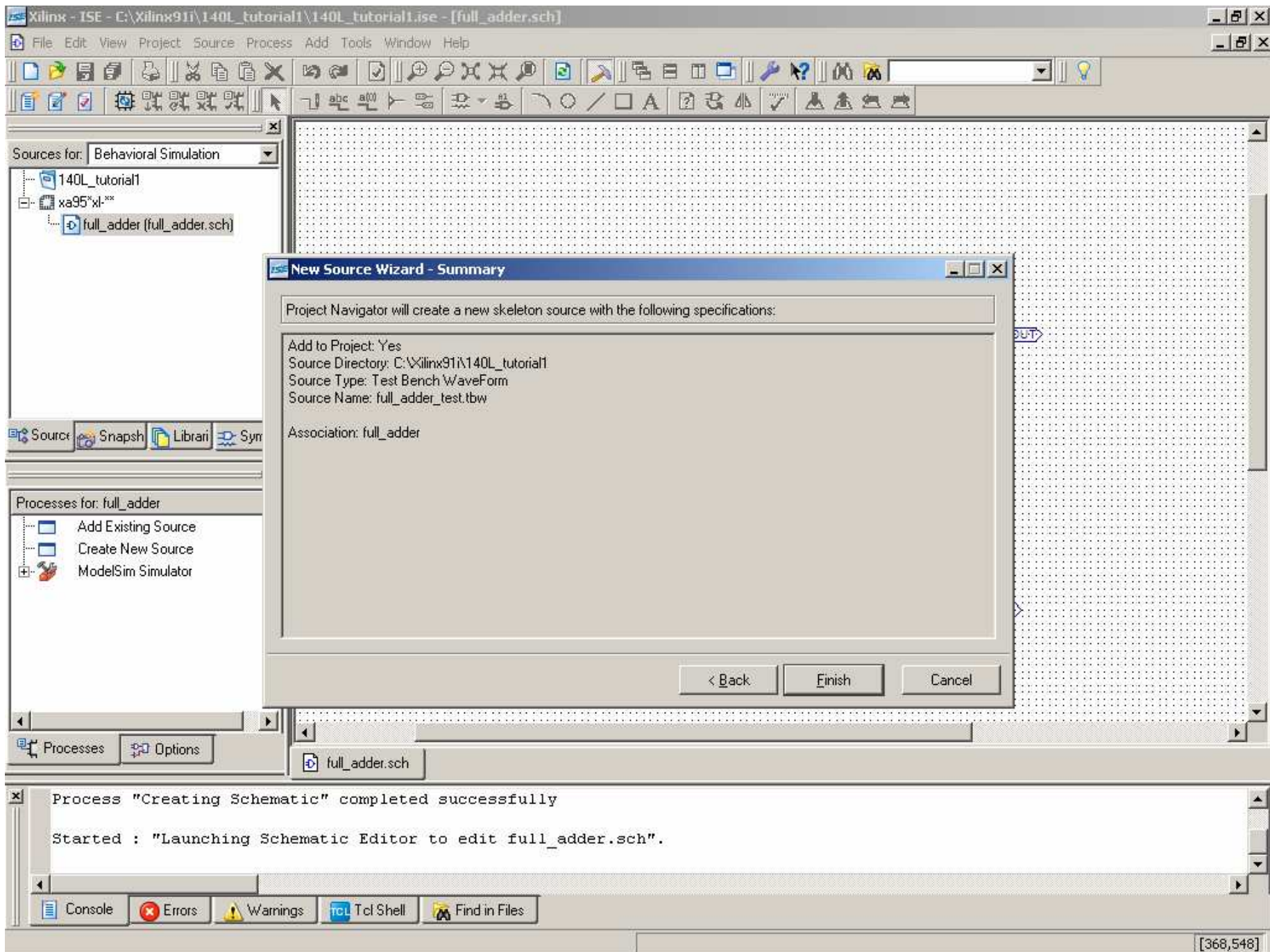
Right click on the full_adder.sch file and select “New Source” to create a test-bench.



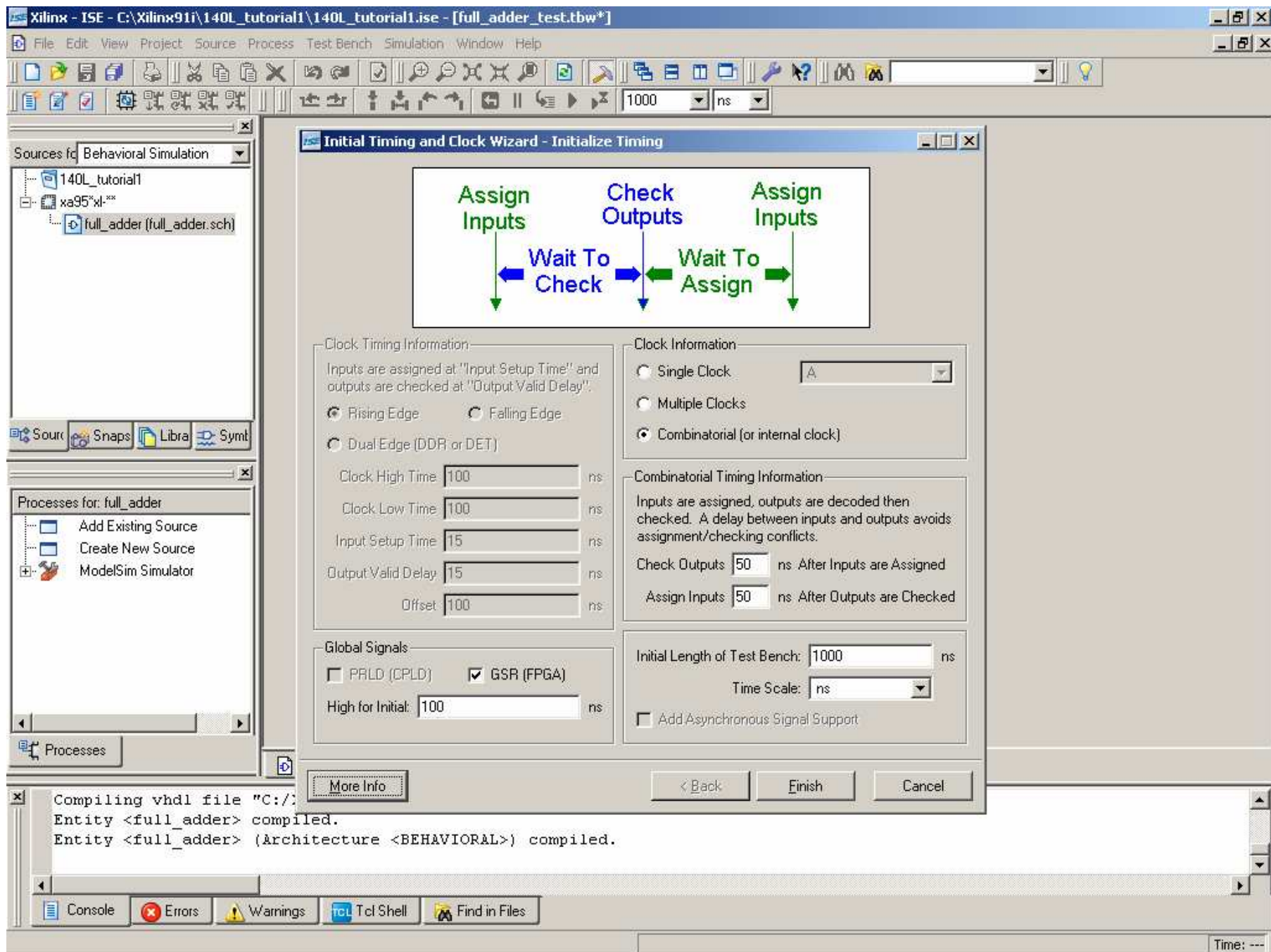
A new window opens. Select the “Test Bench WaveForm” and type in “full_adder_test” in the File name and click Next.



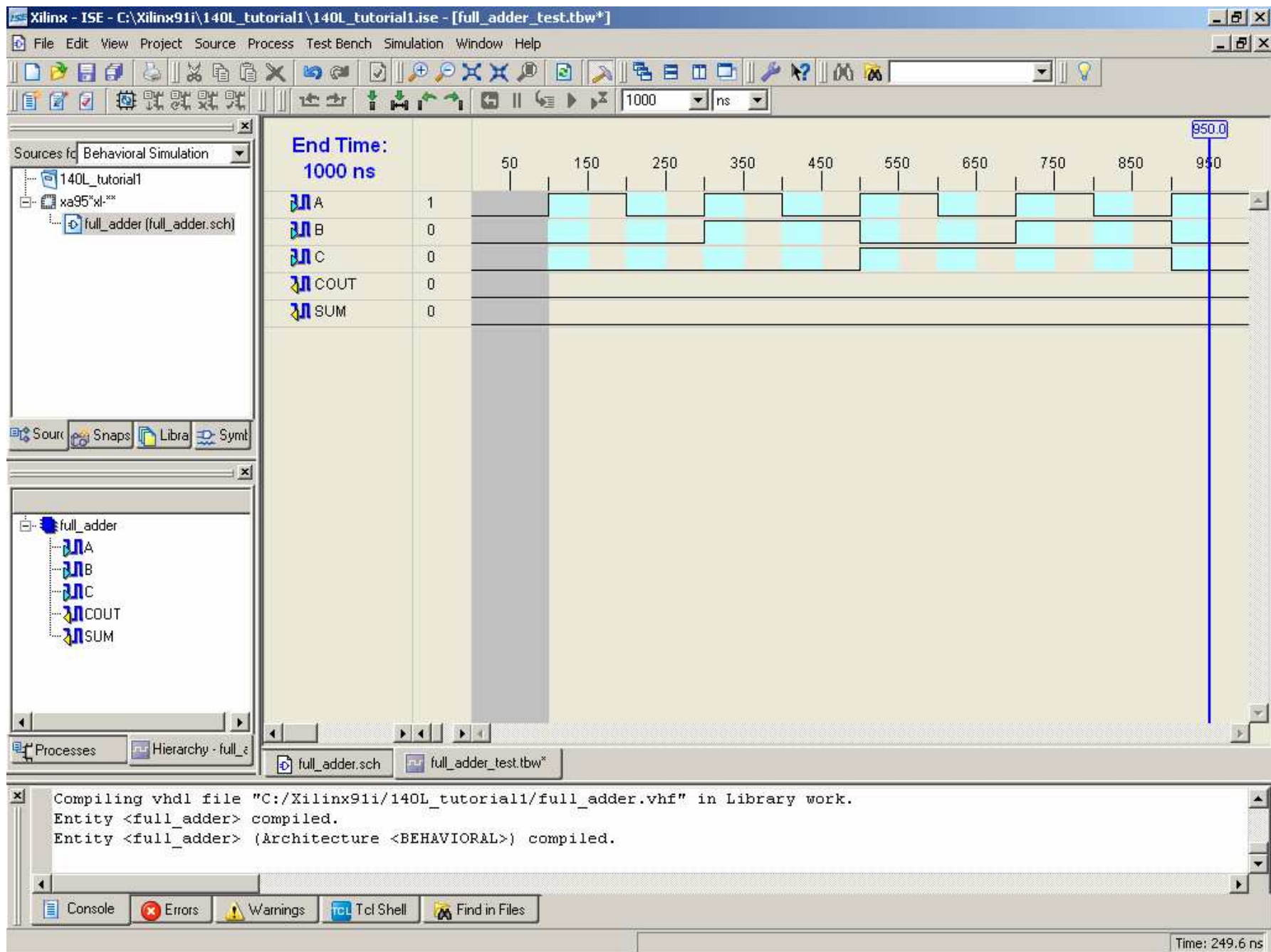
Since we want to create the test for full_adder, simply click on full_adder and then Next button.



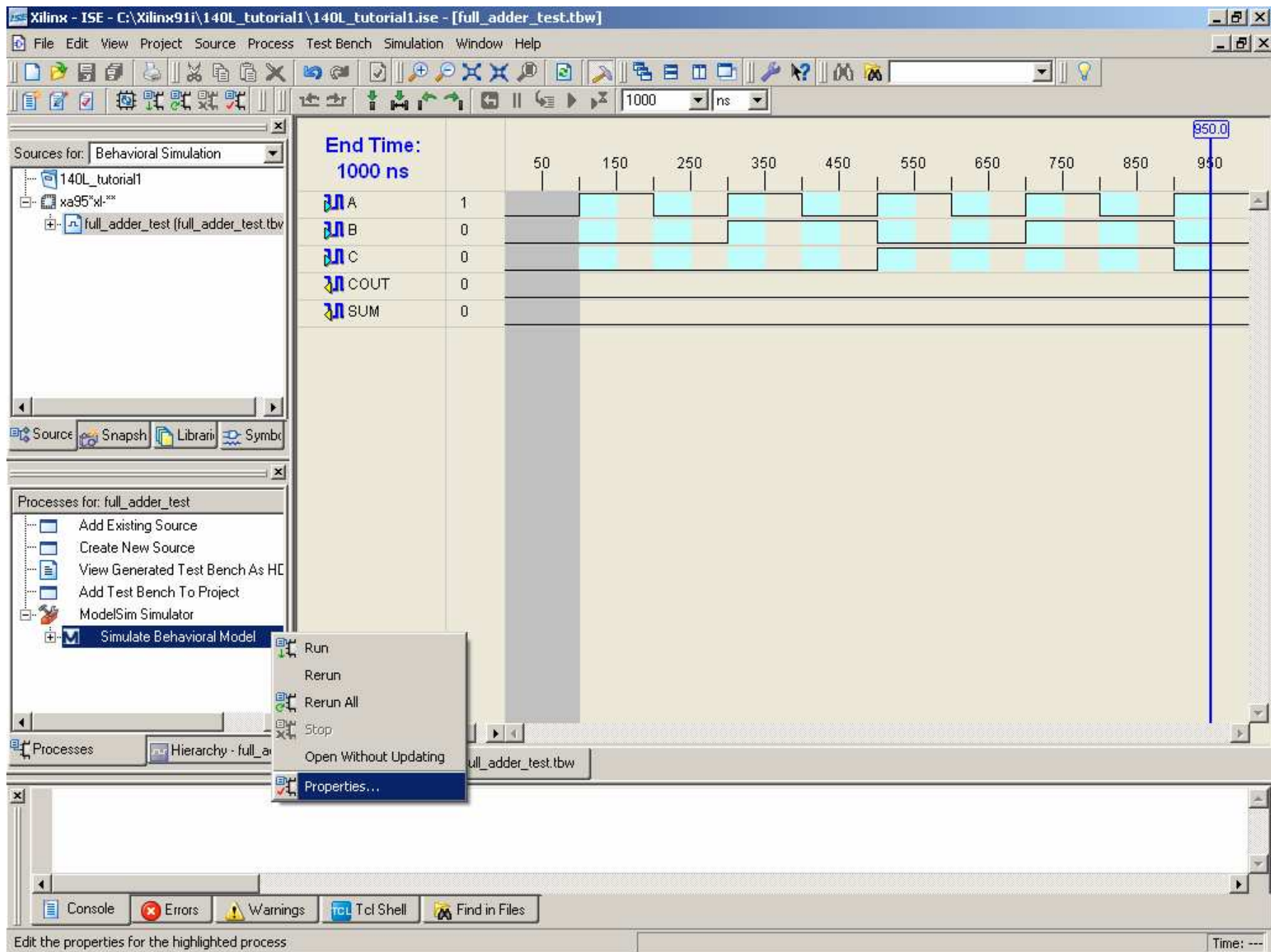
A quick summary screen display. Click Finish.



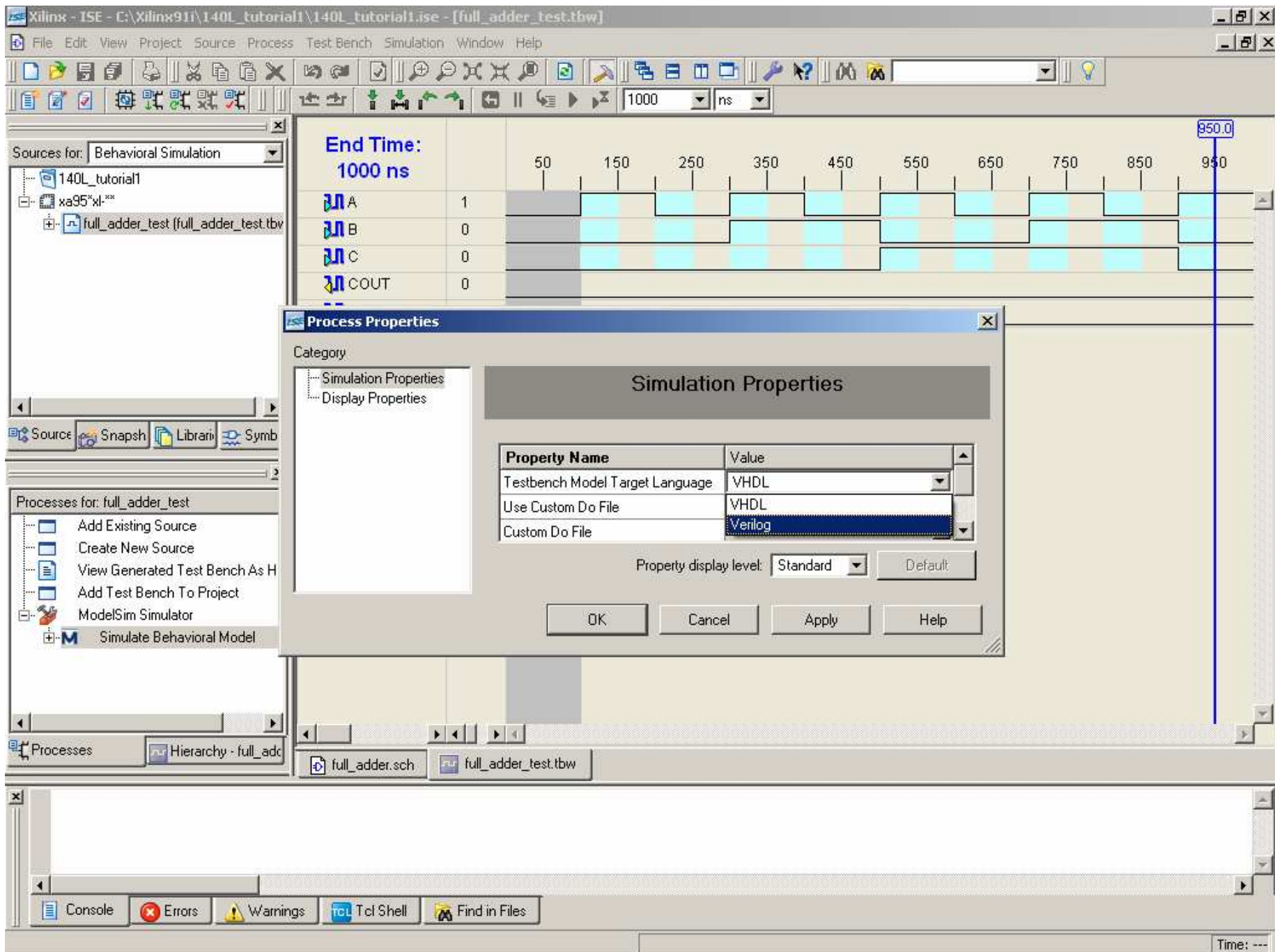
A new window opens to give you some setting on how long you like to simulate. In Clock Information, make sure to select “Combinatorial (or internal clock)” and click Finish.



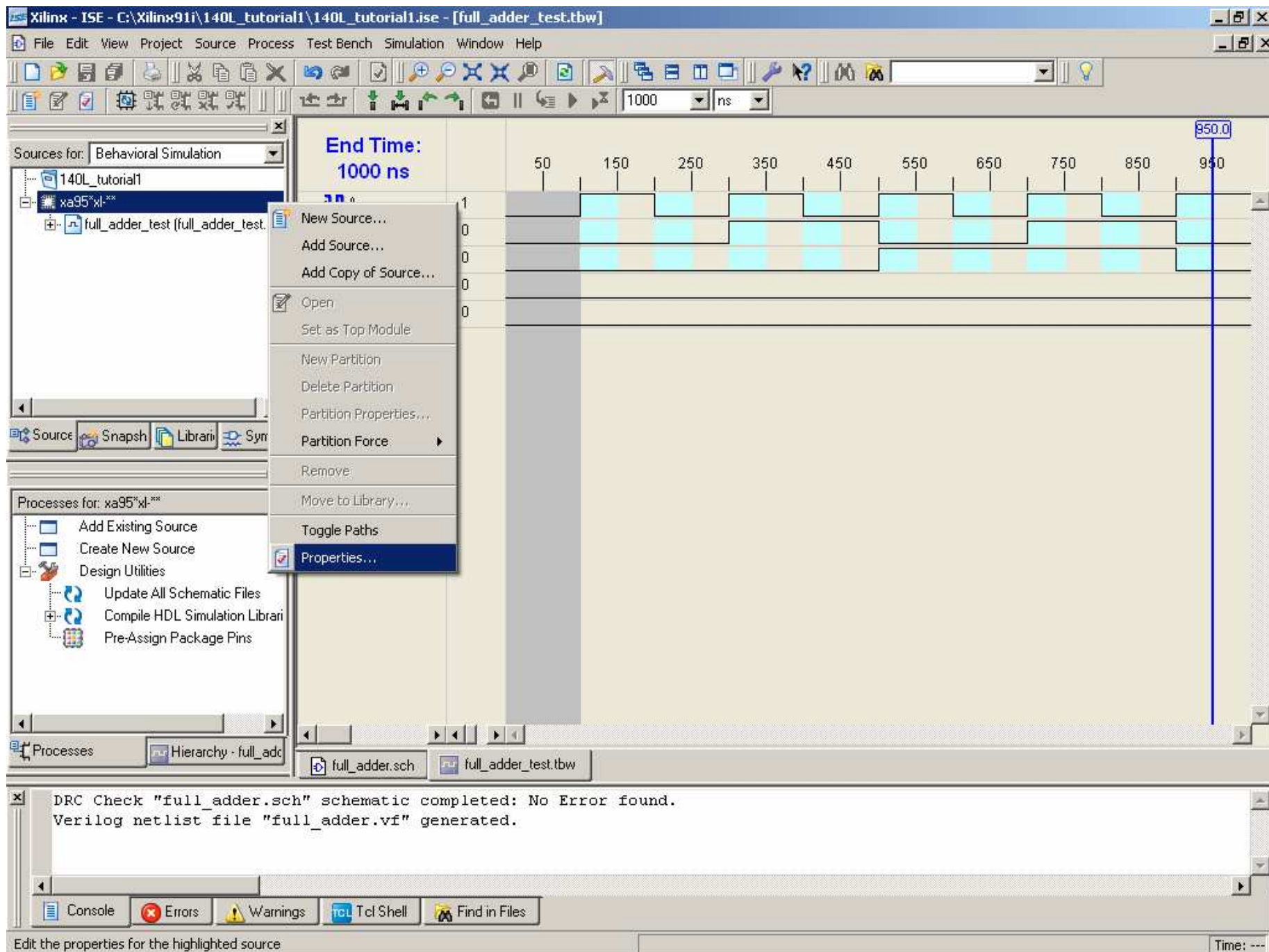
A window of all inputs and outputs are displayed. Go ahead and click on the light-green area of the timing chart to toggle the value. Toggle the A, B, and C so that it counts from 000 to 001 to 010 to 011, all the way to 111 and back to 000 as shown above. Once you have done this, you are ready to run the simulation. Save your simulation (Ctrl-s).



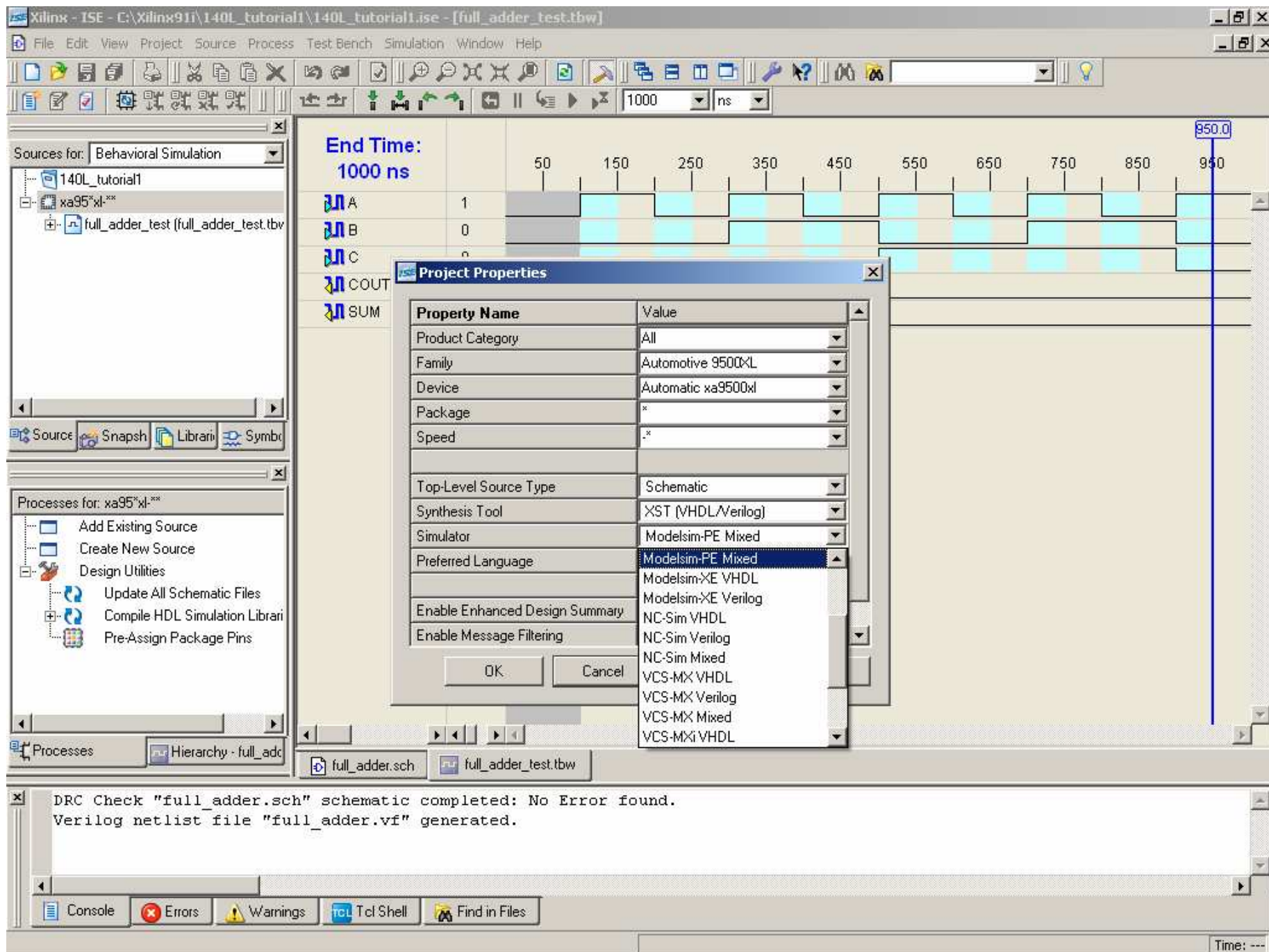
Click on the “Process” tab on the lower left pane and drill down to “Simulate Behavioral Model” and right click to select “Properties”.



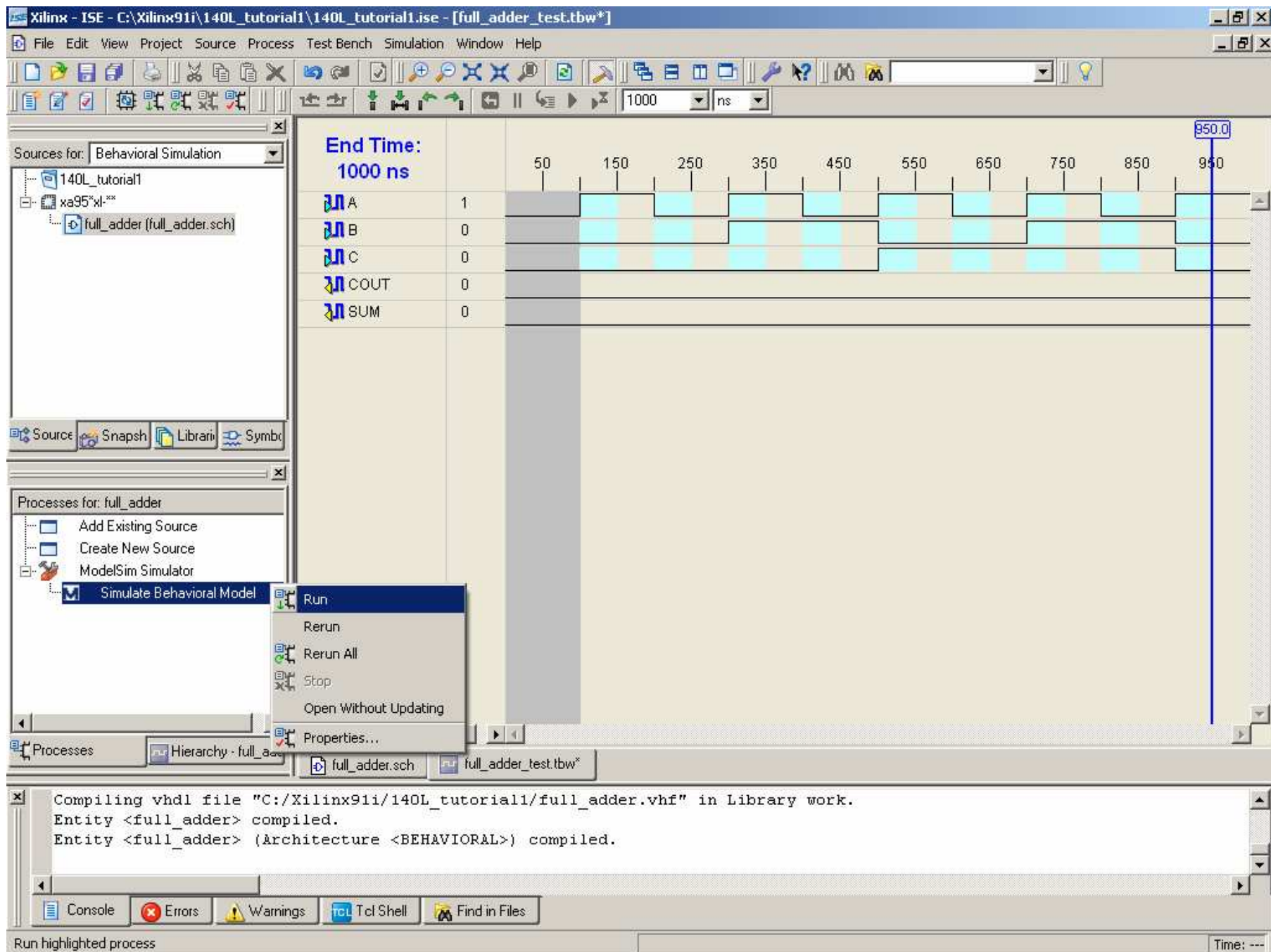
Select the “Verilog” as the Target language. This is the case because Modelsim installation has Verilog language as default language.



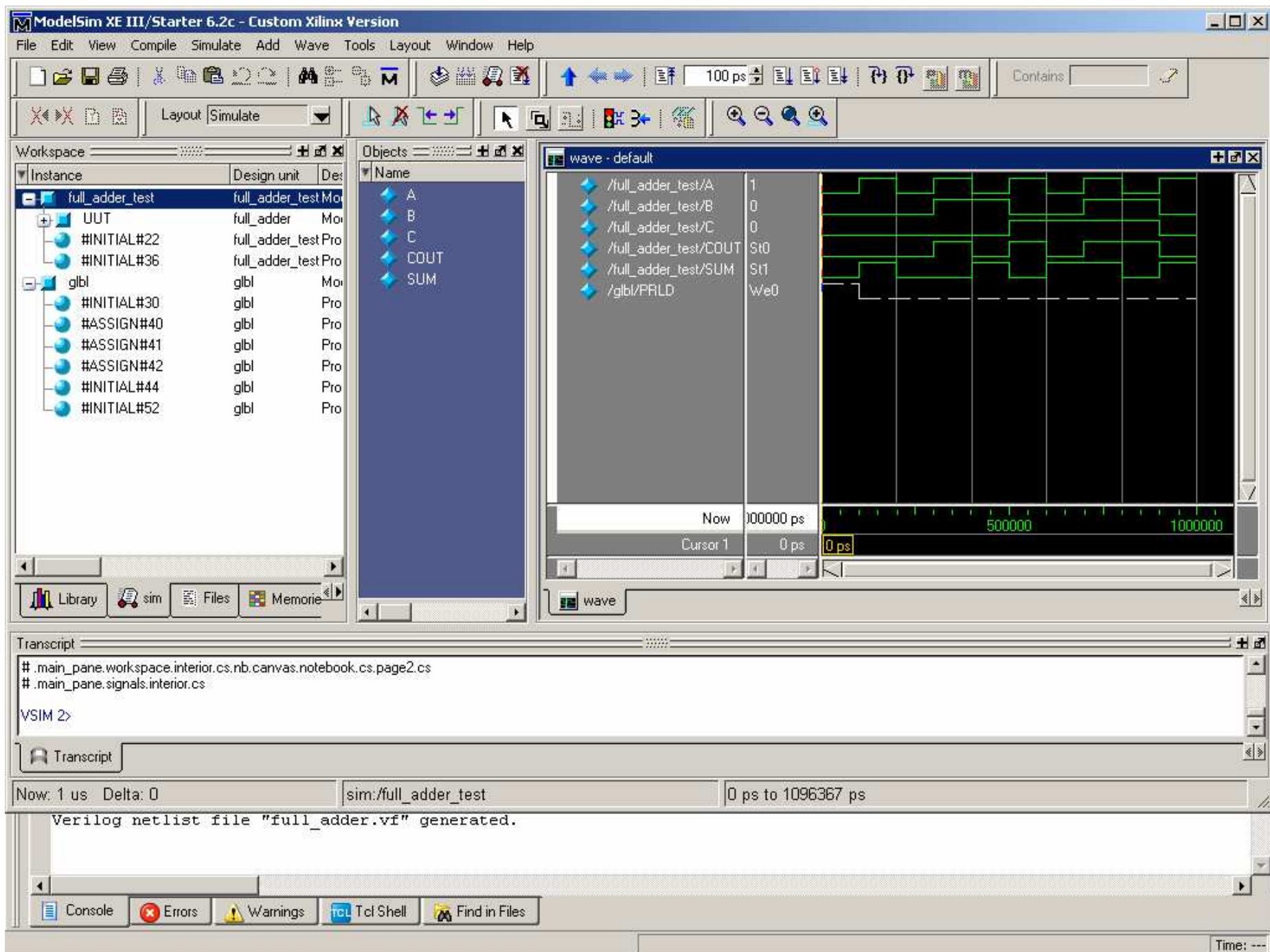
Let's take a look one last time on the properties of this device (xa95*xl-*). Note, the device is the actual hardware chip that you can purchase from Xilinx. You can download your design on this chip and run on it.



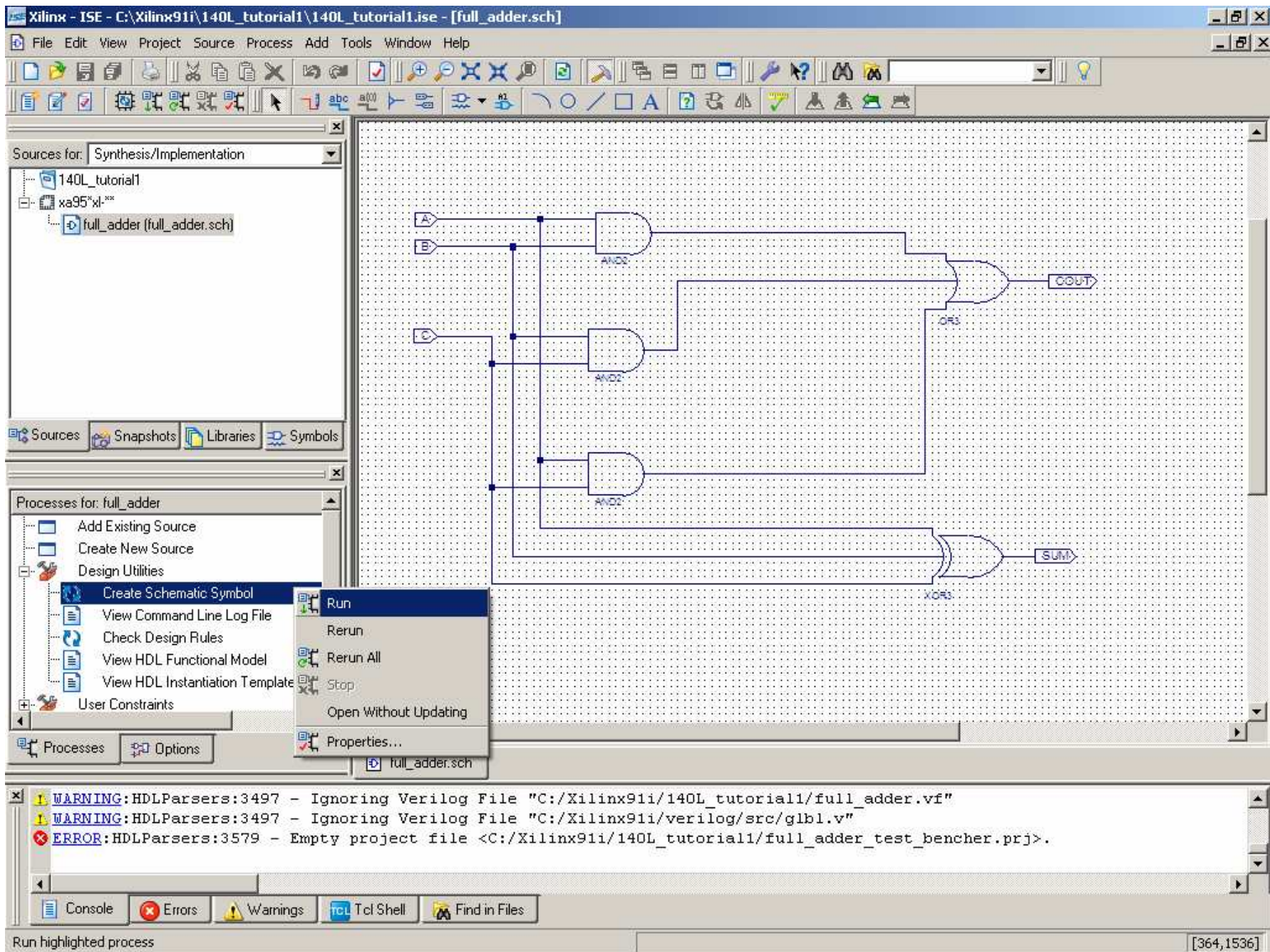
Make sure the Simulator is “ModelSim PE mixed” one last time. Otherwise ModelSim may not work.



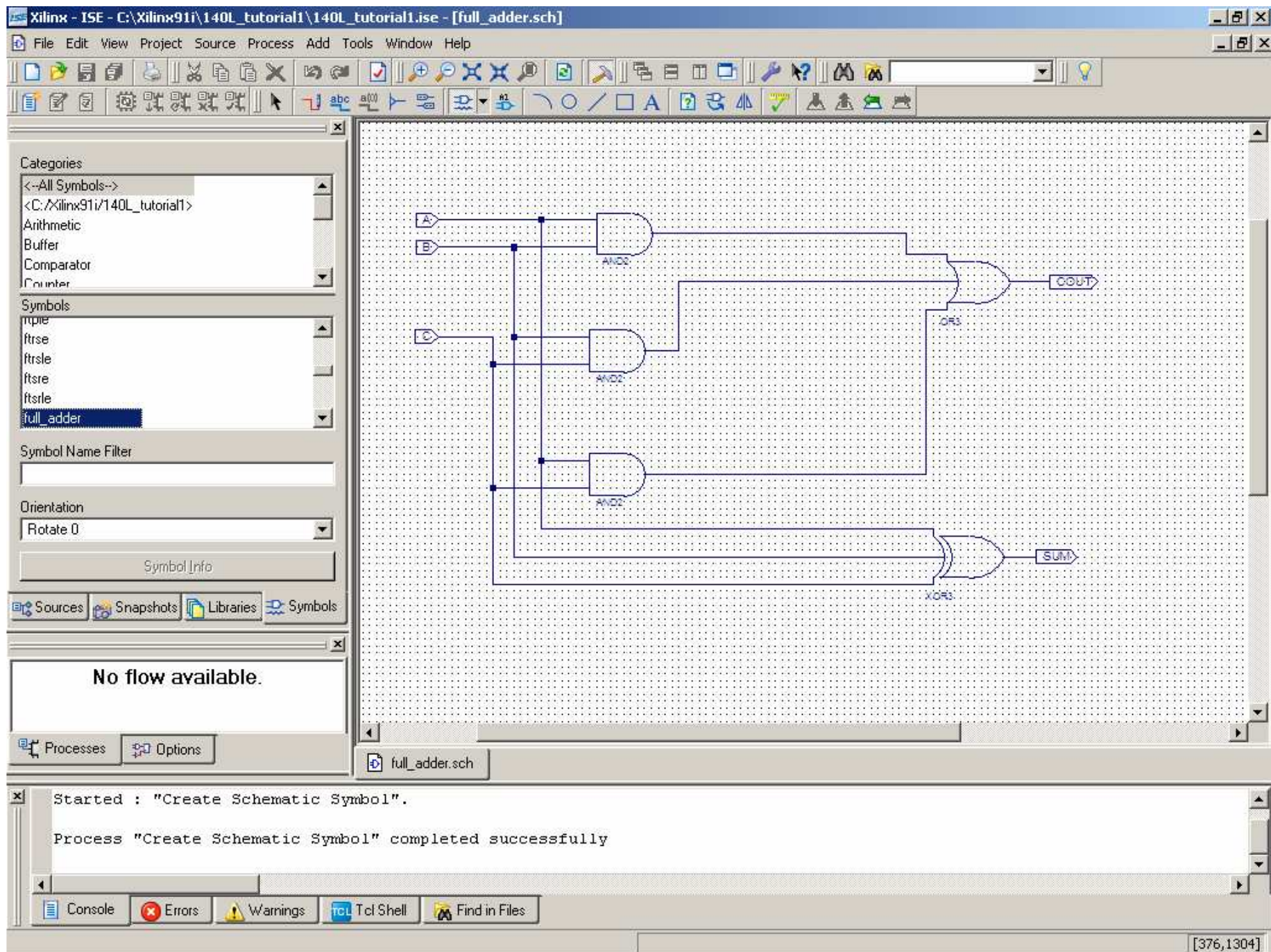
Highlight the full_adder (full_adder.sch) and click on the “Process” tab on the lower left pane and drill down to “Simulate Behavioral Model” and right click to Run the simulation. If everything is successful, you should see the next screen with ModelSim loaded and simulation result. If you can not get the simulation working, try selecting the “ISE Simulator” as the simulator from previous screen. We will accept simulation result from ISE Simulator also. However, it is good to learn ModelSim for it has more feature than ISE Simulator.



If you did not see any error in the Transcript window (lower window) and see only green-color simulation in the timing chart window, your simulation is successfully ran. Try zoom-out and scroll all the way to the left in the timing chart window. You will see the above waveform. Congratulations, you now learn enough skill to do your first lab. The next two pages will show you how to create your own library (full_adder) so you can re-use them many times.



Make sure you select the “Synthesis/Implementation” drop down on the upper-left of the window. And select the “Create Schematic Symbol” under the “Processes” tab and click Run. This will create a new symbol in the symbol-list (see next page). Synthesis is a process which takes a design and turns it into hardware net-list which can be downloaded to the chip (advanced topic).



By expanding Symbols window and make sure the category “All Symbols” is highlighted, you now see the “full_adder” as one of the symbols in the list. You can now use this full_adder symbol to build larger circuits (4-bit adder for example).