CSE 140L Hardware Lab Three, Fall 2002

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Finite State Machine
Due date: November 19

Objective

In this lab, we will build a pattern recognizer. We first use the state diagram to specify the system as a finite state machine. We then use HDL for the implementation. We will try different state assignments, use Mealy and Moore machines and, compare the results. Note that in this lab, we use FPGA Family: Spartan, Part: S05PC84 and Speed: 4.

The Finite State Machine

The finite state machine is a pattern recognizer, which has one output bit, z, and one input bit, x. Whenever the input string x(t, t-7) matches the pattern "10011000" or "00110001", the machine outputs a ’1’ for one clock cycle. Otherwise, the output is ’0’.

Part 1. Tutorial

Go through the ABEL-HDL Primer and Tutorial 7 State Editor posted on http://www.prenhall.com/xilinx. Write a summary of the tutorials commenting on the strength of ABEL in less than 40 words.

Part 2. Mealy Machine

i. Implement the pattern recognizer as a Mealy machine. Try three different coding for state assignment. (hint: Use the state diagram to specify the machine. Convert the specification to an ABEL program. Edit the program and synthesize the machine as a macro cell.)

ii. Given an input sequence x= "1100110000110001", display the timing diagrams of the three implementations. (hint: Initialize the state to start the simulation)

iii. Change the input signal to demonstrate the glitch of the Mealy machine.

Part 3. Moore Machine

Implement the pattern recognizer as a Moore machine. Use three different codes for state assignment.

i. Given an input sequence x= "1100110000110001", display the timing diagrams of the three implementations.

ii. Demonstrate the response of the input signal that causes the glitch in Mealy machine.

Part 4. Comparison

Use a table to compare the above six different implementations (three different state assignments for both Mealy and Moore machines) in terms of the number of states, number of flip-flops, number of lines of ABEL codes, number of Configurable Logic Blocks (CLBs: boxes in layout).

Report

Title page:

Names of students and due date.

Title of the lab and objective.

A brief description of each person's contribution.

Content:

Part 1: A summary with less than 40 words.

Part 2: i. one state diagram, three ABEL programs, ii. three timing diagrams, iii. One timing diagram.

Part 3: i. one state diagram, three ABEL programs, ii. three timing diagrams, iii. one timing diagram.

Part 4: A table.

Grading

90% will based on the completeness and correctness of the report. 10% will based on the neatness, organization, and following instruction of the report format.